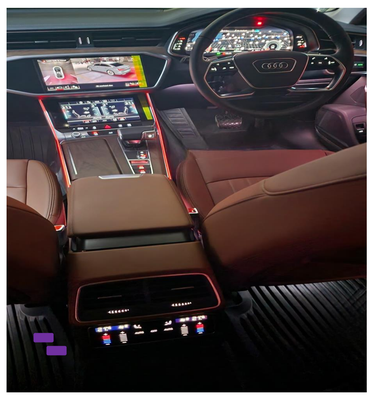
Overcoming the roadblocks in Display Port Automotive Extensions verification

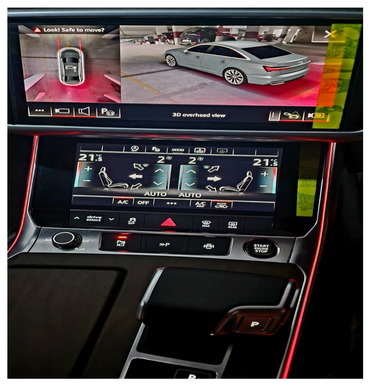
Thenmozhy Kaliyamurthy, Meenakshy Ramachandran

Pankaj Sharma, Nusrat Ali

Problem Statement/Introduction

- Modern automotive displays use DisplayPort(DP) or Embedded DisplayPort(eDP) to carry video data to the displays.
- VESA's DisplayPort Automotive Extensions(DP AE) protocol adds automotive-grade functional safety and security to DP and eDP.
- Follows ISO26262, an international standard for functional safety in the automotive industry.
- Chip manufactures are adopting DP AE => Need an optimized testbench(TB) to ensure product quality and shorter time to market(TTM).





Challenges	Impact
Complexity in DP AE TB integration	Delay in starting verification -> longer TTM
Difficulty in simulating attack scenarios	Quality compromise due to missing design vulnerabilities
High simulation time	Delay in verification closure -> longer TTM

Proposed Methodology/Advantages

- The DP AE test suite is a plug and play environment with a lot of features to help the users verify the safety and security of the display system.
- We have enhanced the existing DP test suite to support the DP AE specification.
- Existing DP test suite customers can continue using the environment as it is for validating the DP AE features, without any integration and start-off challenges.

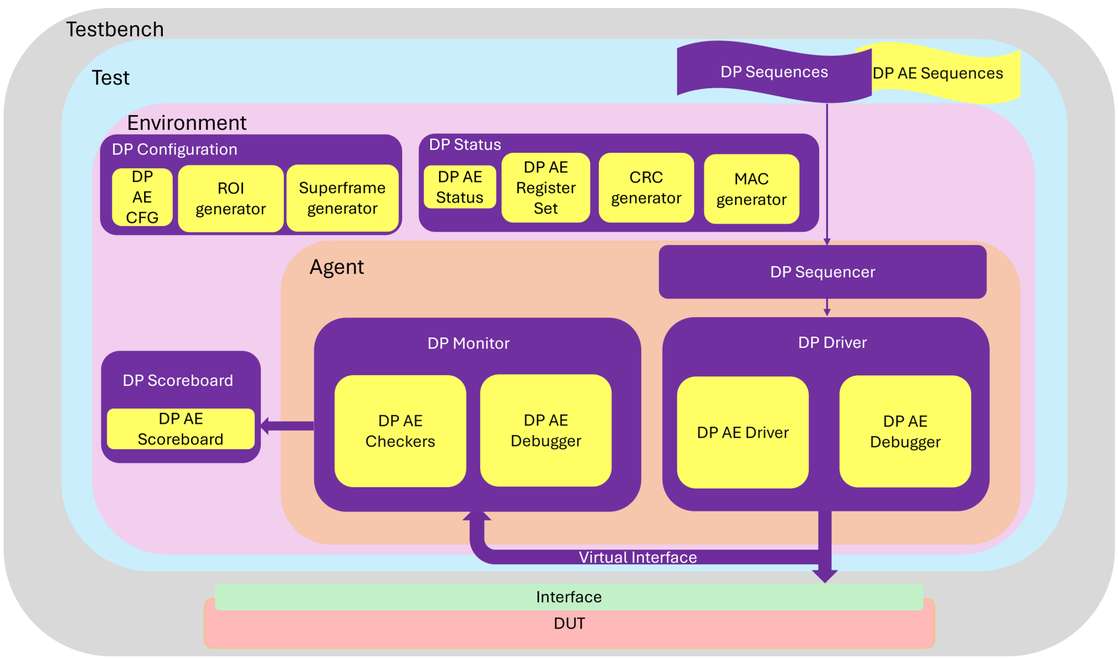
Using our DP AE test suite helps in the following:

✓Ensures the displays meet functional safety standards and work as expected -> prevents accidents and saves lives

✓Identifies weakness in the security of design -> Prevents cyber attacks.

Advantages	Impact
Fully random sequences	Highly configurable
Scaled frames support	Saves simulation time
Bypass standard procedures	Eliminates redundancy
Lookup table-based CRC	High performance
Standard C code for MAC	Re-usable and replaceable
Error injection mechanism	Checks design robustness
Advanced debugging techniques	Detailed debugging for specific feature

Implementation Details/Diagram



Implementation Details/Flow Chart

Component	Description
DP AE Sequences	Validates all Functional Safety (FuSa) and Security features as per the DP AE specification.
Testcases	Reusable across multiple topologies (Source, Sink, Branch) and modes (Single/Multi Stream DP and eDP) via a runtime switch.
DP AE Configuration	Offers user control for verifying specific DP AE features.
CRC Generator	Validates FuSa using a VIP-optimized lookup table-based CRC algorithm, faster than bit-by-bit methods for large data.
MAC Generator	Validates Security using AES-GMAC implemented in C and integrated via SystemVerilog DPI. Reusable and replaceable.
ROI Generator	Generates Regions of Interest (ROIs) that require additional protection.
Superframe Generator	Creates superframes with multiple subframes, each directed to different Sink devices.
DP AE Status	Status variables are accessible across testbench modules; users can extract relevant information.
DP AE Driver	Generates and transmits AE SDP packets containing FuSa and Security data.
DP AE Checkers	Performs detailed checks on received AE SDP packets, validating both content and timing.
DP AE Debugger	Advanced debugging via interface signals, trace files, and configurable log messages. Runtime switches enable feature-specific logs (e.g., detailed CRC mismatch tracing).
DP AE Scoreboard	Ensures that the transmitted AE_SDP matches the received AE_SDP.

Results Table

```
1 UVM_INFO svt_dp_tx.sv(2321) @ 1221536.969ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=73ad1b62 for line=0
  in frame=4, ae_pix_crc_prev_valid=0, ae_pix_crc_prev=0
2 UVM_INFO svt_dp_tx.sv(2321) @ 1253310.425ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=655db79b for line=1
  in frame=4, ae_pix_crc_prev_valid=1, ae_pix_crc_prev=73ad1b62
3 UVM_INFO svt_dp_tx.sv(2321) @ 1285083.881ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=7d3cbc22 for line=2
  in frame=4, ae_pix_crc_prev_valid=1, ae_pix_crc_prev=655db79b
4 UVM_INFO svt_dp_tx.sv(2321) @ 1316857.337ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=e8188d48 for line=3
  in frame=4, ae_pix_crc_prev_valid=1, ae_pix_crc_prev=7d3cbc22
5 UVM_INFO svt_dp_tx.sv(2321) @ 1348630.793ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=82e971d0 for line=4
  in frame=4, ae_pix_crc_prev_valid=1, ae_pix_crc_prev=e8188d48
6 UVM_INFO svt_dp_tx.sv(2321) @ 1380404.249ns: uvm_test_top.env.source_agent.driver [drive_frames] :AE_SRC_DBG :: pix_crc=7939c234 for line=5
  in frame=4, ae_pix_crc_prev_valid=1, ae_pix_crc_prev=82e971d0
```

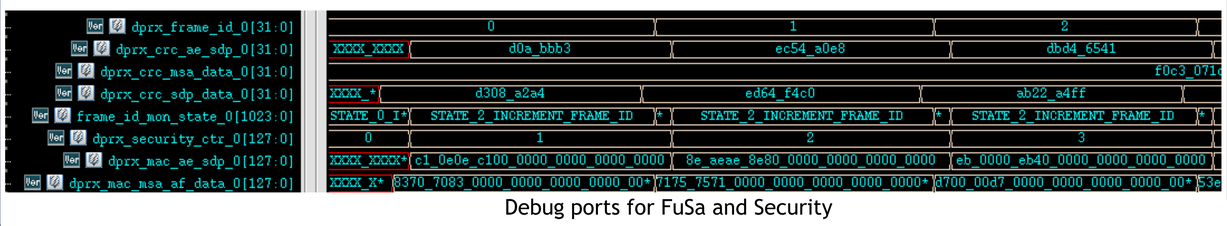
Detailed debug messages from DP AE Source

```
1 UVM_INFO svt_dp_rx.sv(22202) @ 1253333.848ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 4, Active line 0,
  Frame 4, dprx_crc_pixels[0] = 0x73ad1b62
2 UVM_INFO svt_dp_rx.sv(22202) @ 1285107.304ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 5, Active line 1,
  Frame 4, dprx_crc_pixels[0] = 0x655db79b
3 UVM_INFO svt_dp_rx.sv(22202) @ 1316880.760ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 6, Active line 2,
  Frame 4, dprx_crc_pixels[0] = 0x7d3cbc22
4 UVM_INFO svt_dp_rx.sv(22202) @ 1348654.216ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 7, Active line 3,
  Frame 4, dprx_crc_pixels[0] = 0xe8188d48
5 UVM_INFO svt_dp_rx.sv(22202) @ 1380427.672ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 8, Active line 4,
  Frame 4, dprx_crc_pixels[0] = 0x82e971d0
6 UVM_INFO svt_dp_rx.sv(22198) @ 1412201.128ns: uvm_test_top.env.sink_agent.monitor [calculate_crc_pixels] Stream_0:Line 9, Active line 5,
  Frame 4, Final dprx_crc_pixels[0] = 0x7939c234
```

Detailed debug messages from DP AE Sink

```
AE SDP for Frame = 5 at timestamp = 2821878.474000 ns
DB   0  |  7:0  |  IEEE OUI First Byte   | 3a
DB   1  |  7:0  |  IEEE OUI Second Byte  | 2
DB   2  |  7:0  |  IEEE OUI Third Byte   | 92
DB   3  |  7:0  |  VESA TYPE LSB         | 1
DB   4  |  7:0  |  VESA TYPE MSB         | 0
DB   5  |  7:0  |  LENGTH LSB            | 21
DB   6  |  7:0  |  LENGTH MSB            | 0
DB   7  |  1:0  |  SUBFRAME ID           | 0
        |  7:2  |  RESERVED              | 0
DB   8  |  0    |  FUSA COMPARE          | 1
        |  7:1  |  RESERVED              | 0
DB   9  |  7:0  |  FRAME ID [7:0]        | 1
DB  10  |  7:0  |  FRAME ID [15:8]       | 0
DB  11  |  7:0  |  FRAME ID [23:16]      | 0
DB  12  |  7:0  |  FRAME ID [31:24]      | 0
DB  13  |  7:0  |  CRC MSA [7:0]         | ac
DB  14  |  7:0  |  CRC MSA [15:8]        | 4
DB  15  |  7:0  |  CRC MSA [23:16]       | 17
DB  16  |  7:0  |  CRC MSA [31:24]       | 47
DB  17  |  7:0  |  CRC SDP [7:0]         | 9a
DB  18  |  7:0  |  CRC SDP [15:8]        | d1
DB  19  |  7:0  |  CRC SDP [23:16]       | ef
DB  20  |  7:0  |  CRC SDP [31:24]       | 7d
DB  21  |  7:0  |  CRC COMP [7:0]        | 0
DB  22  |  7:0  |  CRC COMP [15:8]       | 0
DB  23  |  7:0  |  CRC COMP [23:16]      | 0
DB  24  |  7:0  |  CRC COMP [31:24]      | 0
DB  25  |  7:0  |  ROI MASK [7:0]        | 0
DB  26  |  7:0  |  ROI MASK [15:8]       | 0
DB  27  |  7:0  |  RESERVED              | 0
DB  28  |  7:0  |  RESERVED              | 0
DB  29  |  7:0  |  RESERVED              | 0
DB  30  |  7:0  |  RESERVED              | 0
DB  31  |  7:0  |  RESERVED              | 0
DB  32  |  7:0  |  CRC PIX [7:0]         | 59
DB  33  |  7:0  |  CRC PIX [15:8]        | 9b
DB  34  |  7:0  |  CRC PIX [23:16]       | ab
DB  35  |  7:0  |  CRC PIX [31:24]       | c
DB  36  |  7:0  |  AE SDP CRC [7:0]      | 11
DB  37  |  7:0  |  AE SDP CRC [15:8]     | e1
DB  38  |  7:0  |  AE SDP CRC [23:16]    | 23
DB  39  |  7:0  |  AE SDP CRC [31:24]    | 28
-----------------------------------------
```

Trace file for AE_SDP packet



Debug ports for FuSa and Security

Conclusion

- ✓ Showcased a systematic approach to **develop a DP AE testbench by enhancing the existing DP testbench.**
- ✓ Demonstrated various strategies to **accelerate the simulation.**
- ✓ The advanced debugging capabilities helped us focus on the real aim of **"unearthing critical bugs in the design that could compromise safety and security."**
- ✓ The run time switches used in the scenario generation helped us achieve **faster coverage closure** which led to **early closure of the DP AE verification activity.**

Configuration	Simulation Time(Config disabled)	Simulation Time(Config enabled)	Gain
Scaled down frame	16797s	553s	96%
Bypass initialization and standard procedures	487s	425s	12%

Performance improving configurations

REFERENCES

[1]www.vesa.org, "VESA DisplayPort (DP) Automotive Extension Services," Version 1.0, July 24, 2025

[2]www.vesa.org, "VESA DisplayPort (DP) Standard", Version 2.1a, 18 December 2023.

[3]www.vesa.org, "VESA Embedded DisplayPort (eDP) Standard", Version 1.5a, February 27, 2023.