Beyond Traditional Testing: Integrating DV and DFT for Zero-Defect Goals

Jyothy Jaganathan
Ann Keffer

Problem Statement/Introduction

The semiconductor industry faces increasing pressure to achieve over 99% defect coverage and meet stringent low DPPM targets, especially in critical sectors like automotive and data centers. Traditional ATPG methods often miss faults in complex designs, making fault grading essential to complement structural testing and ensure comprehensive coverage and compliance with safety standards.

Question	If Yes → Consider Fault Grading
Is ATPG coverage below target?	☑
Are functional patterns already available?	☑
Is the design complex or hierarchical?	☑
Are you targeting low DPM or high quality?	☑
Do you have scan-excluded or graybox IPs?	☑
Are you seeing fault escapes in silicon?	☑

Proposed Methodology/Advantages

Simulation-based fault grading is ideal when functional patterns are already part of the validation flow. Choose a fault simulator that:

Supports Verilog, System Verilog, and UVM testbenches.

Compatible with multiple waveform formats for easy integration.

Handles a wide range of fault models (stuck-at, delay, cell-aware).

Aligns fault models with design type, technology node, and test goals.

Improves fault grading accuracy and DFT effectiveness.

Example Sims	Type	TB
Chain Integrity	Blk	Serial
SSN Loop back	Blk	Serial
Tap Controller	Top	Serial
SSN Integrity graybox	Top	Serial
IJTAG Integrity graybox	Top	Serial

Simulation-based fault grading is ideal when functional patterns are already part of the flow. It uses functional verification stimuli to detect faults missed by ATPG, especially in non-capture logic and graybox IPs, though it can be time-consuming for large designs.

Implementation Details/Diagram

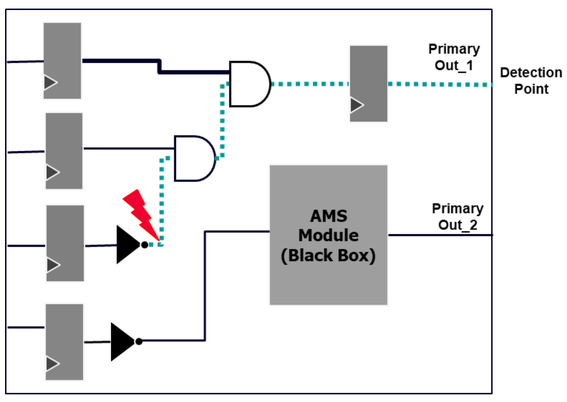
Fault Injection Example: A fault (e.g., stuck-at-0/1) between logic gates is detectable only if it is activated and propagated to an observable output

AMS Challenge: Analog/mixed-signal blocks (black box) are not directly testable via digital ATPG tools.

Coverage Strategy:

- Use surrounding digital logic or specialized mixed-signal tests
- Apply functional fault grading to identify faults covered by functional patterns

Goal: Close coverage gaps and enhance overall test quality

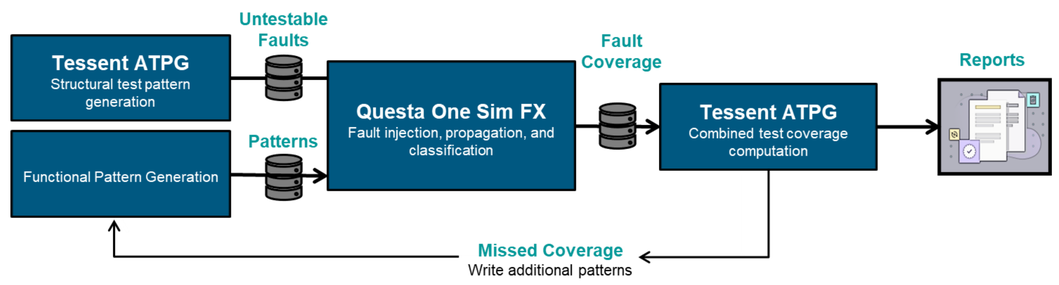


Implementation Details/Flow Chart

The methodology for the experiment uses Siemens' integrated toolchain, combining Tessent TestKompress, Questa One Sim, and Questa One Sim FX. The flow is shown in figure 9.

The flow in summary is:

1. ***Tessent ATPG*** generates structural patterns
2. ***Questa One Sim*** generates functional patterns and grades stimulus for controllability
3. ***Questa One Sim FX*** performs functional fault grading and provides defect coverage report
4. ***Tessent ATPG*** merges structural and functional coverage reports



Results Table

Fault Classes	Result after normal ATPG run		Results after merging the functional fault grading results	
	#faults(total)	#faults(total relevant)	#faults(total)	#faults(total relevant)
FU (full)	298702	294271	298702	297332
UC (uncontrolled)	81 (0.03%)	same (0.03%)	40 (0.01%)	same (0.01%)
UO (unobserved)	19 (0.01%)	same (0.01%)	17 (0.01%)	same (0.01%)
DS (det_simulation)	224897 (75.29%)	same (76.43%)	224897 (75.29%)	same (75.64%)
DI (det_implication)	62081 (20.78%)	same (21.10%)	64470 (21.58%)	same (21.68%)
PU (posdet_untestable)	5 (0.00%)	same (0.00%)	4 (0.00%)	same (0.00%)
UU (unused)	4004 (1.34%)	same (1.36%)	3931 (1.32%)	same (1.32%)
TI (tied)	368 (0.12%)	same (0.13%)	365 (0.12%)	same (0.12%)
BL (blocked)	82 (0.03%)	same (0.03%)	74 (0.02%)	same (0.02%)
RE (redundant)	1348 (0.45%)	same (0.46%)	1348 (0.45%)	same (0.45%)
AU (atpg_untestable)	5817 (1.95%)	1386 (0.47%)	2638 (0.88%)	1268 (0.43%)
test_coverage	97.98%	99.48%	98.92%	99.39%
fault_coverage	96.08%	97.52%	97.03%	97.48%

When applied fault grading results, a 0.94% and 0.95% improvement in test_coverage and fault_coverage was be observed.

Conclusion

Fault grading is a critical component of DFT as it directly measures test quality through fault coverage, identifies gaps in test patterns, and guides improvements in scan architecture and logic design. By enhancing fault detection capabilities, it supports higher product reliability and yield, ultimately ensuring robust and efficient manufacturing outcomes.

REFERENCES

1. S. Praveen, Siva Yellampalli, Ashish Kothari, “Optimization of Test Time and Fault Grading of Functional Test Vectors using Fault Simulation Flow,” 2014 International Conference on Electronics, Communication and Computational Engineering (ICECCE)