2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

SYNOPSYS®

Novel Approach to Verification and Validation for Multi-die Systems

Dr. Tim Kogel
Sr. Director, Technical Product Management
Oct 2024

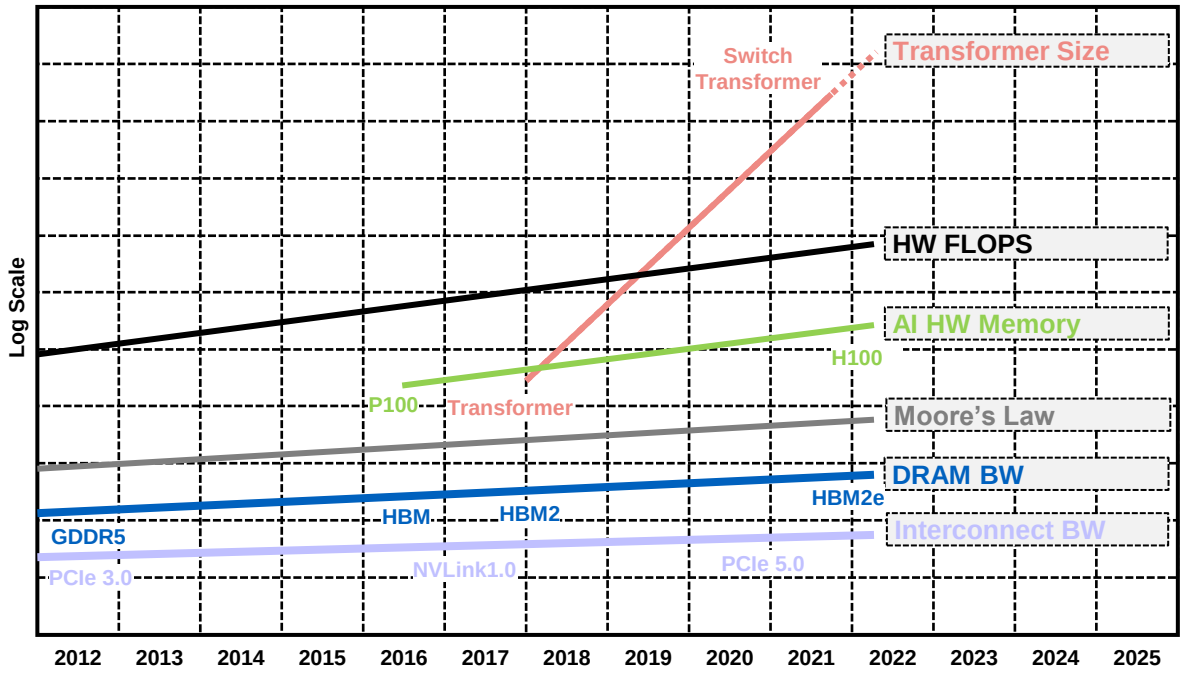
Agenda

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

- Multi-die market trends and challenges
- Multi-die architecture performance and power validation
- Functional verification of multi-die designs
- Multi-Die physical validation and optimization
- Summary

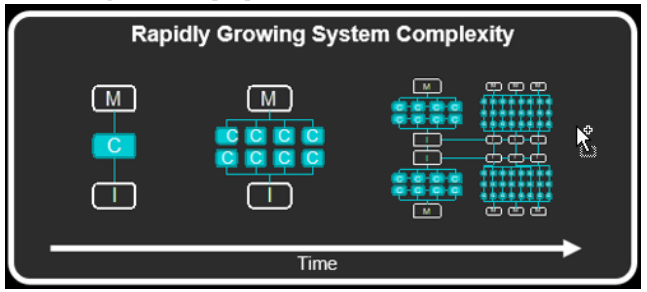
AI Drives New Design Paradigms

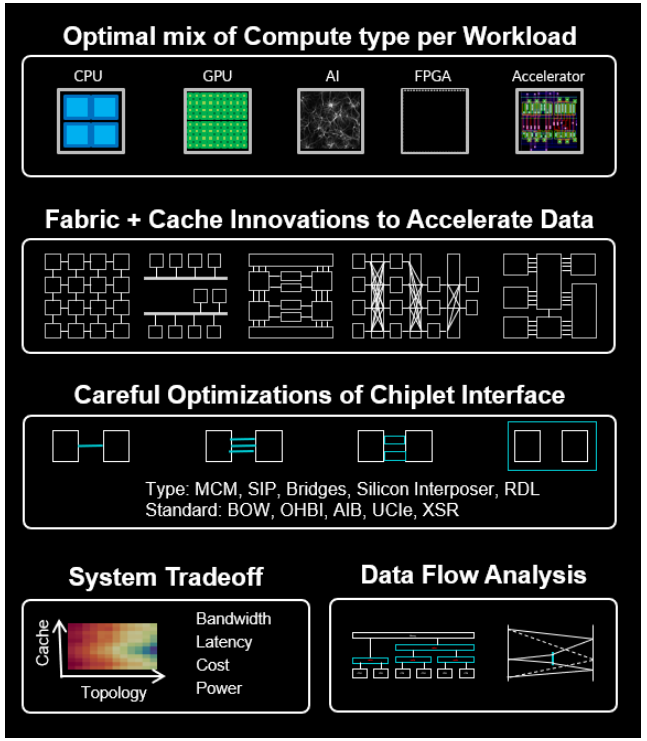
The need for hardware scaling leads to new architectures and design approaches



Transformer Size: 410x / 2yrs
HW FLOPS: 3.0x / 2 yrs
AI HW Memory: 2x /2 yrs
Moore's Law: 2x / 2 yrs
DRAM Bandwidth: 1.6x / 2 yrs
Interconnect Bandwidth: 1.4x / 2 yrs

Wide range of optimizations & innovations





Source: AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems @ EETimes Chiplet Summit

Use Cases for the Era of Pervasive Intelligence

From **Silicon IP** to **System HW** for AI Inference & Training running **SW**

Early Performance and Power Analysis

Early Software Bring-up, Hardware/Software Validation

Functional Verification, RTL Regressions

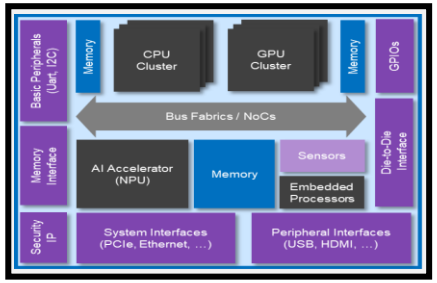
IP in System Validation, Performance Validation, Compliance

Workloads

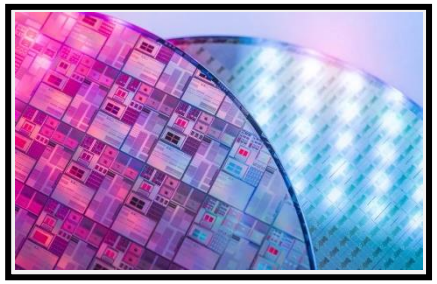
- Applications
- Middleware
- Operating System
- Firmware

Silicon IP / Blocks

Architecture



Silicon



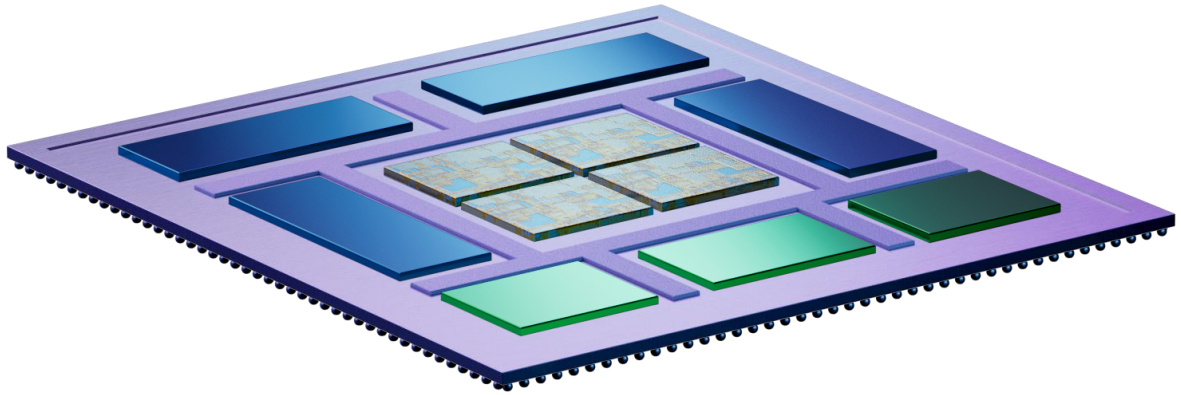
Multi-Die Package

System

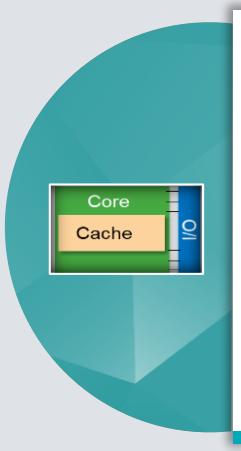
Safety, Reliability, Security, Design for Test, Sign-off, Silicon Lifecycle Management

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

Multi-Die Design in the Era of Pervasive Intelligence

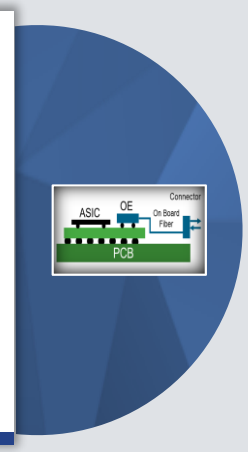


Expanding Use Cases Across Market Verticals



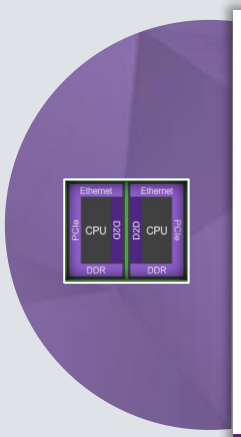
Disaggregate

Disaggregate a SOC to IO or Cache dies for better yield and cost



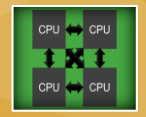
Aggregate

Aggregate multiple functions at optimized nodes and form factor



Split

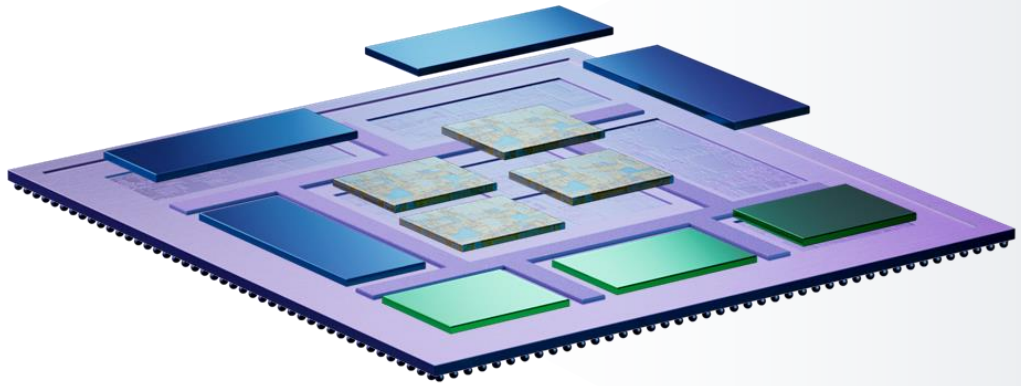
Split a die to overcome reticle size limit and create a bigger capacity system



Scale-Up

Scale up processor/ accelerator by adding tightly coupled die fabric (clusters)

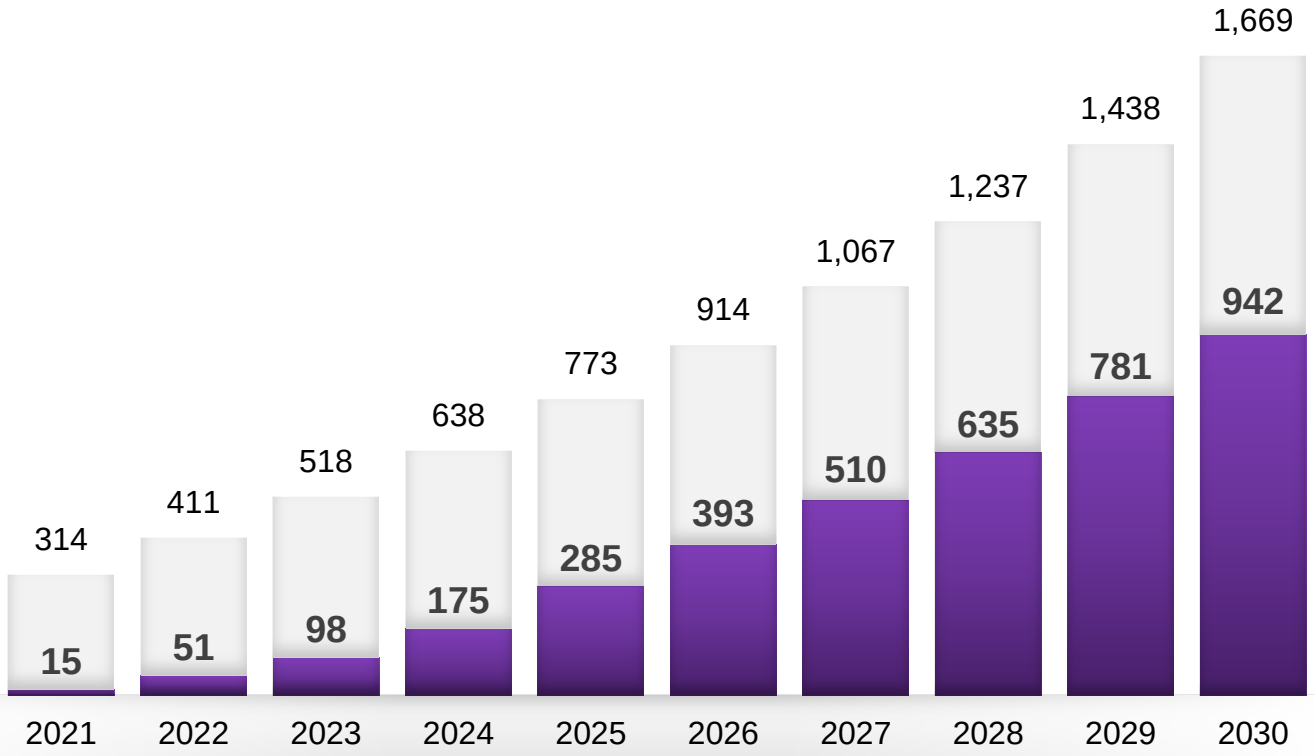
The Shift to Multi-Die Design



Motivation

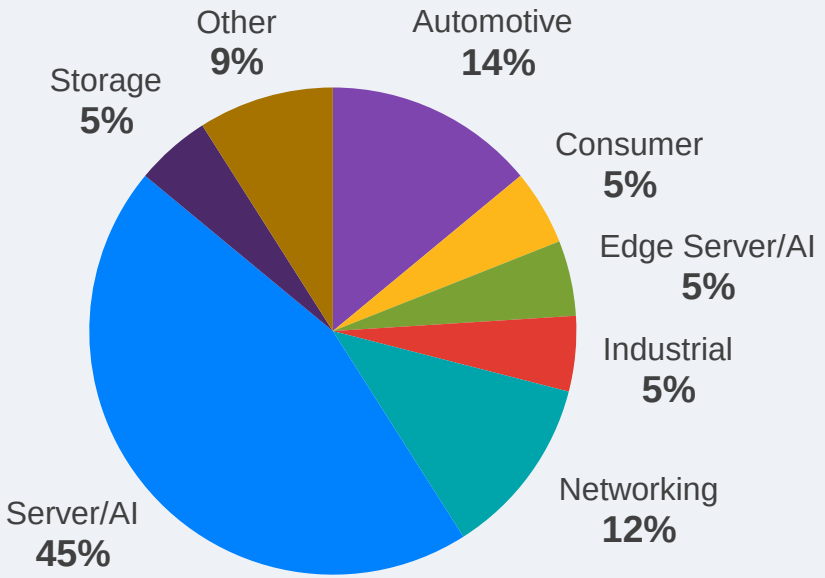
- Accelerated scaling of system functionality at a cost-effective price
- Reduced risk & time-to-market by re-using proven designs/die
- Lower system power while increasing throughput
- Rapid creation of new product variants for flexible portfolio management

Multi-Die Design Adoption is Growing



Source: IBS Semiconductor Industry Outlook May 2023

Multi-Die Designs by Application



Source: Synopsys

Chiplets Design

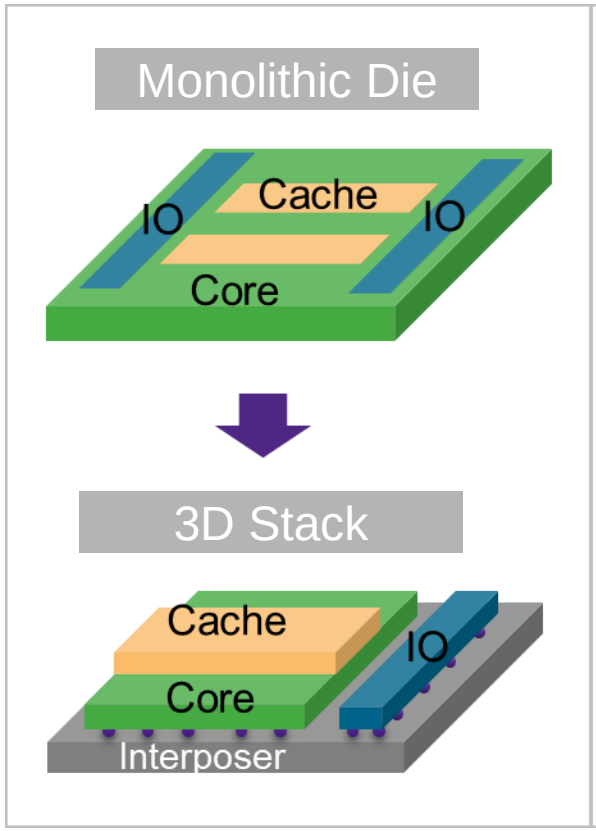
Cost Analysis Example: Disaggregated Silicon

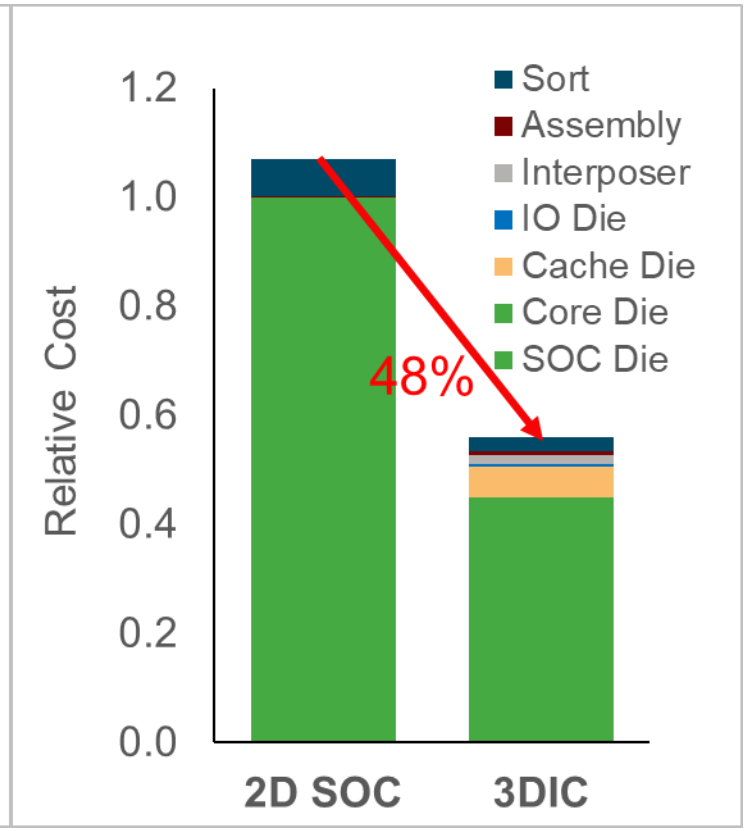
2DIC

Monolithic	Tech Node	Area
SOC	2nm GAA 17ML	6.0 cm^2
- Core	Same	51%
- Cache	Same	34%
- IO	Same	15%

3DIC

3D Chiplet	Node	Intercon.	Area
Core + L1-2	2nm GAA 17ML	TSV + mbumps	3.88 cm^2
L3 Cache	2nm GAA 4ML	Direct bonding	1.22 cm^2
IO	90nm planar 7ML	mbumps	1.17 cm^2
Silicon interposer		6ML + TSV + mbumps	6.84 cm^2





- 3DIC lowers the cost by 48%, thanks to a) better yield due to smaller die size; b) simpler BEOL for L3 cache chiplet; and c) mature and cheaper node for IO.
- They offset added cost due to sort and assembly and interposer.

Heterogeneous Integration Enabled by the State-of-the-Art 3DIC and CMOS Technologies: Design, Cost, and Modeling

X.-W. Lin[1], V. Moroz[1], X. Xu[1], Y. Gao[1], D. Rennie[2], P. Asenov[3], S. Smidstrup[4], D. Sherlekar[1], Z. Qin[1], T. Fang[5], J. Lee[3], M. Choi[1], and S. Jones[6]

Multi-Die is Enabling Truly Transformative Products

Commercial examples

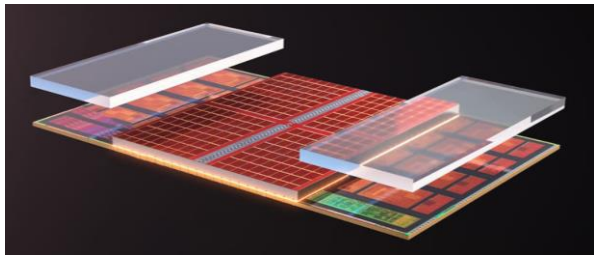
Disaggregate

Aggregate

Split

Scale-Up

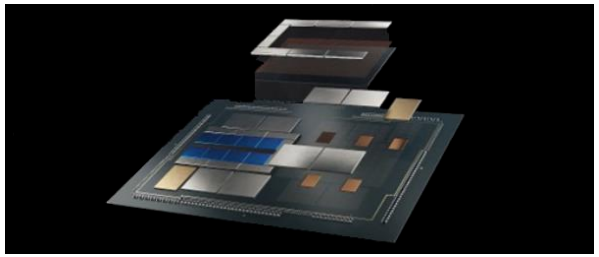
AMD



3D V-Cache: Hybrid Bonded

3x Energy Efficiency, 15x Interconnect Density (v. µbumps)

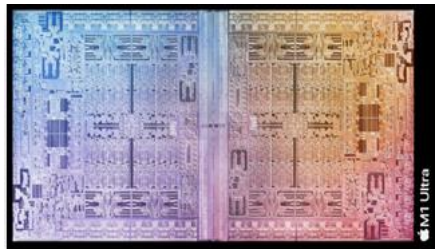
Intel



Exascale Computing / AI

100B+ Tr's, 47 Active Tiles, 5 Process Nodes, EMIB/Foveros

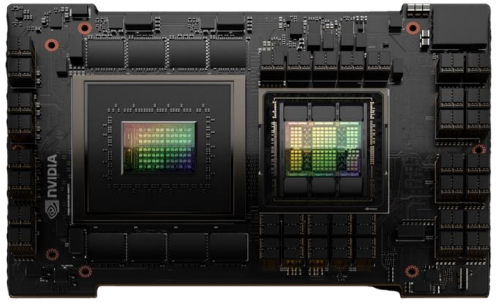
Apple



Personal Computing

2x Dies, 114B Transistors, 2.5TB/s D2D BW, Silicon Connected

Nvidia



Superchip: Gen AI Computing

2x Dies, 200B+ Transistors, 3.2TB/s Fabric

Multi-Die Interface Standardization

Technical Merits, Maturity & Strength of Ecosystem are Key for Success

Alliance	OIF	OPEN Compute Project®		CHIPS ALLIANCE	UCIe Universal Chiplet Interconnect Express
Standard	**XSR**	**BOW**	**OHBI**	**AIB**	**UCIe**
Data Rate	112G / 224G	8G / 16G	8G / 16G	6G	16G / 32G
Protocol	Not Defined	Not Defined	Not Defined	Not Defined	Streaming, PCIe, CXL
Package Focus	2D	2D (2.5D also supported)	2.5D (2D also supported)	2.5D	2D, 2.5D, 3D
Target Applications	Optical Networking (CPO/NPO)	Cost sensitive aggregation	High density scale for data center	Mil-aero ecosystem	Scale & Split w/ streaming Aggregation w/ PCIe/CXL

Why is UCIe a Preferred D2D Interface?

Technical Merits, Comprehensive Spec & Broad Eco-System

- Technical Merits (Most compelling PPAs)
  - Energy efficiency <0.3pJ/Bit
  - Edge efficiency >5Tbps/mm
  - Latency ~2ns from FDI to FDI
- Comprehensive & Futureproof
  - All use cases
  - All package types
  - Chip to Chip use case with retimer
  - Complete protocol stack
  - Future proof with support up to 32Gbps data rate per pin
- Broad Ecosystem
  - Wide range of promoters & contributors spanning all industry segments

> 110 members (June 2023)

The First UCIe Test Chips for the Chiplet Era

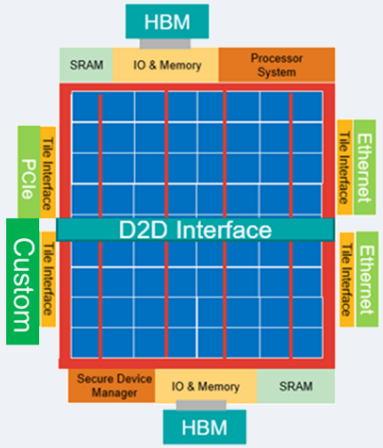
> TSMC, Synopsys, and Intel Foundry Pike Creek—the first test chips for UCIe and **the beginning of the chiplet era**.

Pat Gelsinger, CEO
Keynote at Intel Innovation 2023

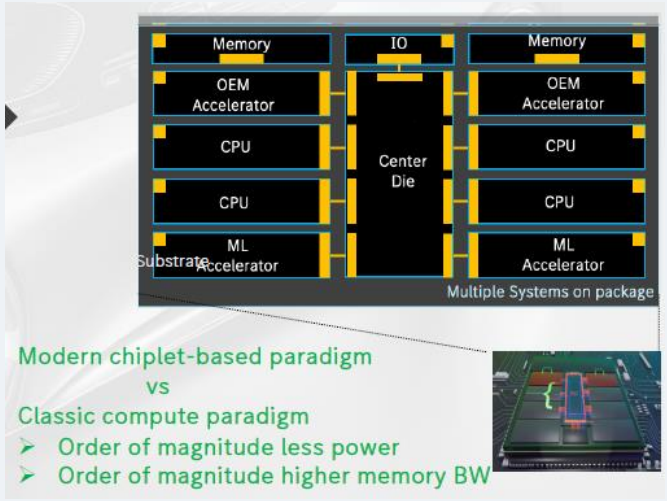
Enabling the Multi-Die Ecosystem

Specialization with domain-specific accelerator chiplets

"Data Driven Design for Adaptive Multi-Die Designs"
Vikrant Kapila, Principal Engineer & Director, Altera
SNUG Silicon Valley, 2024, slides

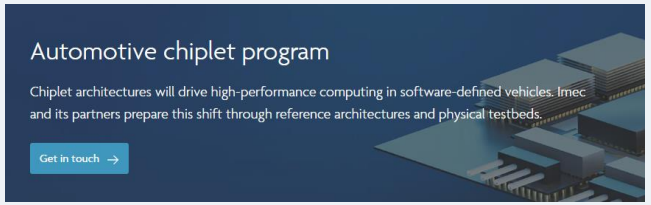


"Standardization for Automotive Computing HW"
François Piednoël, Distinguished Architect, MBZ
Automotive Compute Conference, US, 2024



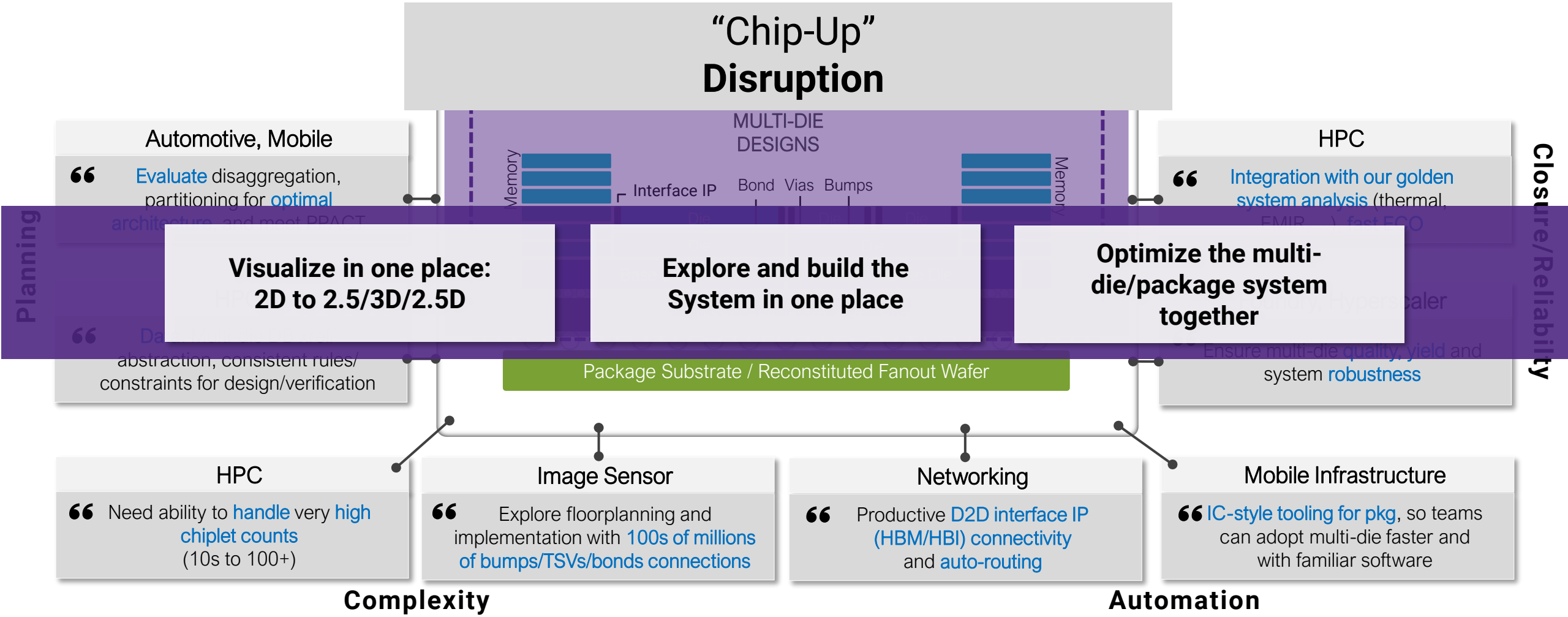
"Standardization could open door to 3rd-party chiplets"
AMD's CTO Mark Papermaster
and SVP Sam Naffziger
https://www.theregister.com/2024/03/27/amd_chiplets_future

IMEC's "Automotive Chiplet Program", link



- Baseline compute, memory, and IO dies with standard multi-die interface
- Custom companion chiplets with access to memory infrastructure
- Architecture challenges:
  - Workload partitioning & mapping
  - Interconnect/memory fabric dimensioning
  - End-to-end performance, power, and thermal analysis
  - Physical design planning

Multi-Die Design: A Wide Range of Needs



Multi-Die Validation and Verification Challenges

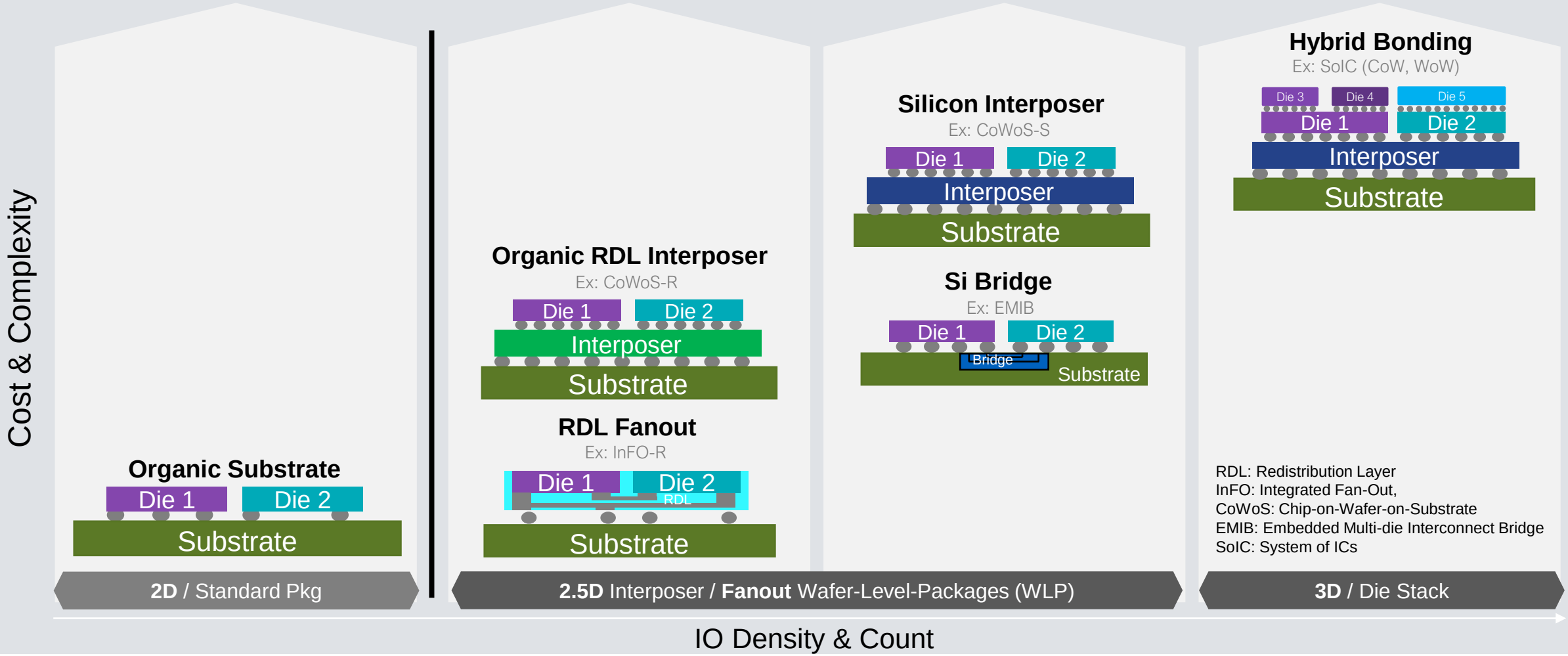
- System verification must validate assumptions made during architecture design
  - Must consider die-to-die communication: delay, jitter, coherency, power, guaranteed delivery and errors
    - Monolithic SoCs only consider delay
- Design size and complexity exacerbate Verification
  - Need adequate levels of capacity and performance
    - Hybrid models and traffic generators to focus on a few dies at a time
    - Very large memories bottlenecks
  - Scalability of simulation/emulation models
    - Include analog components
  - Scalable system integration methodology (system aggregation)
- Knowing when Verification is complete
  - Exhaustive verification of individual dies – Complete functional coverage (UVM)
    - Die-level bugs cannot be fixed at the system level

Agenda

- Multi-die market trends and challenges
- Multi-die architecture performance and power validation
- Functional verification of multi-die designs
- Multi-Die physical architecture validation, optimization, and sign-off
- Summary

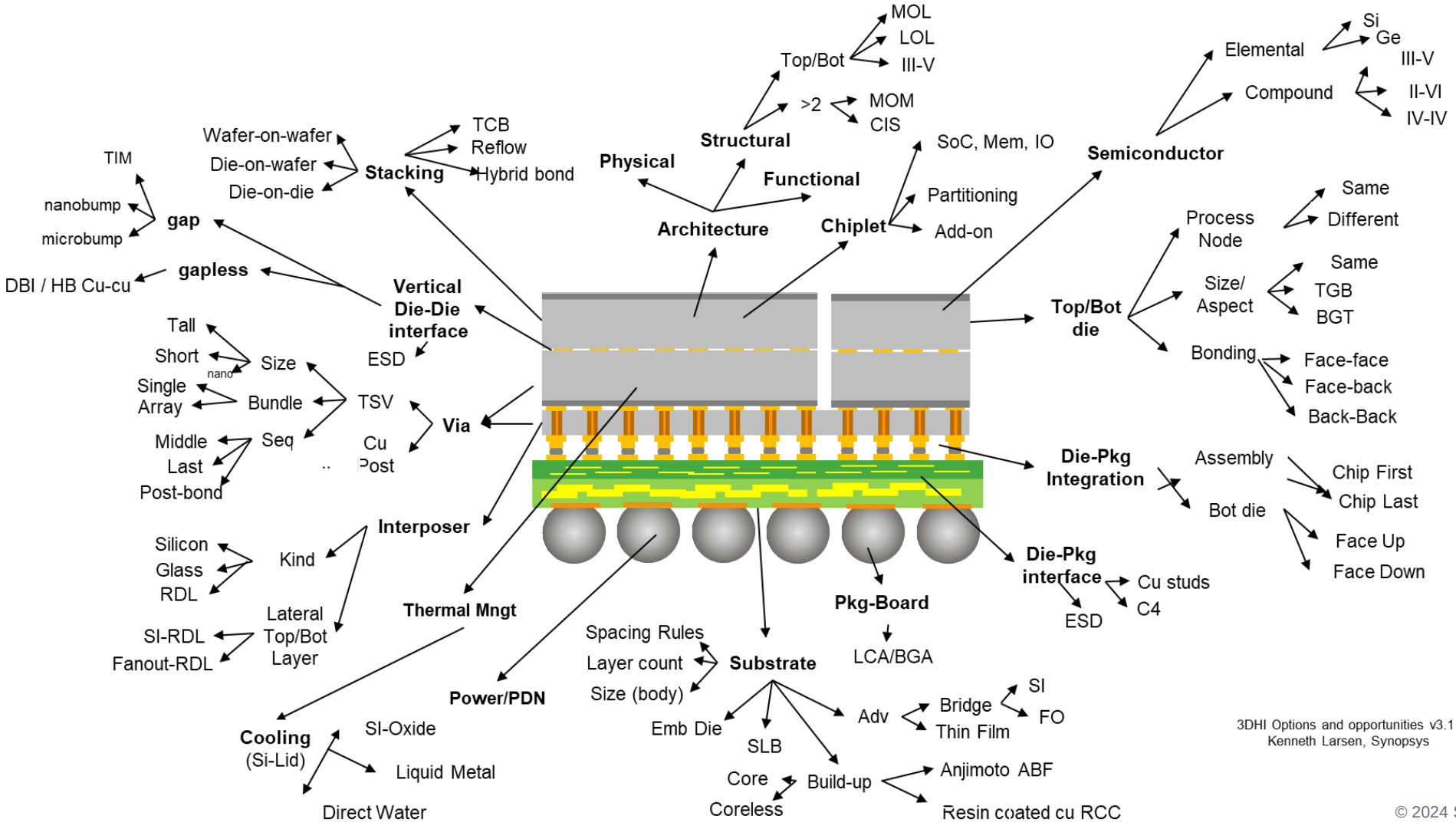
System Integration: Already a Multitude of Options

Driven by power, performance, function, cost, thermal



Choices Influencing PPA/mm3

Bandwidth, performance, power, latency, cost, and schedules



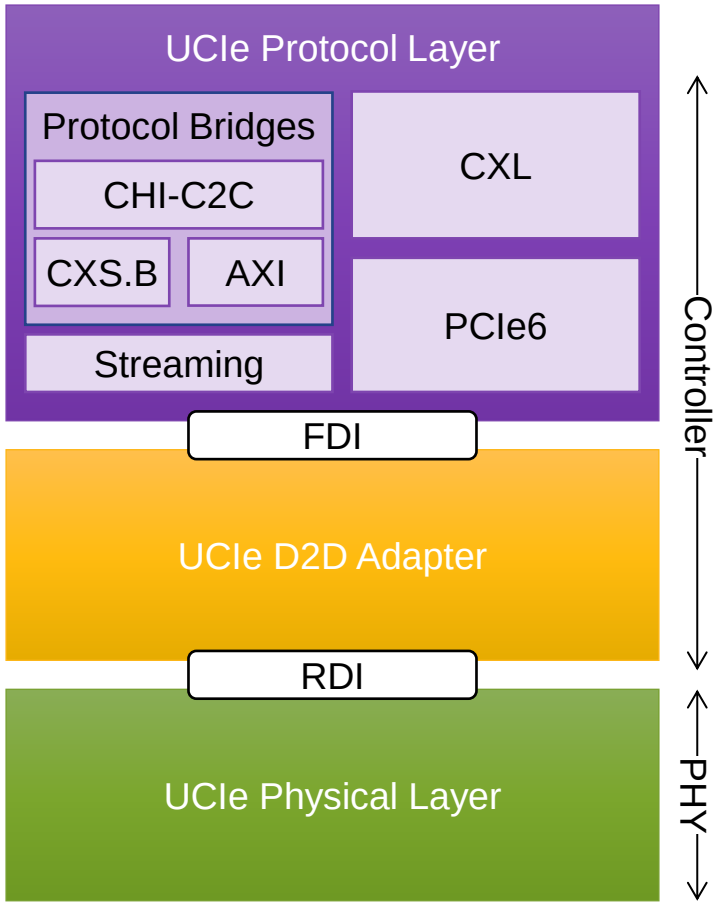
3DHI Options and opportunities v3.1
Kenneth Larsen, Synopsys

UCIe is De Facto Standard for Multi-Die Designs

Lightweight die-to-die interface for all use cases

Characteristics / KPIs	Standard Package	Advanced Package
Data Rate (GT/s)	4, 8, 12, 16, 24, 32	
Width (each cluster)	16	64
Bump Pitch (um)	100 – 130	25 - 55
Channel Reach (mm)	<= 25	<=2
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317
B/W Density (GB/s/mm^2)	22-125	188-1350
Power Efficiency target (pJ/b)	0.5	0.25

Universal Chiplet Interconnect Express (UCIe)™ Whitepaper: Building an Open Chiplet Ecosystem

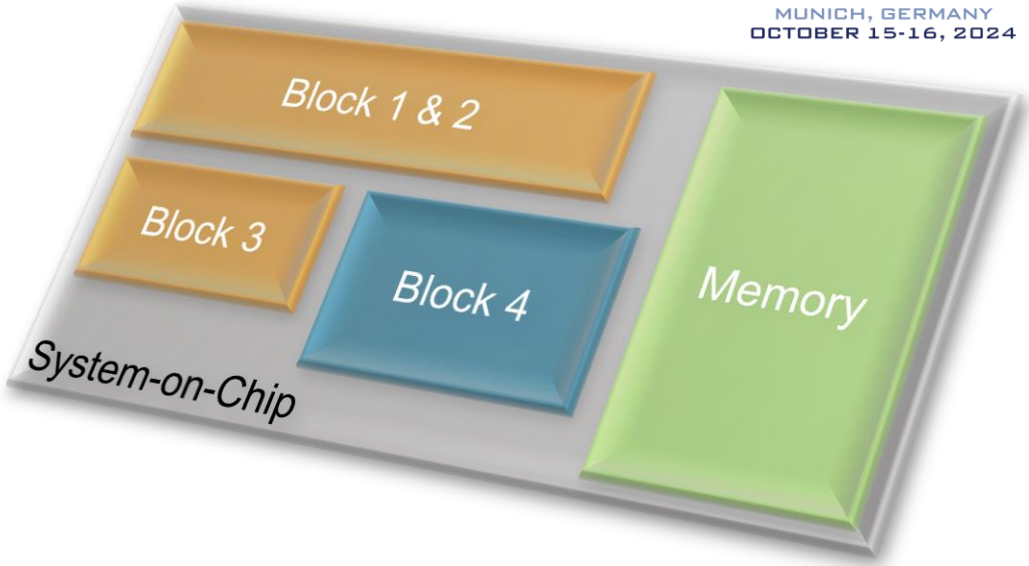


FDI = FLIT-aware Die-to-die Interface
RDI = Raw-data Die-to-die Interface

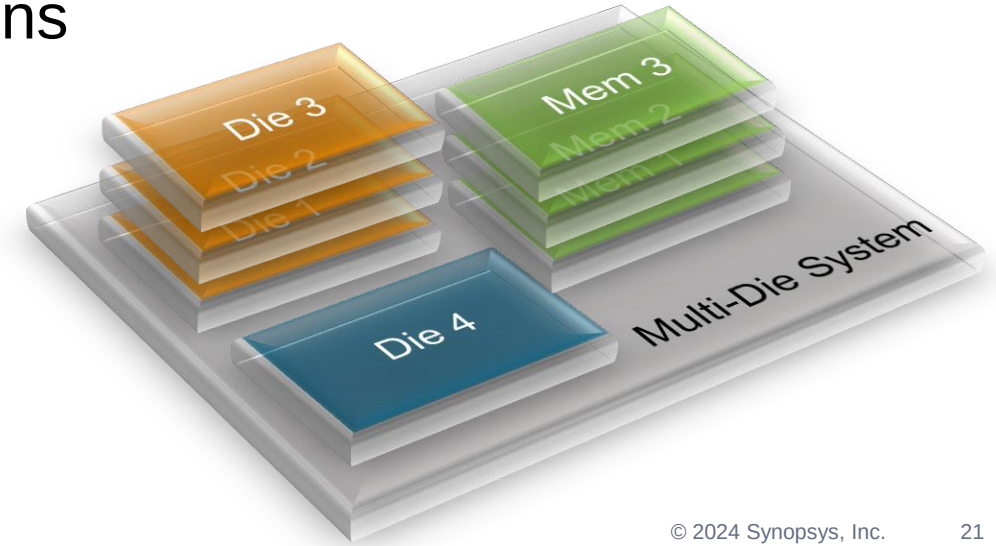
- Supports variety of different use cases and on-chip fabrics
  - Streaming for latency optimized and for proprietary implementations
  - AXI, CXS.B, and CHI-C2C for seamless multi-die disaggregation of on-chip interconnects
  - Coherent multi-die aggregation with CXL in compute & memory expansion use cases
  - Non-coherent multi-die aggregation with PCIe for latency insensitive use cases

New Dimensions in Architecture Exploration

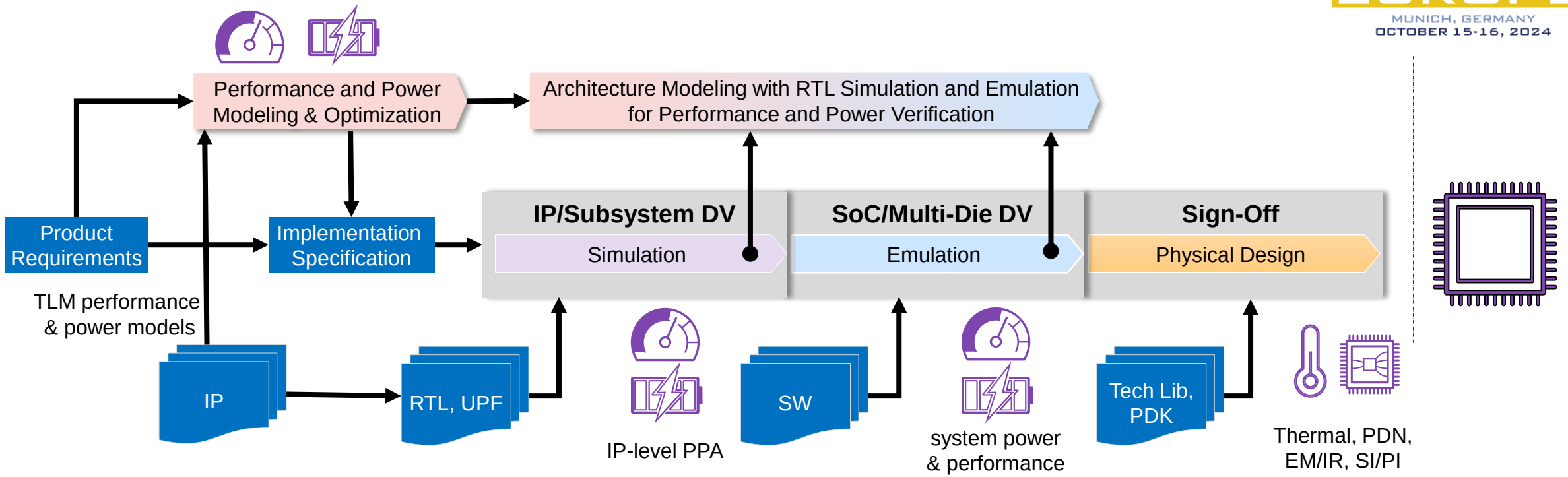
- SoC-level macro-architecture decisions
  - HW/SW partitioning
  - IP selection, configuration, and connectivity
  - Interconnect/memory dimensioning
  - System-level power analysis



- Additional multi-die macro-architecture decisions
  - Aggregation: assemble multi-die system from chiplets
  - Disaggregation: partitioning into multiple chiplets
  - Dimensioning of die-to-die interfaces
  - Selection of technologies for each chiplet
  - Selection of packaging technology



Semiconductor Design and Verification Flow



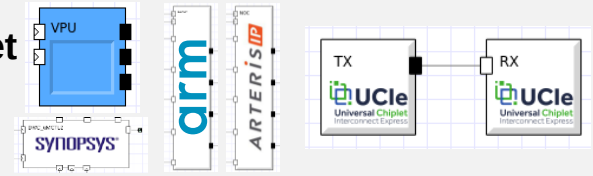
- **Goal:** design the right product, de-risk architecture, translate product requirements into implementation specification, track requirements
- **Use cases:** data-driven performance and power analysis, HW/SW partitioning, interconnect/memory dimensioning, iterative architecture optimization

Early Architecture Exploration of Multi-Die Designs

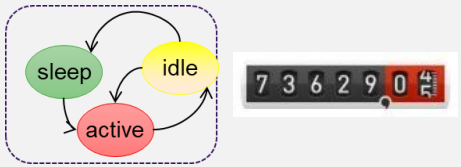
Platform Architect for Multi-Die

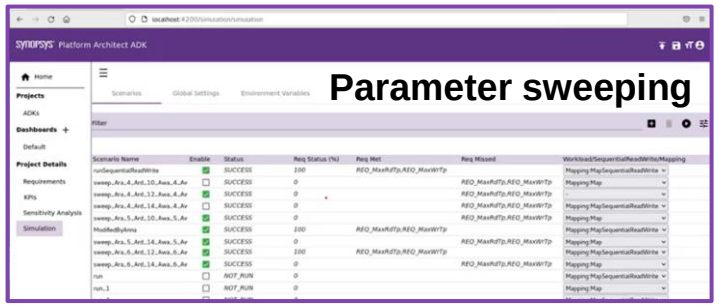
Application specification and requirements

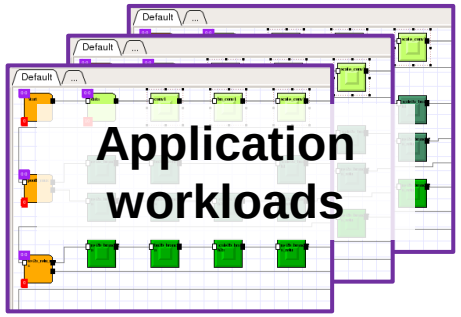
HW & chiplet model libraries



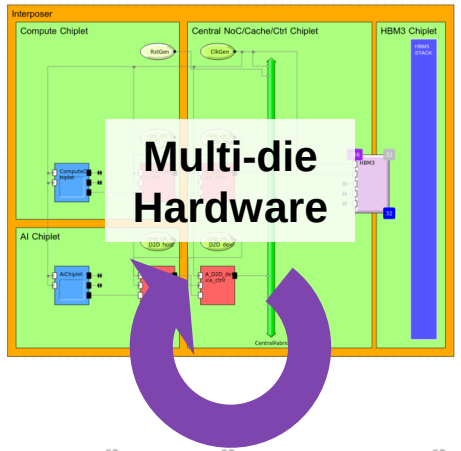
Power models and characterization



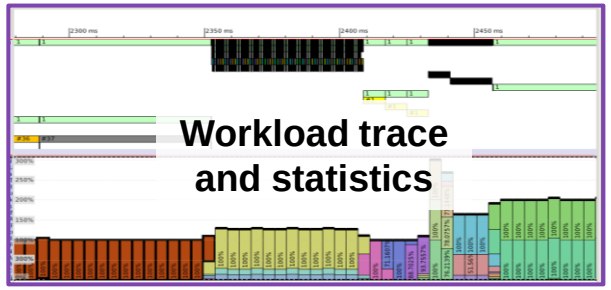


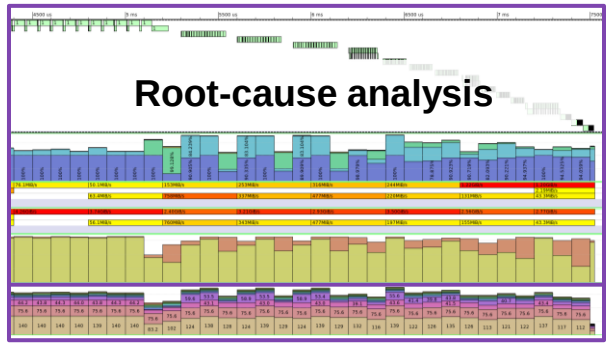


map



Design space exploration and collaboration



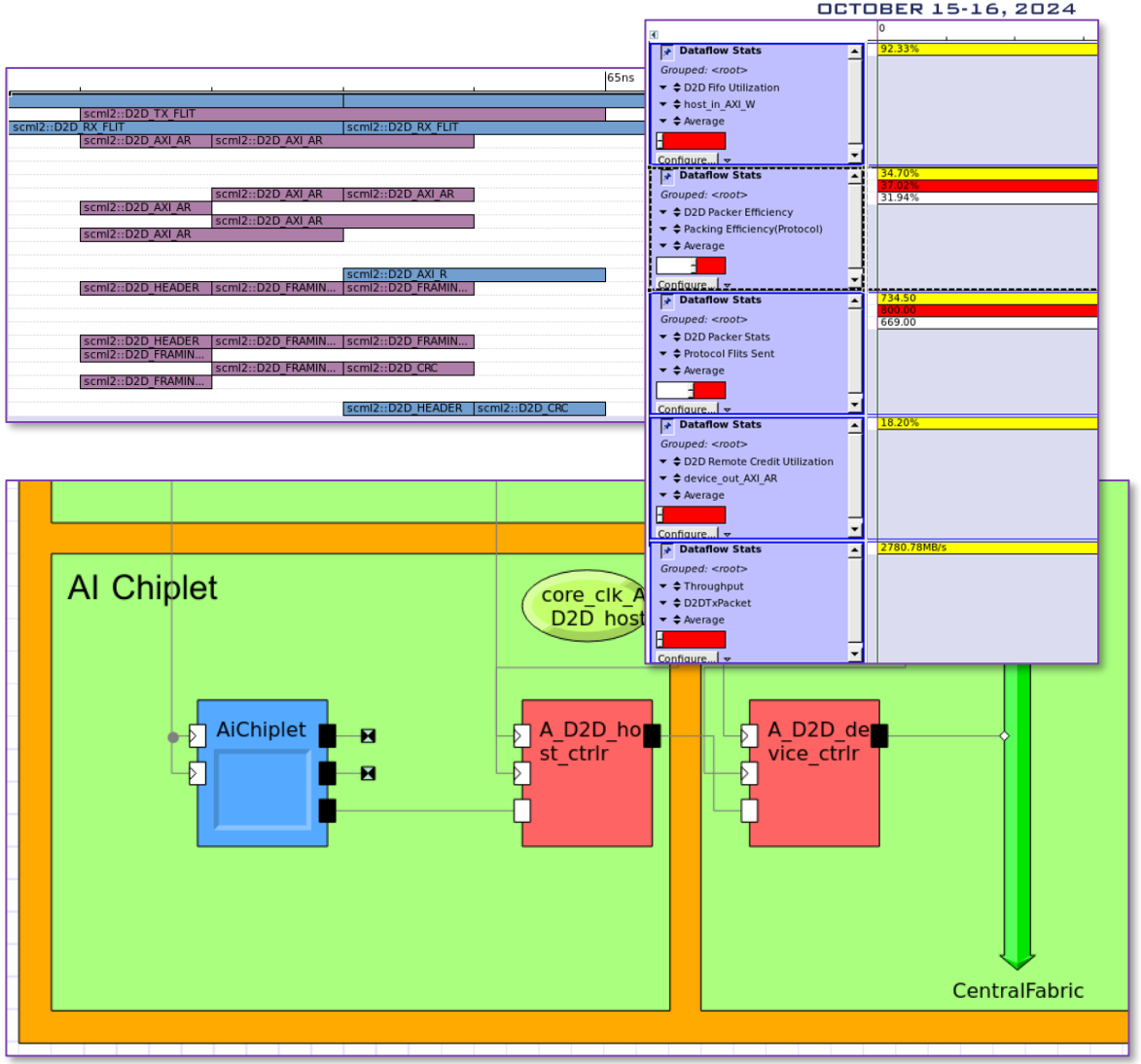


Generic Die-to-Die (D2D) Controller

Overview

Configurable generic model to mimic architecture and timing of D2D interfaces

- Application protocols: AXI, CHI
- Die-to-die protocols
  - UCIe protocol and configuration
  - Additional D2D protocols can be customized
- One pair of d2d host and device ctrlr represents
  - D2D controller and core
  - PHY(s) – one per module
  - Protocol bridge (AXI)
- Highly configurable for performance exploration
- Trace-based and statistical analysis
- Starting point example platform for AXI over UCIe

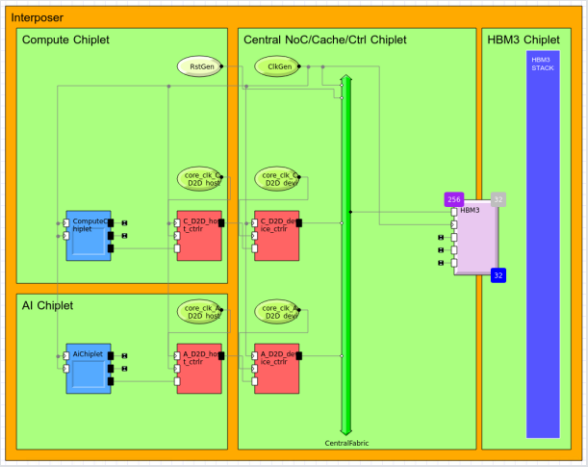


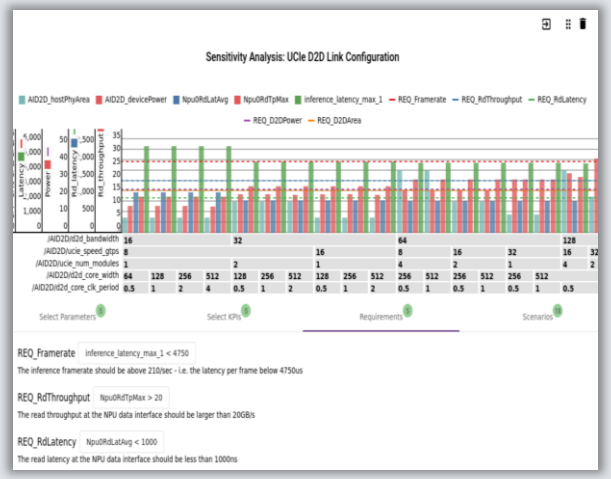
Case Study

Multi-die performance/power analysis of AI workload

- Goals/requirements:
  - Framerate 210Hz / 4.75ms inference latency per frame
  - minimize power and energy

- Optimize hardware configuration:
  - UCIe chip-to-chip interface
  - Local memory of AI chiplet (NPX6-64K)
  - Interconnect, buffers, credits, …

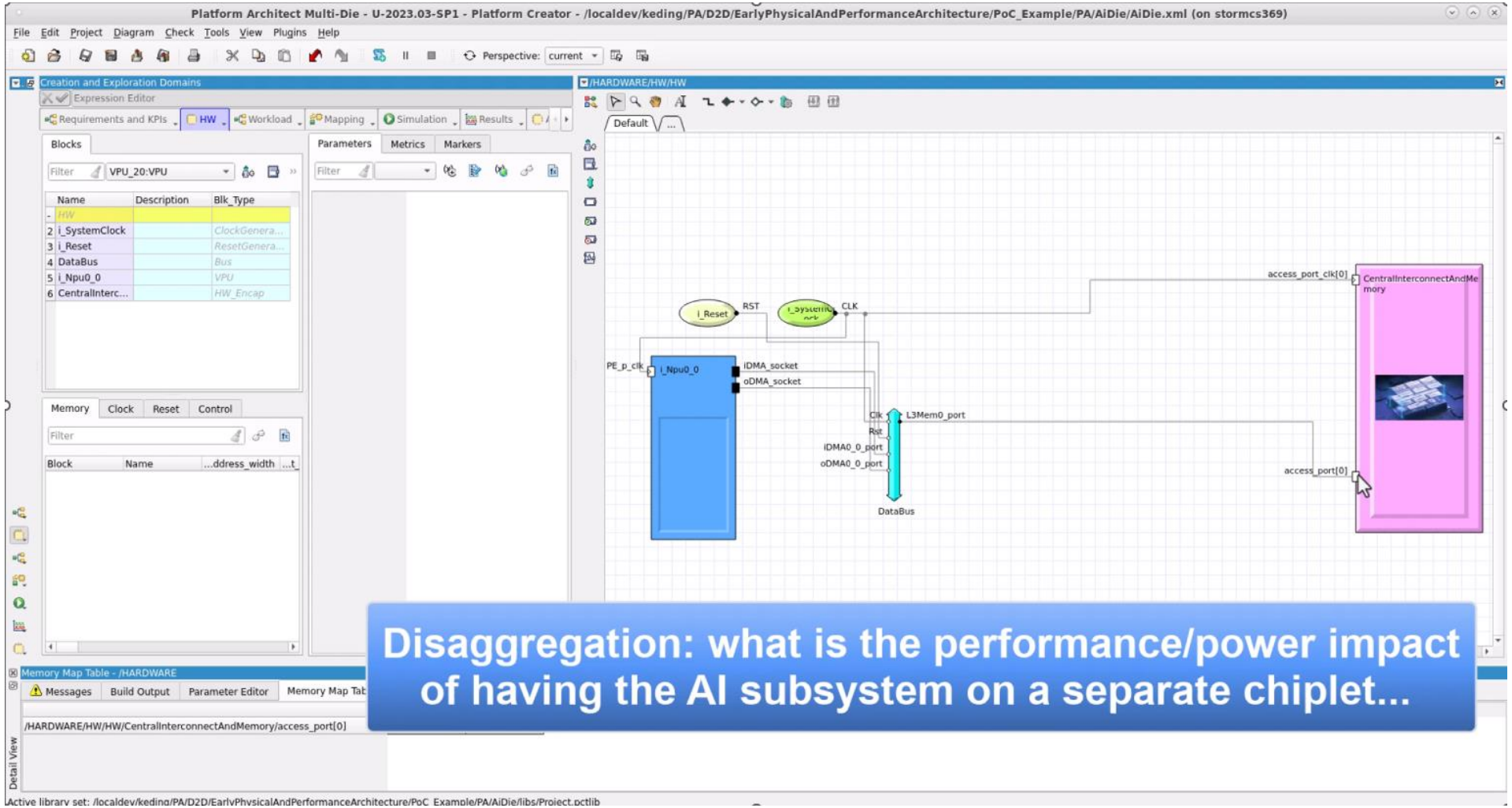




Demo Video
Multi-Die Power/Performance Analysis Case-Study

1. Show system disaggregation and D2D adapter configuration options
2. Run simulations to find D2D link configuration meeting functional performance requirements
3. Analyze the resulting data using sensitivity charts – identify trends and best suited configurations

Demo Video Placeholder

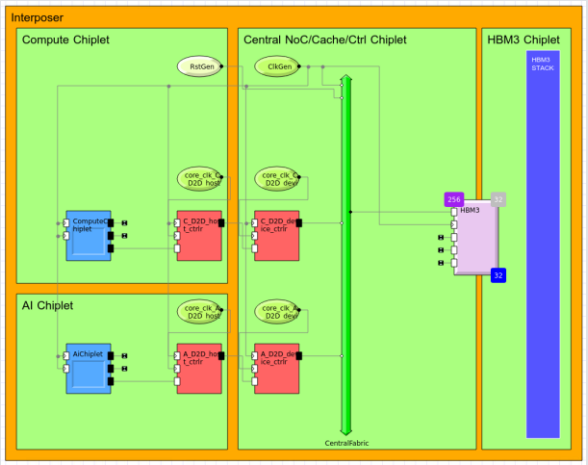


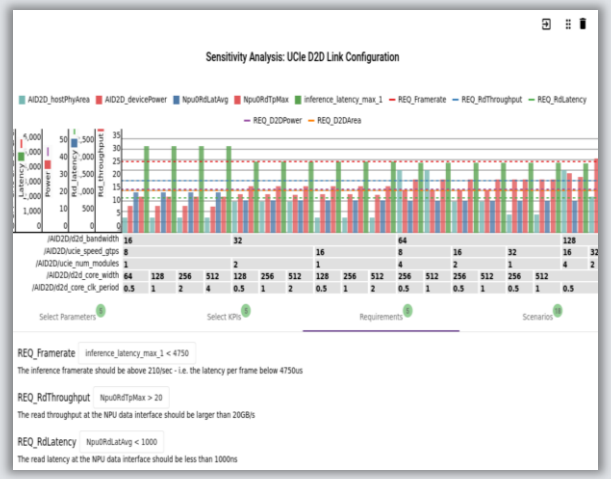
Case Study Results

Multi-die performance/power analysis of AI workload

- Requirements met / Goals achieved:
  - Framerate 212Hz = 4.72ms inference latency per frame
  - D2D power < 50mW

- Optimize hardware configuration:
  - UCIe interface: 2 modules, 16GT/s, 512bit core @ 1GHz
  - AI (NPX6) chiplet memory: 16MB CSM





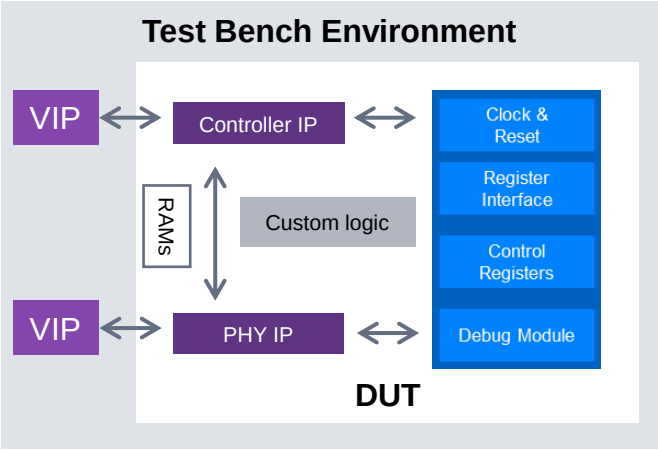
Agenda

- Multi-die market trends and challenges
- Multi-die architecture performance and power validation
- Functional verification of multi-die designs
- Multi-Die physical architecture validation, optimization, and sign-off
- Summary

How to Reduce SoCs Tape-out Risks?

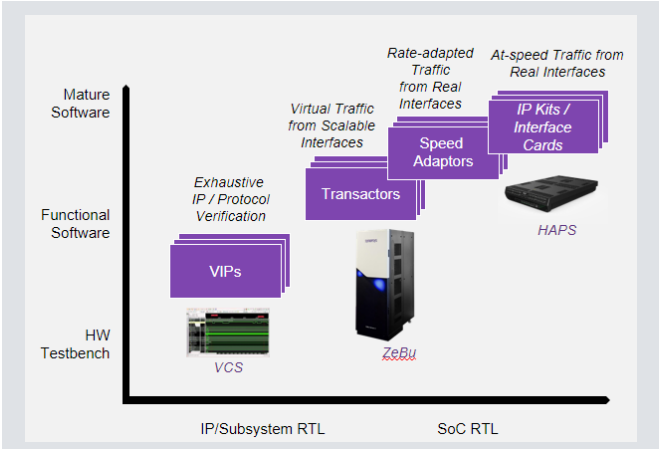
IP/Vendor Selection

- Broadest IP VIP portfolio
- Pre-tested, silicon-proven IP Subsystems for your SoC
- IP & SoC experts configure and customize to your requirements



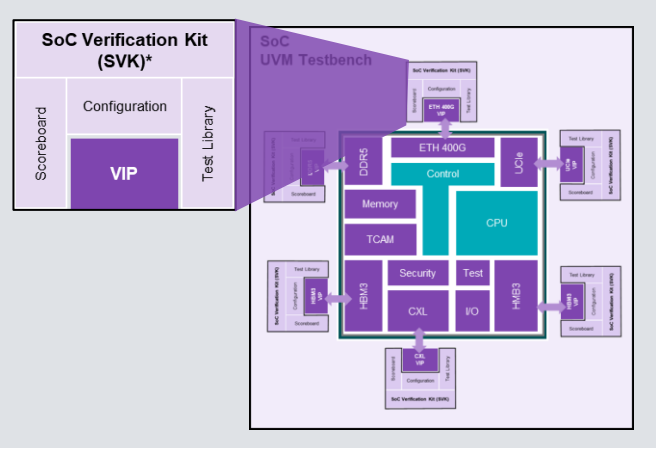
IP Qualification

- Active engagement with standards bodies and eco-system partners
- Ready-to-go compliance test suites for IP qualification
- Frees your team to work on your product differentiation

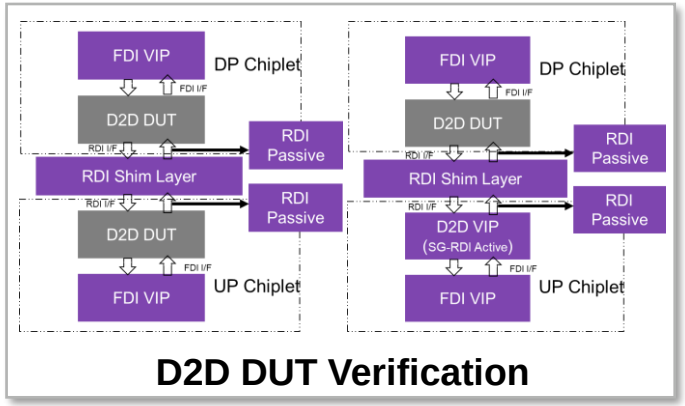


IP Integration

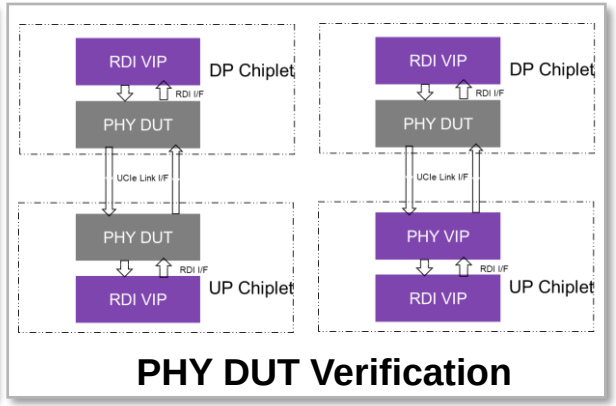
- Reference flows and services for IP integration and convergence between project teams
- First-time-right SoC integration speeds TTM



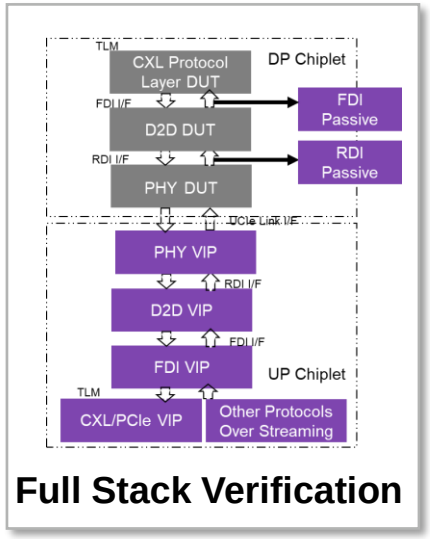
UCIe VIP Use-cases and Topologies



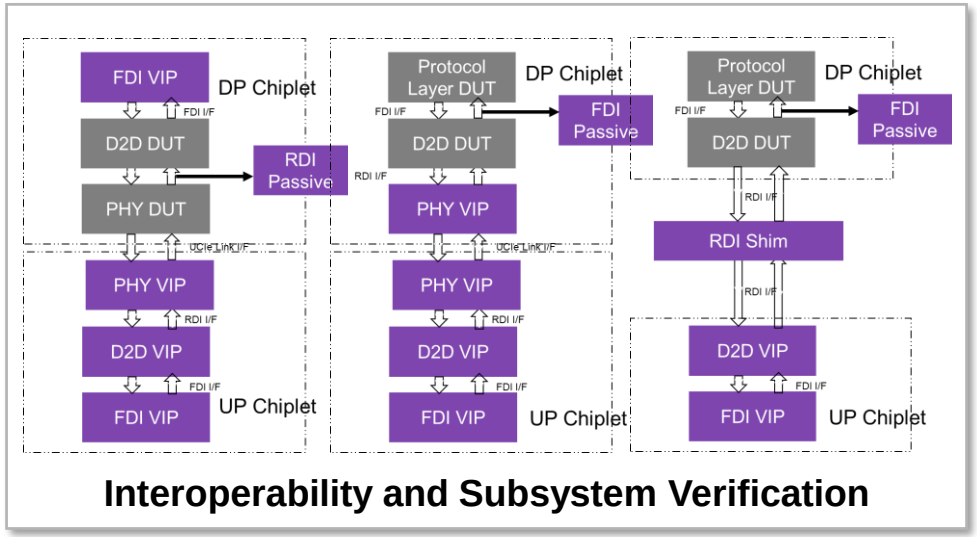
D2D DUT Verification



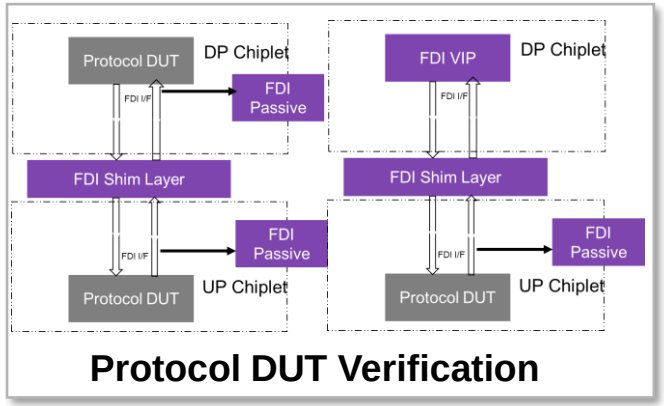
PHY DUT Verification



Full Stack Verification



Interoperability and Subsystem Verification



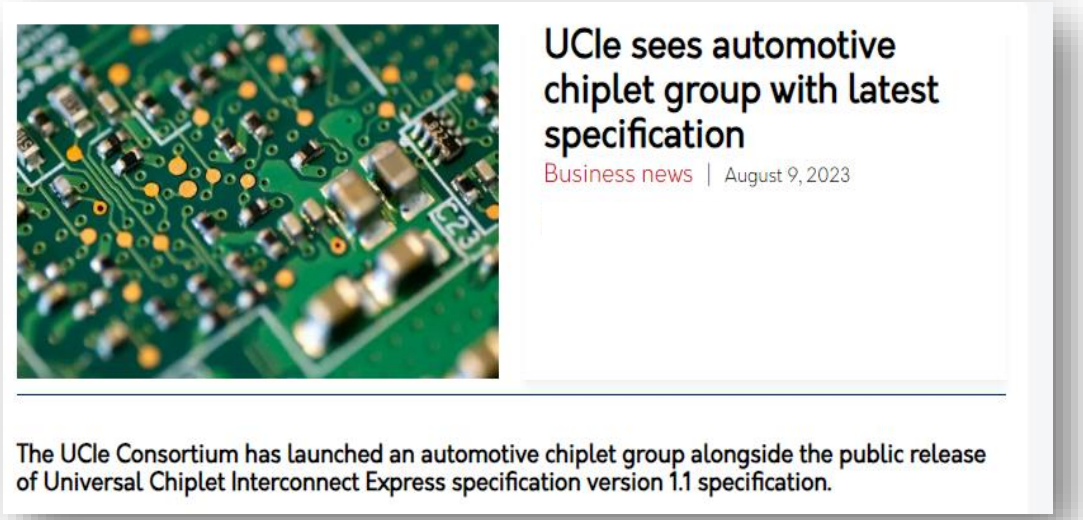
Protocol DUT Verification

- Verification topologies for various Design types
- Use-cases:
  - D2D / PHY / Protocol Layer DUT
  - D2D-PHY Interoperability
  - Protocol-layer-D2D-Controller Interoperability
  - UCIe Subsystem
  - UCIe Full Stack

UCIe 1.1 Focus on Automotive Requirements

Safety, Security, Reliability and Ecosystem Adoptions

- Preventive monitoring
- In-field repairability
- Multi-protocol support for ecosystem adoption
- Cost Optimization
- Compliance Testing



Preventive Monitoring

Design and Verification considerations	VIP features

Continuous monitoring & reporting	• API
	  • Control eye margins during LTSM states
	  • Read/write UHM registers

Failure rate of link	• Parity computation and correction • Callback to inject parity error

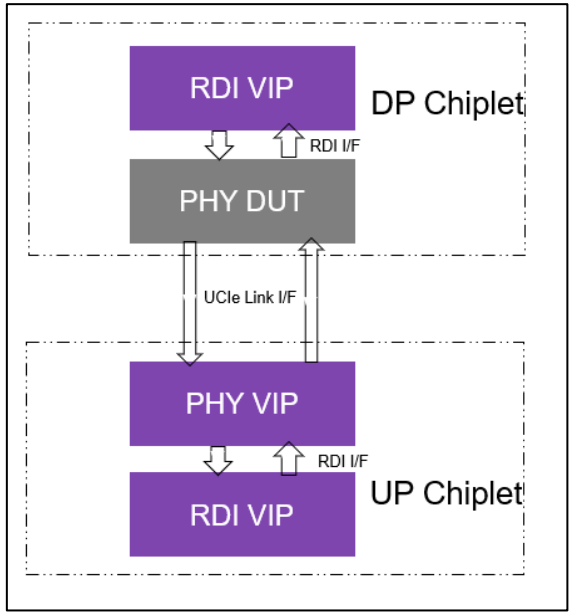
PHYRETRAIN	• Local and remote Adapter and PHY initiated retrain
	• API
	  • Control retrain pattern count
	  • Corrupt retrain results
	  • Forcibly move to retrain state

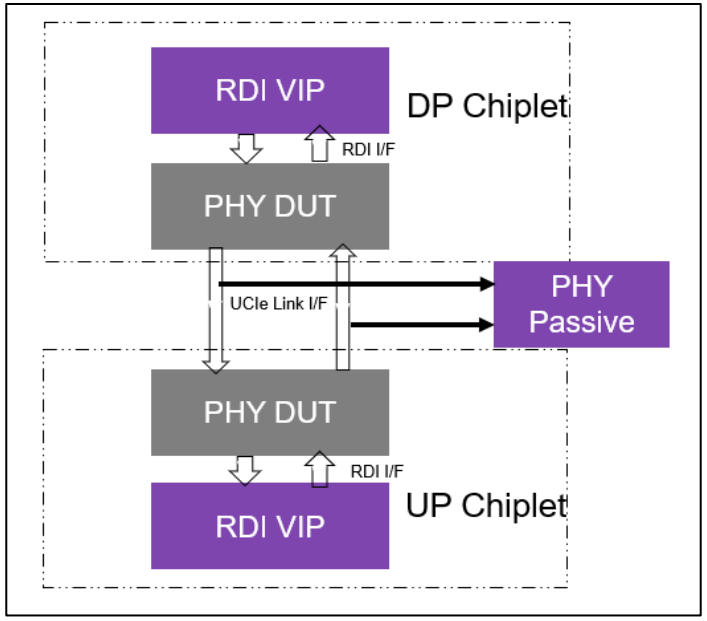
Interrupt	• API to enable/disable interrupts

Protocol checks to catch unexpected DUT behaviours

In-field Repairability

- Repairability Considerations
  - *Redundancy mapping:* Clock and valid lane mapping, single lane and two-lane data mapping
  - *REPAIR:* Usage of Redundant pins to repair clock, valid and data lanes
  - *TRAINERROR:* Repair of lanes is not feasible





Ecosystem Adoption

- Streaming Protocol usage considerations
  - *Flit formats*: Usage of existing PCIe/CXL flit formats for various streaming protocol chiplets e.g. AXI, CHI, vendor defined etc.
  - *Features:* Use D2D features like CRC, Retry, parity, etc.

Flit Format Number	Flit Format Name	PCIe Flit Mode	CXL 68B Flit Mode	CXL 256B Flit Mode	Streaming	
					UCIe 1.0	UCIe 1.1
1	Raw	Optional	Optional	Optional	Mandatory	Mandatory
2	68B	N/A	Mandatory	N/A	N/A	Supported
3	Standard 256B End Header	Mandatory	N/A	N/A	N/A	Supported
4	Standard 256B Start Header	Optional	N/A	Mandatory	N/A	Supported
5	Latency Optimized 256B without optional Bytes	N/A	N/A	Optional	N/A	Supported
6	Latency Optimized 256B with optional Bytes	Strongly Recommended	N/A	Strongly Recommended	N/A	Supported

Ecosystem Adoption

- Streaming Protocol usage considerations
  - *Flit formats*: Usage of existing PCIe/CXL flit formats for various streaming protocol chiplets e.g. AXI, CHI, vendor defined etc.
  - *Features:* Use D2D features like CRC, Retry, parity, etc.

Flit Format Number	Flit Format Name	PCIe Flit Mode	CXL 68B Flit Mode	CXL 256B Flit Mode	Streaming	
					UCIe 1.0	UCIe 1.1
1	Raw	Optional	Optional	Optional	Mandatory	Mandatory
2	68B	N/A	Mandatory	N/A	N/A	Supported
3	Standard 256B End Header	Mandatory	N/A	N/A	N/A	Supported
4	Standard 256B Start Header	Optional	N/A	Mandatory	N/A	Supported
5	Latency Optimized 256B without optional Bytes	N/A	N/A	Optional	N/A	Supported
6	Latency Optimized 256B with optional Bytes	Strongly Recommended	N/A	Strongly Recommended	N/A	Supported

Ecosystem Adoption

Design and Verification considerations	VIP features
Link initialization	• Parameter exchange advertisement • Clock gate handshake for independent FDI interface • API to move to specific state

Data Flow	• Independent interfaces to transport data using multiple instances
	• API
	  • Configure flit format
	  • Configure protocol for both stacks
	• Data integrity check using CRC, parity etc.

Throughput	• Per flit arbitration with 50% bandwidth

Error injection	• Callback
	  • To inject error in flit
	  • To corrupt sideband messages

Cost Optimization

Design and Verification considerations	VIP features

Parameter Exchange	• UCIe-A x32 parameter exchange
	• API
	  • Enable x32 support
	  • Bypass link states
	  • Move to specific link state

MB Repair	• API
	  • Control repair pattern count
	  • Corrupt repair result

MB Reversal	• API
	  • Control reversal pattern count
	  • Corrupt reversal result

Data Flow	• API
	  • Control inter packet delay
	  • Inject back pressure

Compliance testing

Testing Phases

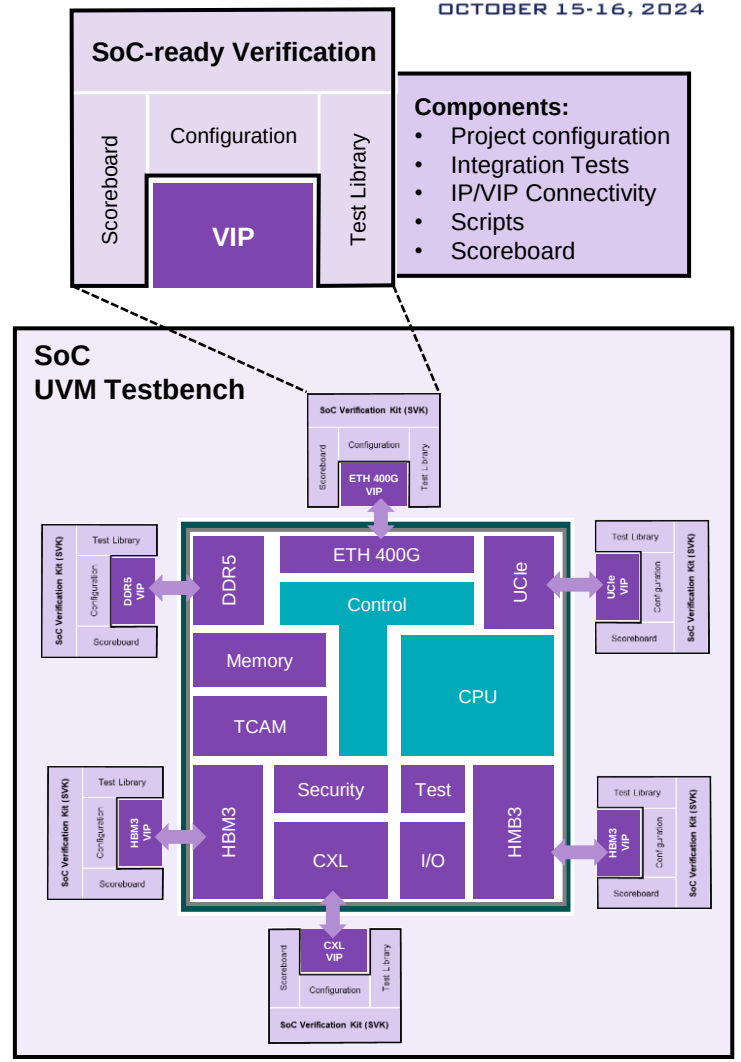
Phases	Phase1	Phase2	Phase 3
Goal	Bring Up	Data Flow	Error injection
Design Verification Consideration	• Link up • RDI bring up • FDI bring up	• Flit formats • CRC, parity, retry etc. • Data integrity	• Error injection at each layer

VIP feature	• API
	  • Trigger link initialization
	  • Control training pattern counts
		• API
		  • Drive sideband and main-band traffic.
		  • Control parity and retry features
		• Analysis port at each interface for score-boarding
		• All flit formats
			• Callback
			  • To inject errors
			  • To block sideband response message
			• API
			  • Control timeout of state
			  • Delay sideband response message

SoC-level Verification

Transition from IP-level to SoC-level Verification

- Challenge
  - Re-use IP-level testbenches for SoC verification
- Approach
  - “SoC-ready” modular testbench structure
  - Provides testbench components for SoC integration
- Benefits
  - Accelerates the SoC testbench development
  - Enables testing of Interface IPs in Subsystem/SoC environment
  - Lowers integration risk



UCIe 2.0 Focus on Manageability and 3D Packaging

Safety, Security, Reliability and Ecosystem Adoptions

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

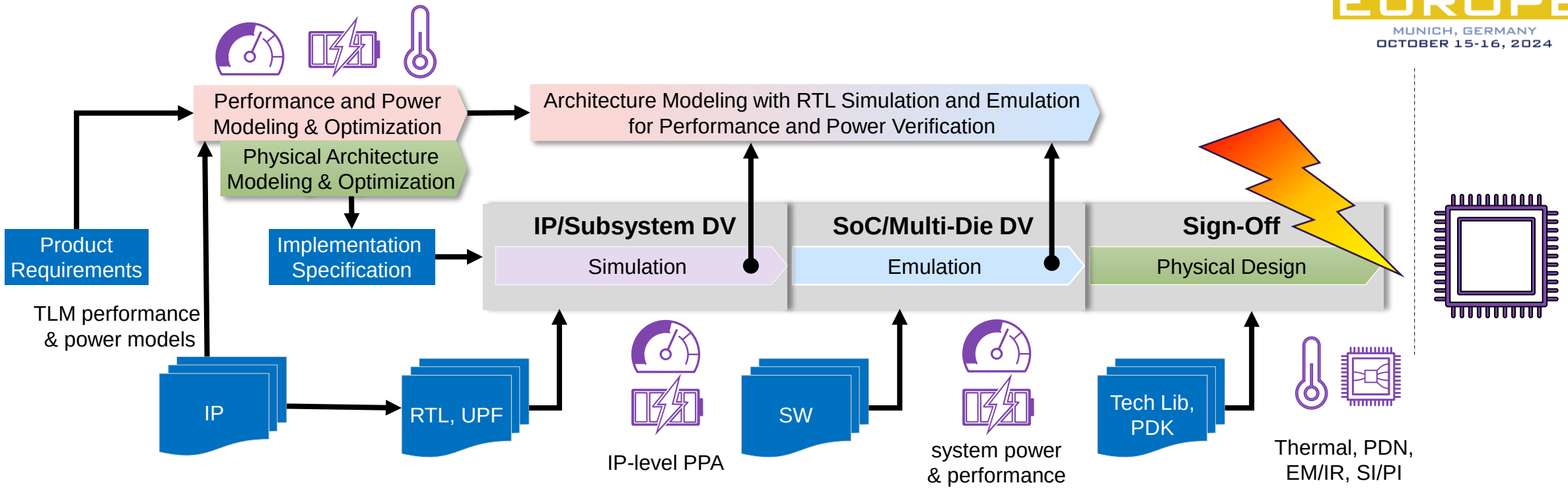
- Management Transport Protocol (MTP)
- UCIe Debug and Test Architecture (UDA)
- UCIe-S Sideband only (SO) port
- x8, x4 link width for standard package
- UCIe 3D packaging

Agenda

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

- Multi-die market trends and challenges
- Multi-die architecture performance and power validation
- Functional verification of multi-die designs
- Multi-Die physical architecture validation, optimization, and sign-off
- Summary

Physical-aware Architecture Optimization



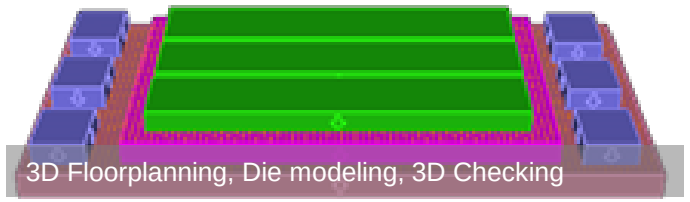
- **Goal:** Consider physical effects during architecture specification
- **Use cases:** Multi-die geometry and floor-plan, thermal analysis, power-delivery network architecture

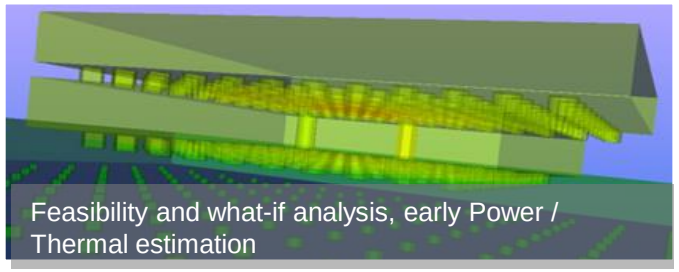
3DIC Compiler Platform

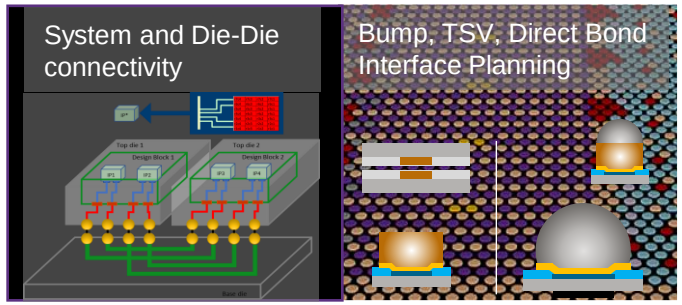
Unified exploration-to-signoff platform for multi-die designs

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

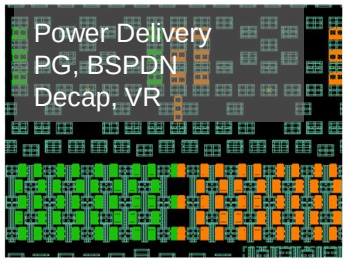
Design

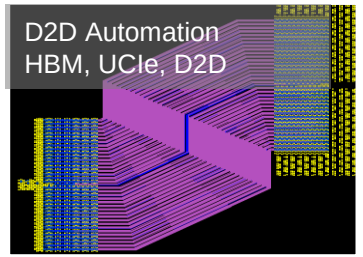


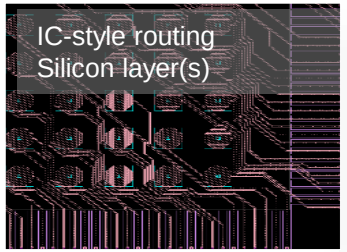


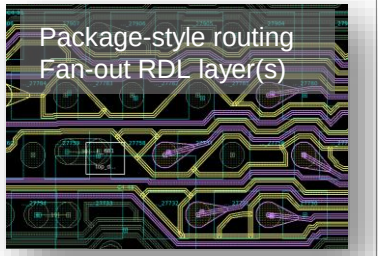


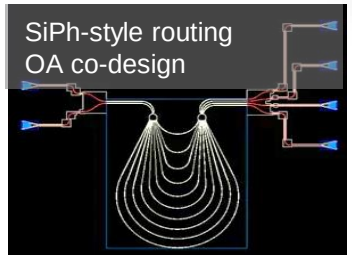
Implement

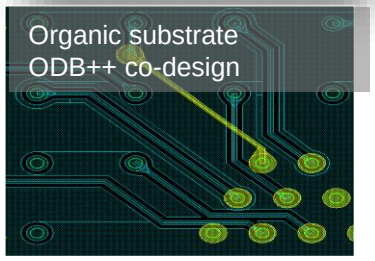




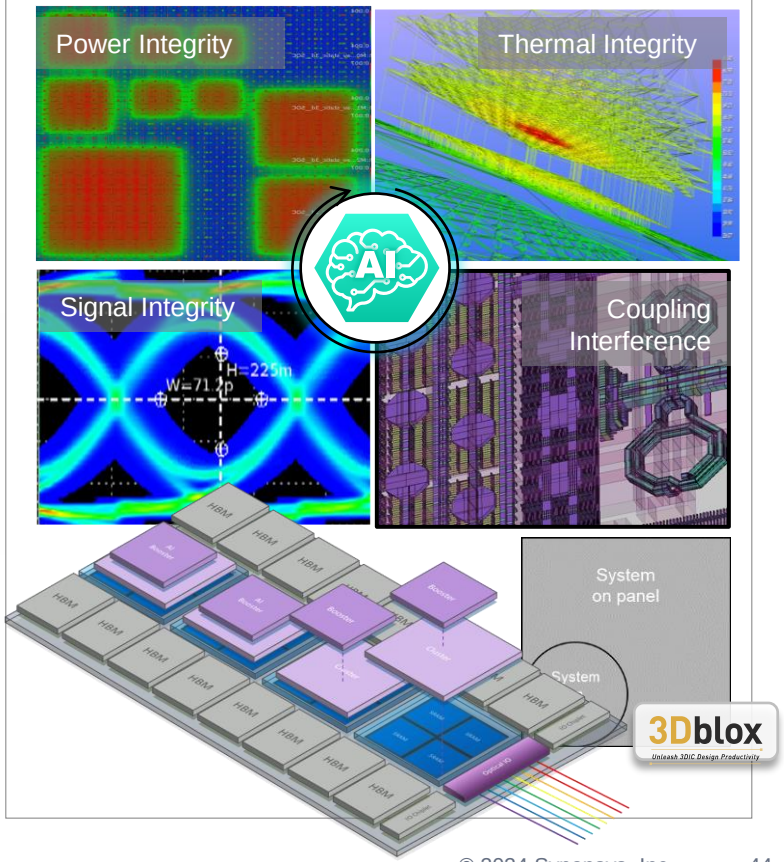






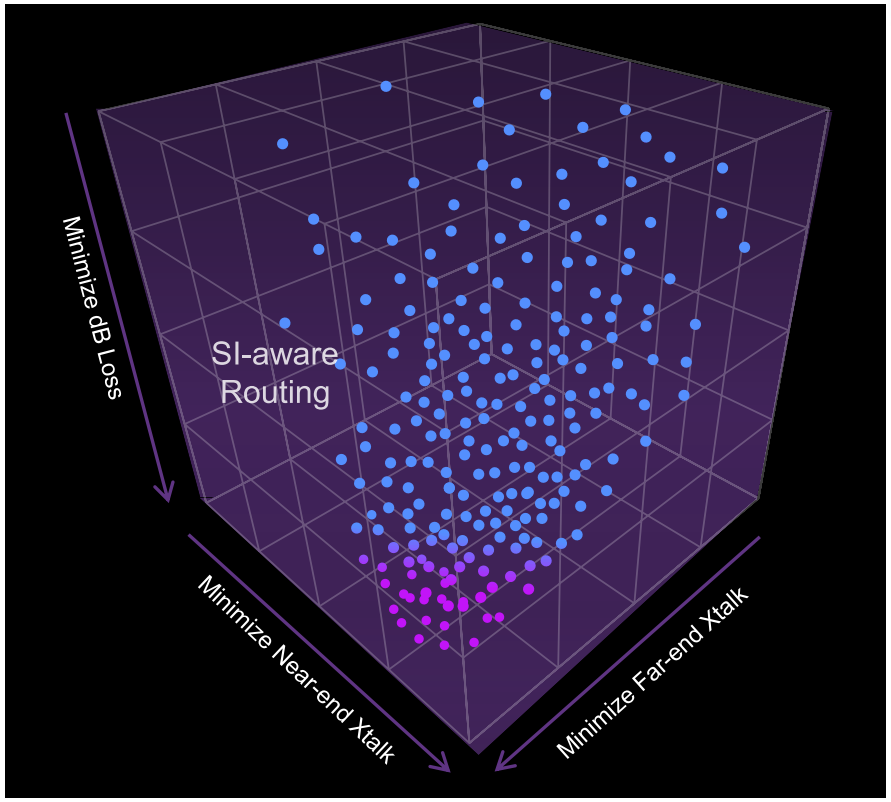


Optimize



AI-driven Multi-Die Design Space Optimization

Autonomous exploration and optimization of 2.5D/3DHI design space



Integrated AI optimization of multi-die designs for signal, thermal and power integrity in single design platform

Fast native analysis for system performance and compute efficiency, while maximizing quality-of-results (QoR)

Scalability to optimize across massive 3D design space of hundreds of billions of transistors and trillions of permutations

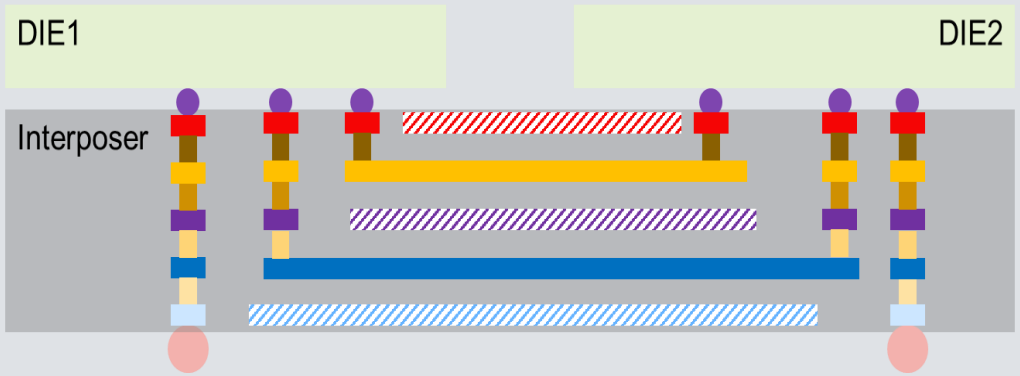
CoWoS-S Interposer UCIe PHY Routing Validation

Dense routing with 78 signals per signal layer in 388um cross section

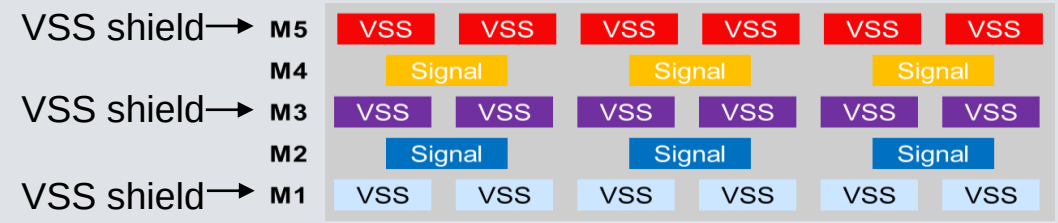
Interposer: CoWoS-S

- Metal stack: 5M-5I
- eDTC not used

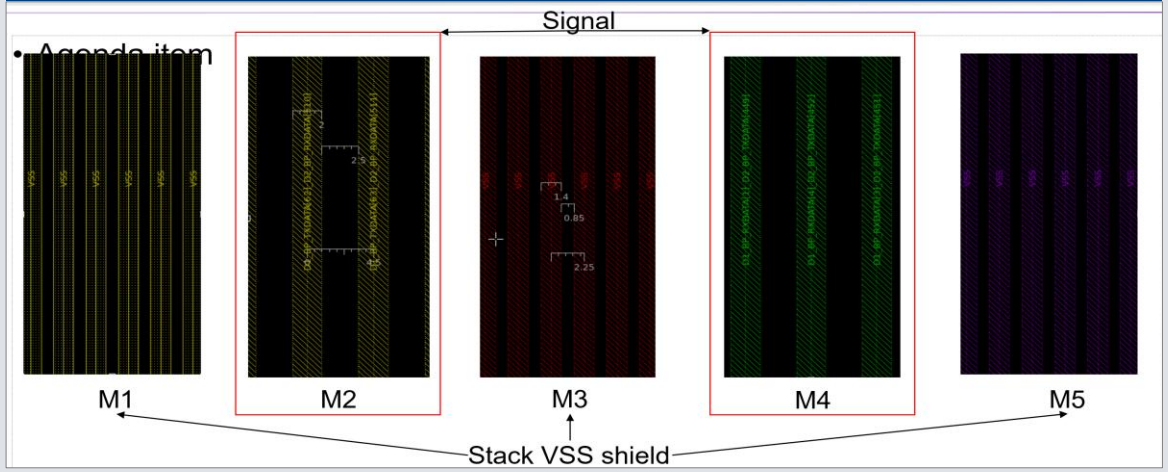
- Bump pitch: 45um
- Routing pitch: 4.5um
- Shielding optimized for XTALK minimization
- Channel length: ~2mm



Interposer Cross Section (4.5um signal pitch)



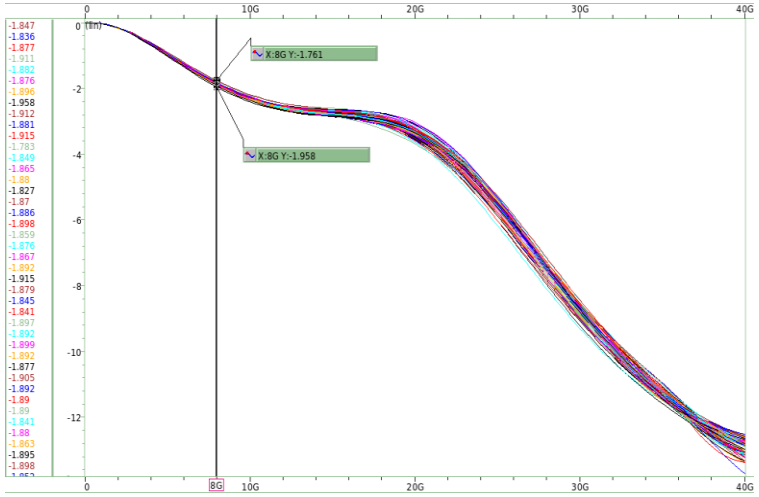
Interposer Layout Detail



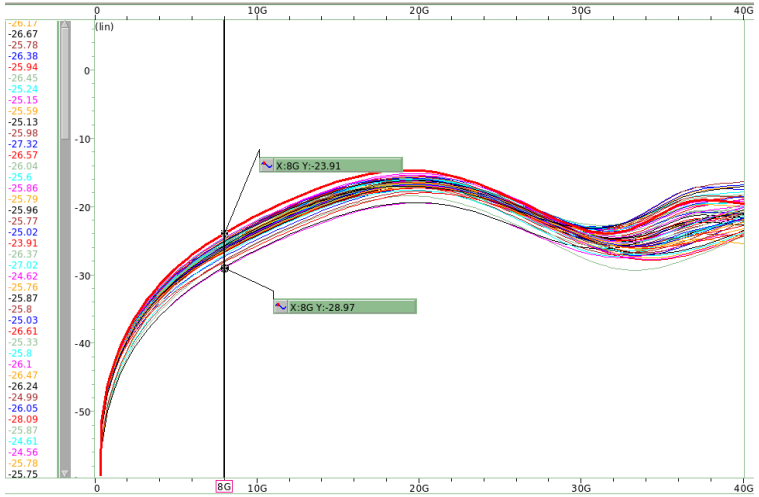
Signal Integrity Validation of CoWoS-S Test Chip

UCIe routing optimization using Synopsys 3DIC Compiler

Insertion Loss Results (all Channels)



Crosstalk Results (All Channels)



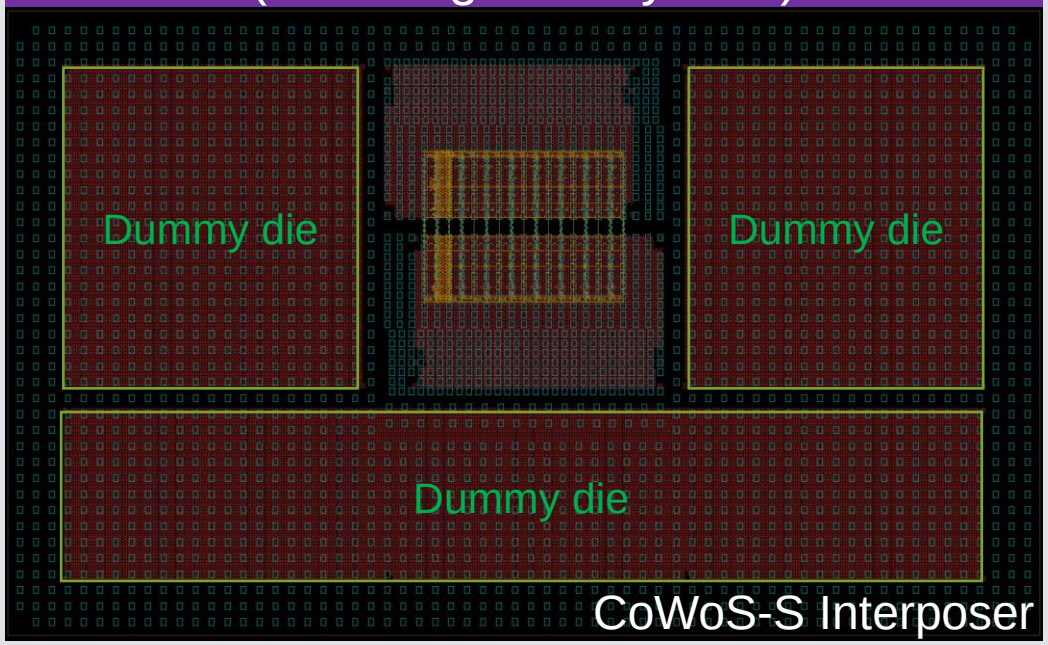
Signal Integrity (SI) Optimization with Synopsys 3DIC Compiler

Parameter	Specification	Manual	Optimized
Insertion Loss	> -3 dB	-2.48 dB	-1.91 dB
PSFEXT	< -23 dB	-21.7 dB	-23.91 dB

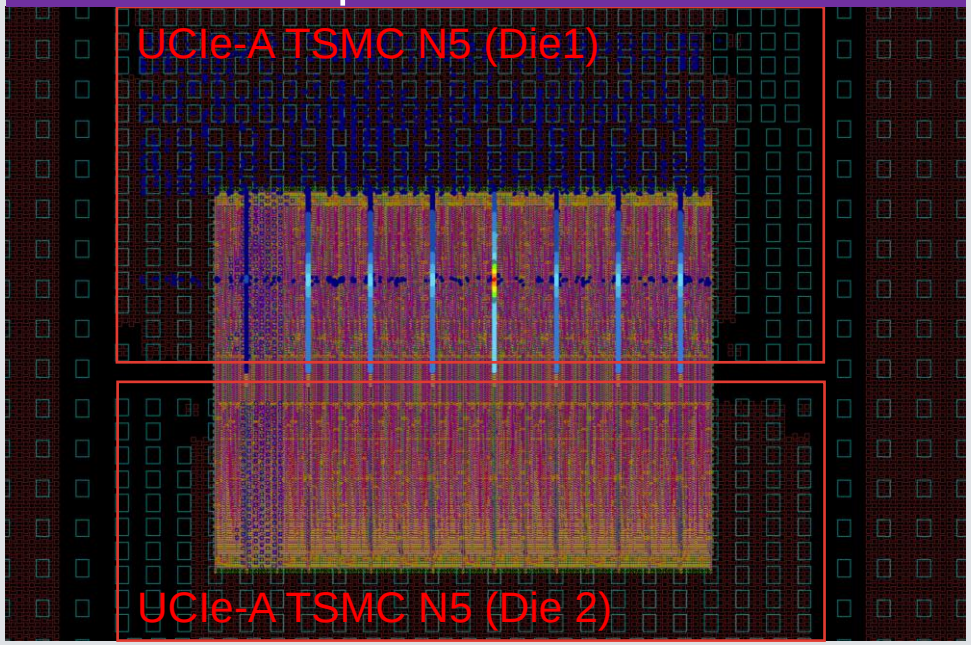
UCIe-A on TSMC N5 with CoWoS-S Test Chip

8 UCIe-A (x64) modules are routed over CoWoS-S interposer

Layout of Interposer (including dummy dies)



Close View of the Test Chip dies & D2D Traces

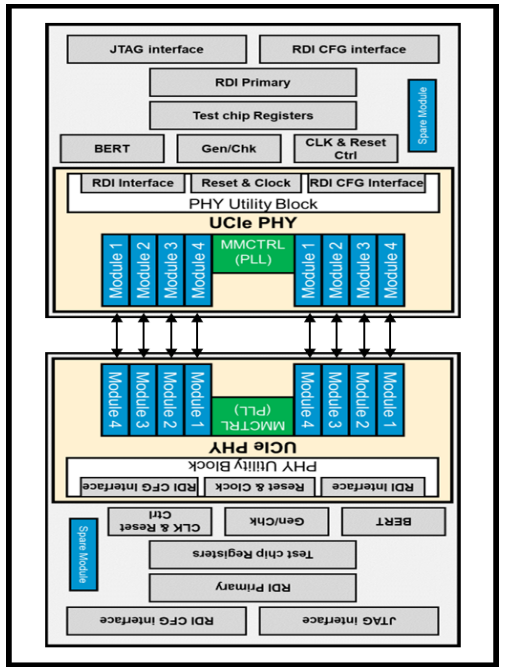


UCIe-A PHY on TSMC CoWoS-S Silicon Results

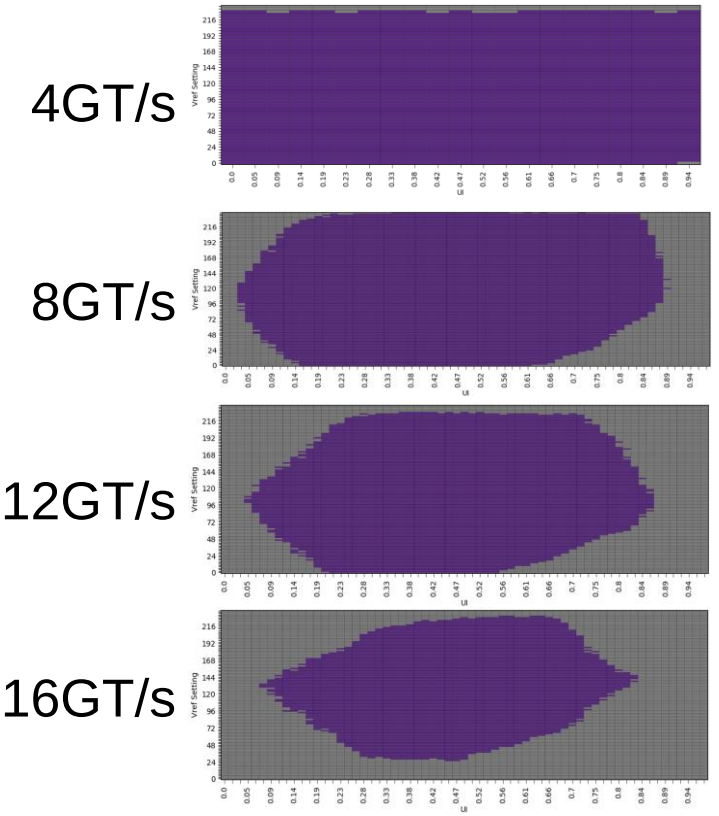
Results validate UCIe-A over CoWoS design methodology

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

Leveraging Comprehensive Testability Functionality in Synopsys UCIe PHY

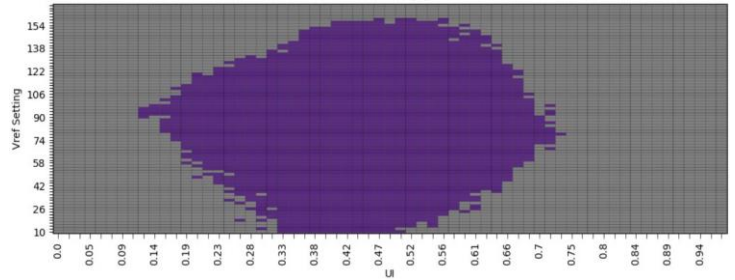


Eye Diagrams

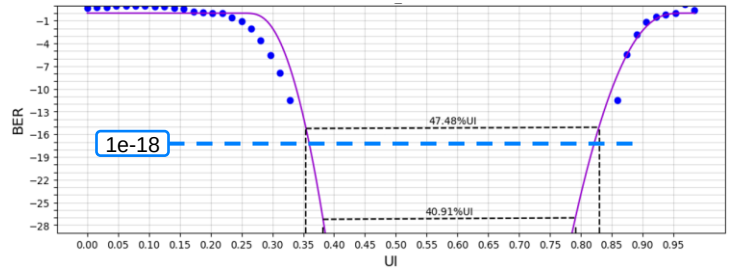


Robust Performance

24GT/s “Overclocked” Eye



16GT/s Bathtub Plot



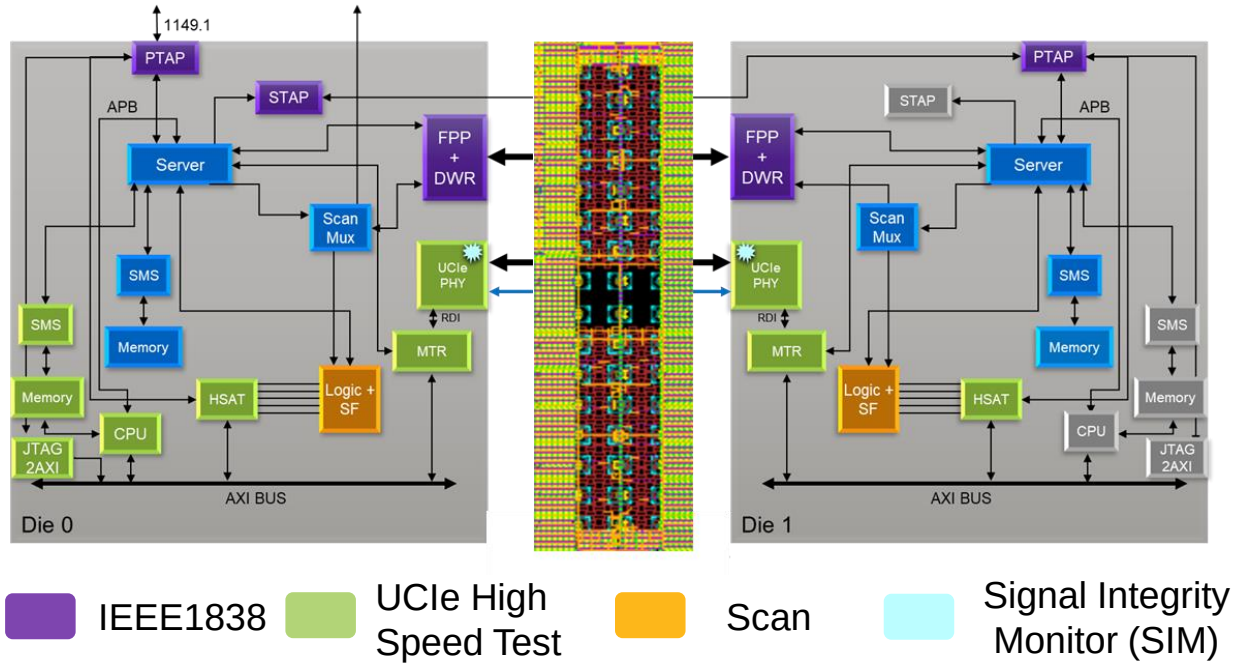
UCIe PHY is Silicon Proven on TSMC N5 with Various Package Technologies

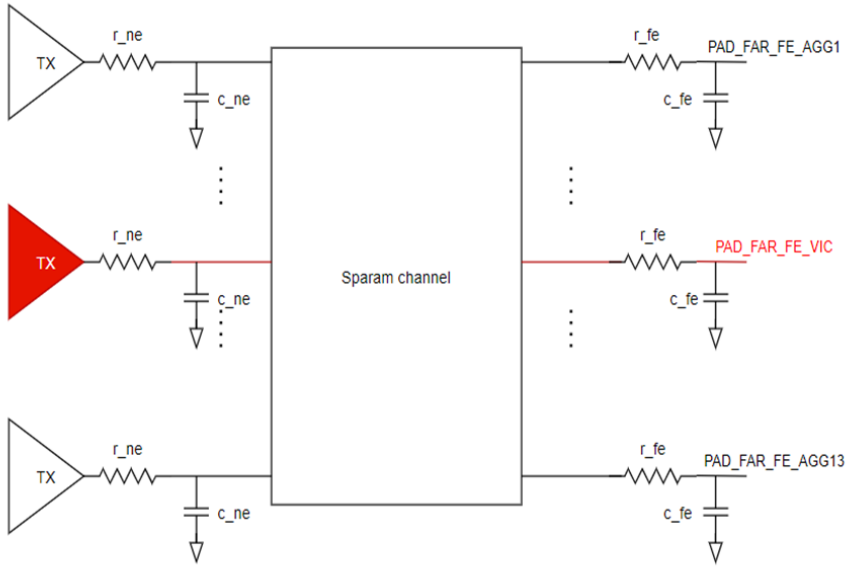
Case Study: UCIe Multi-Die SLM & Test Architecture

Test, Repair & Monitoring of Interconnect, Memory, and Logic

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

- 3DSO.ai used to optimize layout and performance of D2D Routing
  - AI-driven optimization: Insertion Loss (IL), Near-End Cross-Talk (NEXT), Far-End Cross-Talk (FEXT)
  - Goal is for multiple solutions with improved Signal Integrety



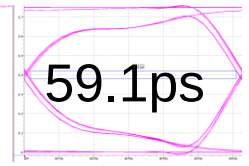
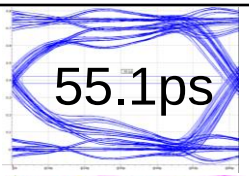
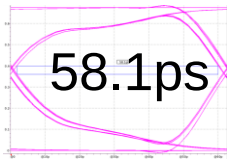
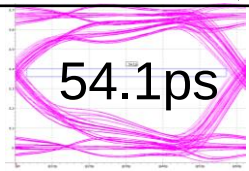
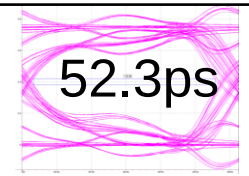
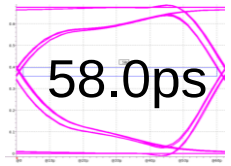
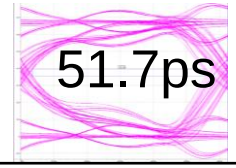


Transient Simulation Setup

Results: Typical and Slow Corner

Summary: 64 nets

Parameters	Specification [ps]	Typical corner [ps]	Slow corner [ps]
ISI eye opening	50 (0.8UI)	59.1 (0.946UI)	58.0 (0.928UI)
ISI jitter	8.75	62.5(1*UI) - 59.1 = 3.4	62.5(1*UI) - 58.0 = 4.5
Xtalk eye opening	50 (0.8UI)	52.3 (0.837UI)	51.7 (0.821UI)
Xtalk jitter	6.88	59.1 - 52.3 = 6.8	58.0 - 51.7 = 6.3
Total jitter[ps]	15.62	3.4 + 6.8 = 10.2	4.5 + 6.3 = 10.8
Total jitter[UI]	0.25UI	0.163UI (10.4/62.5)	0.173UI (10.8/62.5)

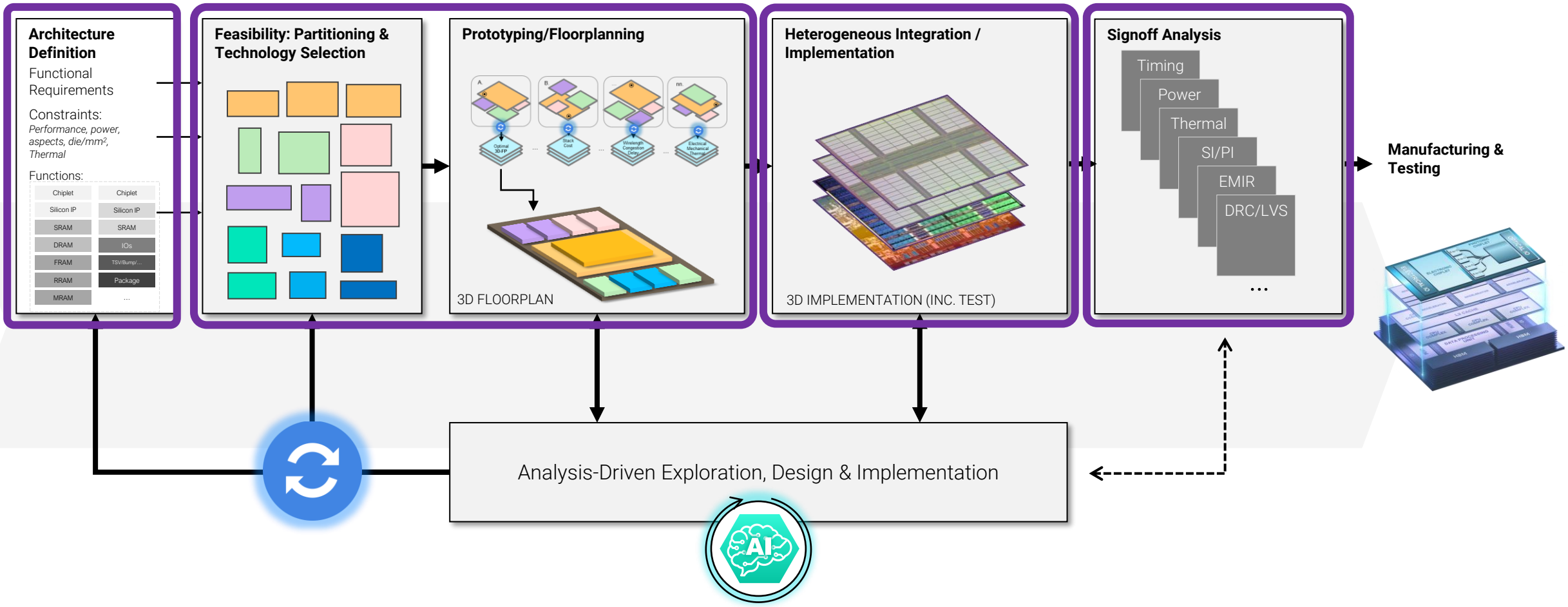
	ISI at Far End	Xtalk at Far End
Typical corner (21 nets)		
Slow corner (21 nets)		
Typical corner (64 nets)		
Slow corner (64 nets)		

I/O Buffer Information Specification (IBIS) definition

Temp range	25.0	-40.0	125.0
Voltage range	750.00mV	675.00mV	825.00mV

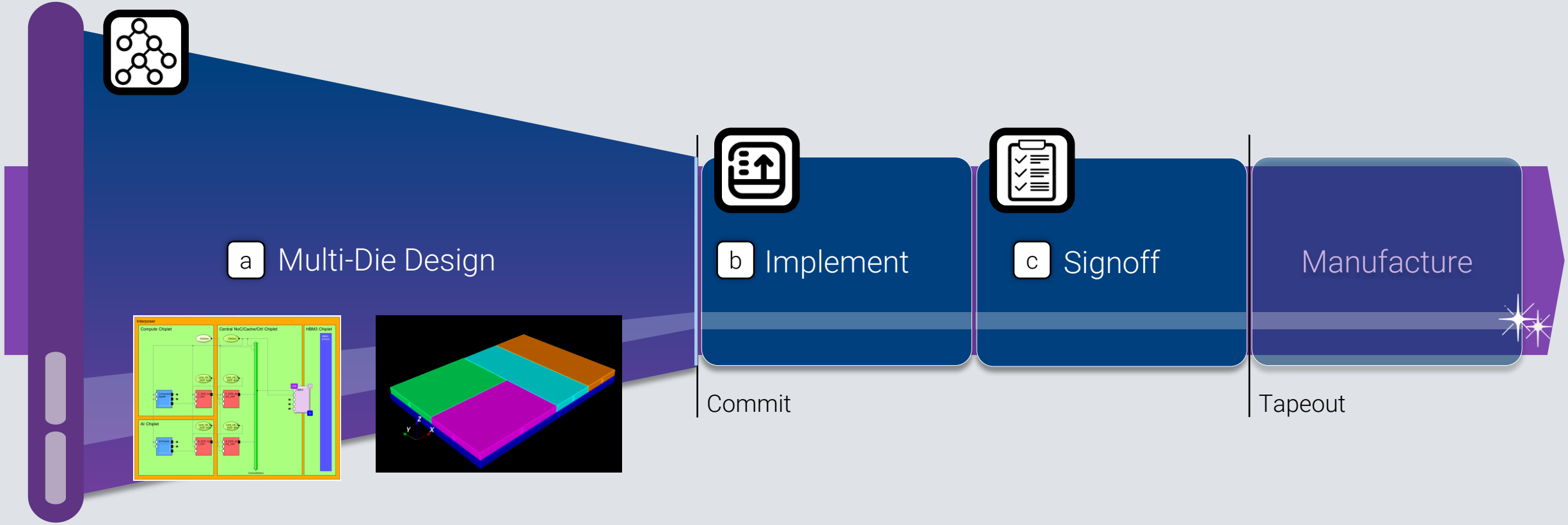
Synopsys' Multi-Die Design Methodology

Efficiently create, implement, optimize, and close in one place



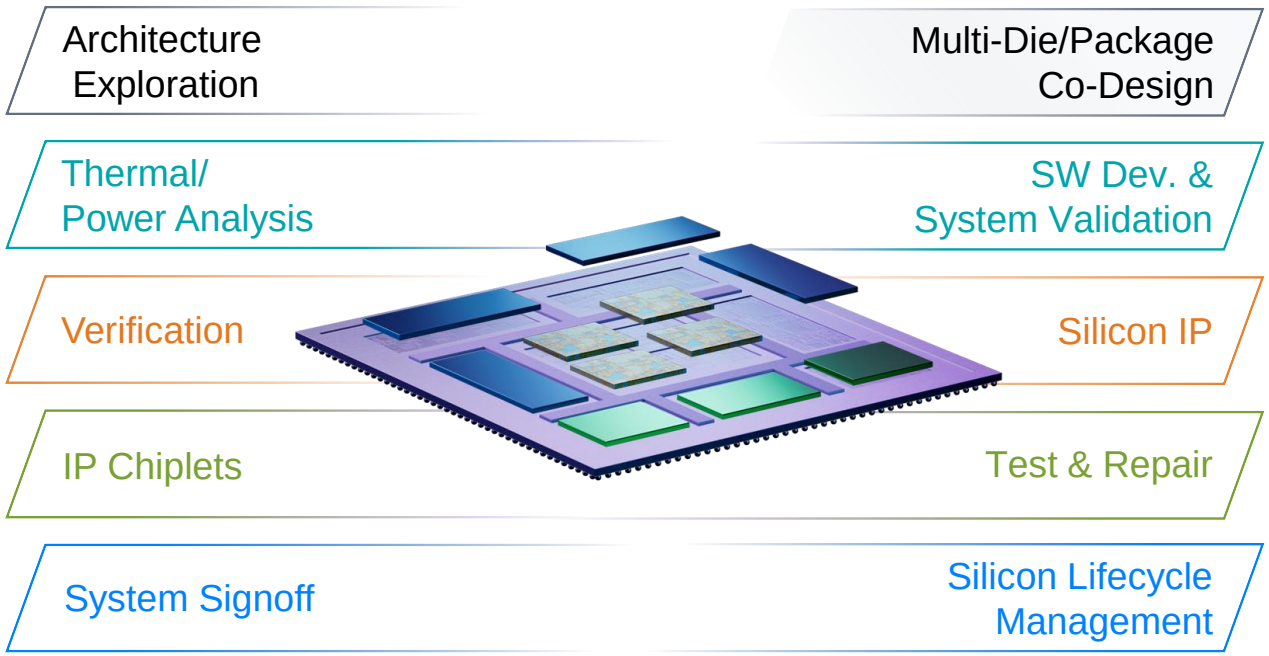
The Multi-Die Design Convergence Path

Uncovering bottlenecks and PPA + cost opportunities



Synopsys Multi-Die Solution

A comprehensive and scalable solution for fast heterogeneous integration



Architecture Exploration	Optimize thermal, power, and performance with early exploration and partitioning
Software Dev. & Validation	Rapid software development and validation with high-capacity emulation & prototyping
Design Implementation & IP	Efficient die/package co-design with unified exploration-to-signoff platform and robust IP
Manufacturing & Reliability	Improve health, security and reliability with holistic test and lifecycle management solutions

2024 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

SYNOPSYS®

synopsys.com/multidie