Accurate Charge-pump Regulator Modeling using SV EEnet

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MOTIVATION

➢ To model analog blocks with high accuracy
➢ To balance simulation speed and accuracy for SOC functional verification
➢ Extend functional coverage in top-level verification and reduce effort and time for AMS

CHARGE-PUMP REGULATOR

➢ Internal power supply used in boost converter products
➢ Consists of a current-controlled oscillator, 2x cross-coupled charge-pump, a high gain amplifier, a resistor-divider and a Power FET

MODEL VERIFICATION

➢ Model matches with schematic with load current steps up to 1mA, 2mA, 3mA, 4mA
➢ Model sim runs 10.36 seconds, 10x speed up compared to schematic

SYSTEM VERILOG EENET

➢ Built-in SV nettype supported by Cadence with 3 fields, V, I and R
➢ Include analog impedance-based interactions

CHARGE-PUMP MODEL

➢ Two-phase switch capacitor circuits

NMOS FET MODEL

➢ Nonlinear function of gate voltage
➢ Composes of a dependent current source and an internal resistor in parallel.

OSCILLATOR MODEL

➢ RC delay circuit and 3 inverter buffers
➢ Oscillator frequency is proportional to its controlled bias voltage

REFERENCES


ACKNOWLEDGEMENT

Highly appreciate Ayesha Huq for her fully guidance and support.
Many Thanks to Tulong Yang for his great help and suggestions.