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Mixed-Signal Design Verification: Leveraging the Best of AMS and DMS

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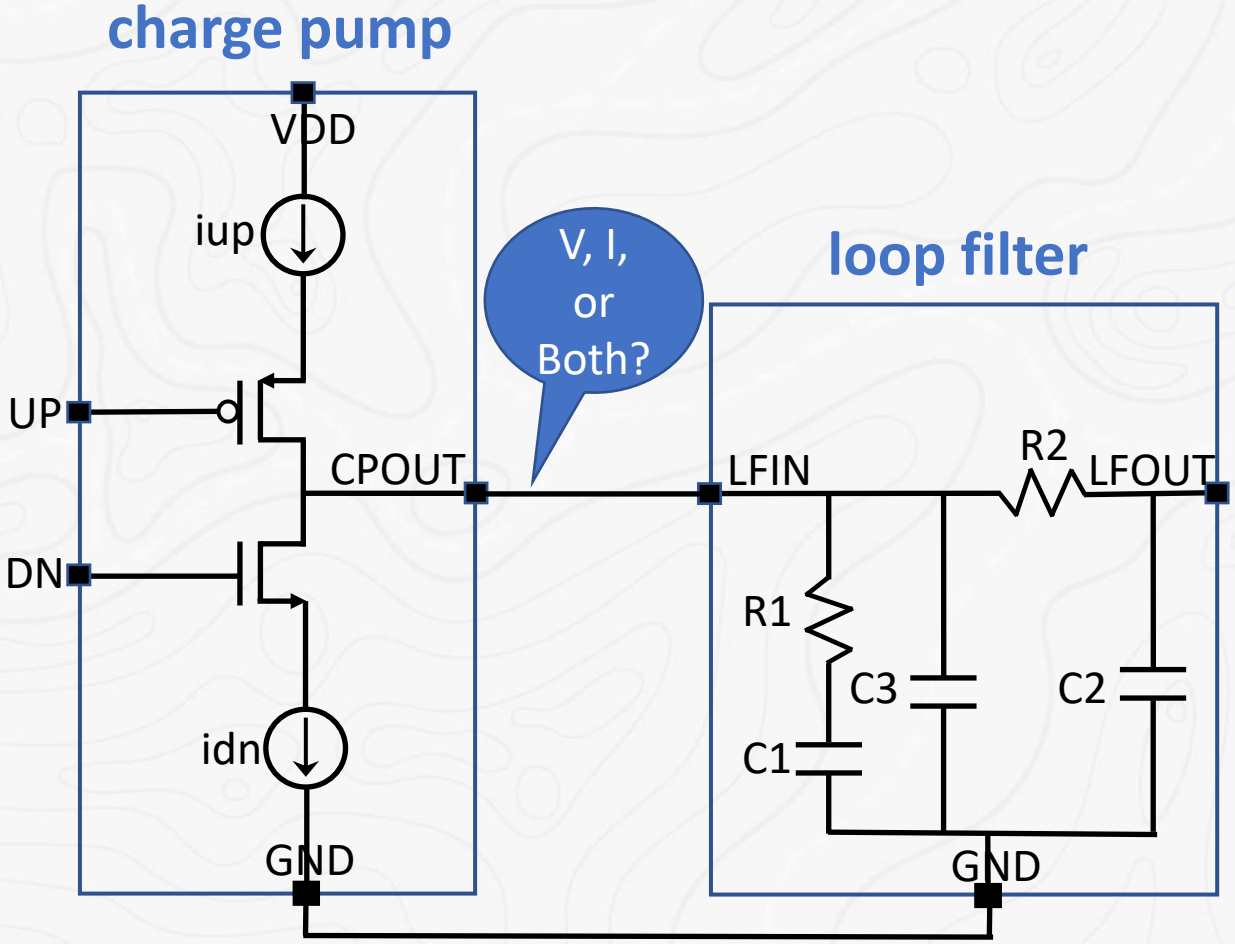
Introduction

- The role of analog and mixed-signal (AMS) design and verification methodology has gradually become less clear since the emerging dominance of digital mixed-signal (DMS) methodology.
- In this paper, we seek to analyze individual roles of AMS and DMS
  - When, and why both are necessary and complementary
  - How we can take advantage of each flow's strength to optimize verification resources and job efficiency.
- Mixed-signal design verification (MSDV)
  - An emerging industry discipline and dedicated career path
  - Role, function, and spectrum of common activities

Analog Modeling is Key to the Success of MSDV

- The availability and *quality* of models for analog circuits have a large impact on the flow to use and the quality of the verification.
- DMS modeling has been found its limitation in capacity and efficiency when modeling some type of analog circuits.
- The real number modeling, being SystemVerilog real nettype or Verilog-AMS wreal, is in essence a digital modeling approach
  - Analog designers are not familiar with.
  - Always requires a digital simulator in addition to the SPICE engine.
- Analog designers continue to prefer using AMS models in their design phase for good reasons.
  - DMS models that are desired for full chip verification are usually not available from the design team.
  - DMS models developed solely for verification purpose, rarely used by analog design.

Case Study: PLL Charge Pump and Loop Filter



- CPOUT in block charge pump can be modeled as “real” variable or “wreal” nettype representing the resulting current.
- Loop filter modeling requires solving 3-rd order z-domain transfer function
  - Converting input current from CPOUT to voltage LFOUT to drive VCO.

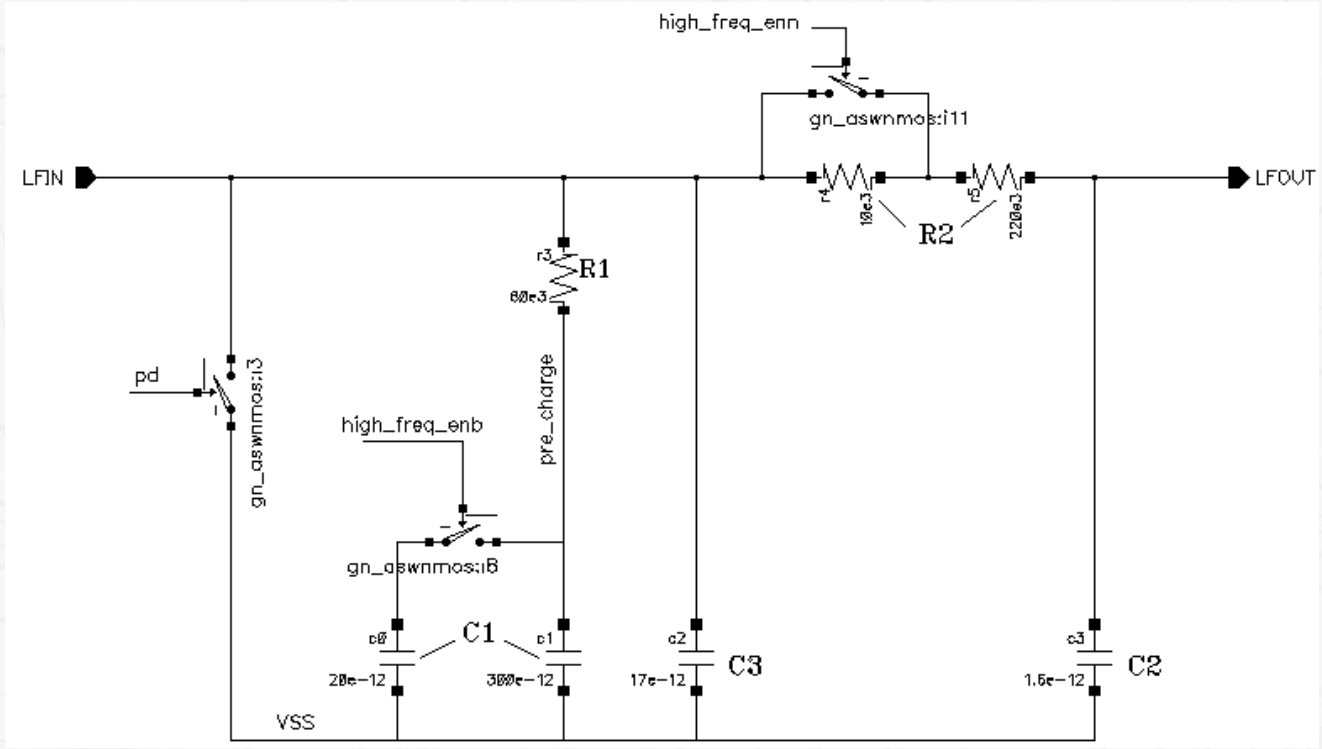
Some Challenges of Real Number Modeling

- Without SPICE engine in DMS flow, the DMS modeler himself is the analog solver
  - Node or loop analysis and solving the differential equations in a digital way.
- Signals in real number models by default are voltages (V) for nets or ports.
  - A real value in DMS models can be interpreted or modeled as a current (I) (e.g., CPOUT), but cannot be both (V and I).
  - Not a problem in most of applications, but it does introduce difficulty in modeling where both V and I are in a play on the same net.
- Advanced SystemVerilog features needed
  - User-defined type (UDT) to enable a net to carry both voltage and current simultaneously
  - User-defined resolution (UDR) to resolve multi-driver functions (e.g., resolution of summation for KCL).
  - It however would introduce extra effort to handle this special nettype in the whole verification environment.
  - It also makes AMS simulation more complicated such as special interface handling between electrical and digital UDT models.
- DMS modeling has impact on circuit partition or structure.

The Quality of Analog Behavioral Models

- We define the “quality” of an analog behavior model in the following context:
  - The intended use of the model is for full chip verification.
  - The model should facilitate full chip A-D interface connectivity and function check.
  - Some special analog behavior and performance verification at chip level.
  - The model should be validated and kept updated with analog design change.
- Developing high quality of DMS models can be time consuming.
  - High quality of DMS models often require modeling down to lower level of hierarchical analog design.
  - Model validation process long (lower-level analog design keeps changing)
  - DMS models less re-usable as they become so chip specific.
- The time a DMS model saves in a simulator can be traded off by the time to produce it.
  - AMS models, although slower in simulation, can be produced faster with less validation effort.

Loop Filter: AMS Models



- At ADI, a centralized library of general behavioral models and analog primitives are developed and maintained by a central CAD team.
- To model an analog design block, a designer often creates and maintains equivalent alternative schematics consisting of behavioral model schematic symbols
- AMS model has the advantage of using R and C primitives directly and counting on SPICE engine to solve the transformation from input current (LFIN) to output voltage

Loop Filter: DMS Models

- Find out the Laplacian transform function of the block:

$$H(s) = \frac{LFOUT}{LFIN} = \frac{n_0 + n_1 s}{d_0 + d_1 s + d_2 s^2 + d_3 s^3}$$

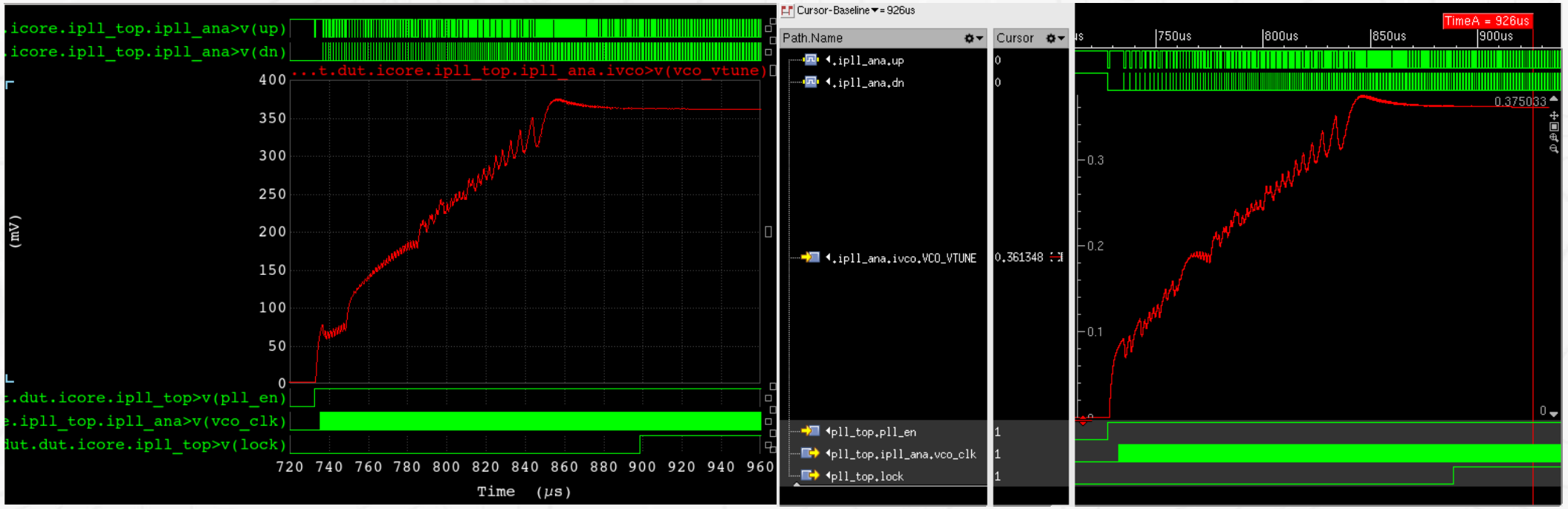
- Convert to z-domain transfer function with the Bilinear Transform

$$s = \frac{2/T_s}{(1 - z^{-1})(1 + z^{-1})}$$

$$H(z) = \frac{N_0 + N_1 z^{-1} + N_2 z^{-2} + N_3 z^{-3}}{D_0 + D_1 z^{-1} + D_2 z^{-2} + D_3 z^{-3}}$$

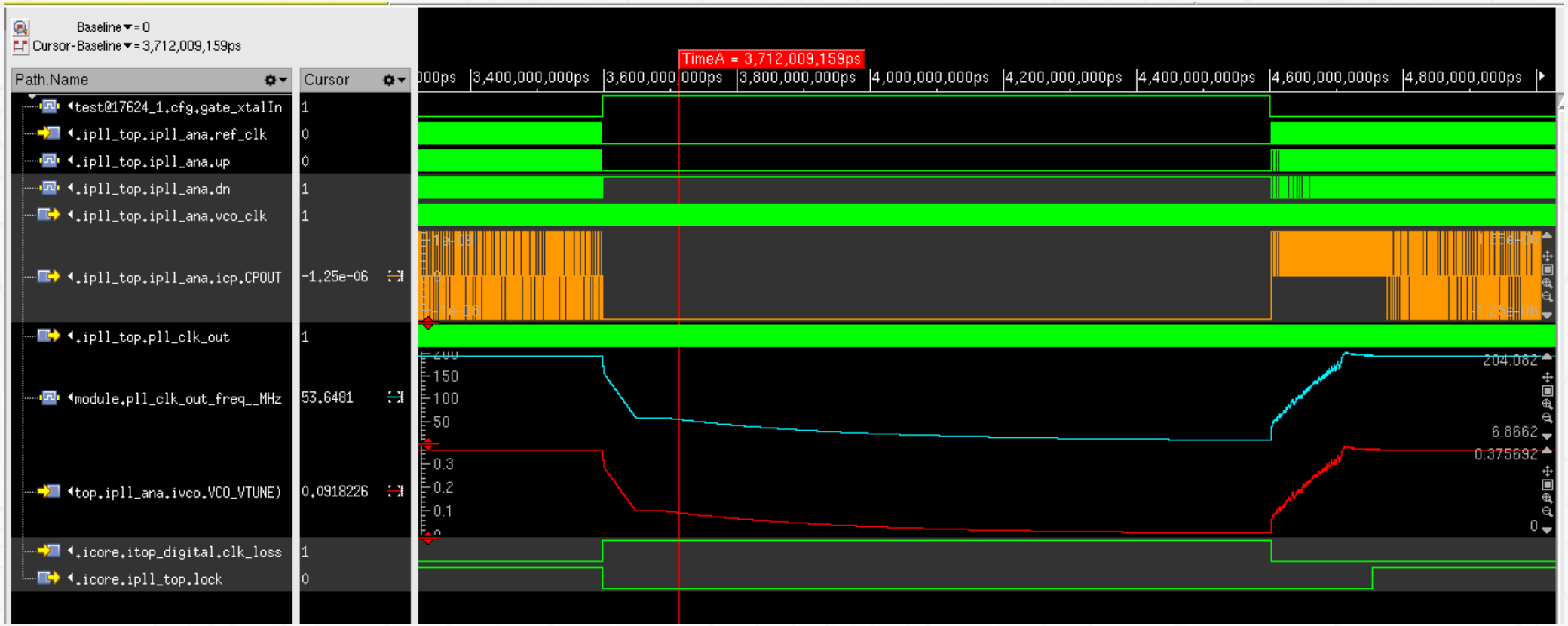
- Solve for the output new iteration value by realizing that z^{-1} is the unit delay operator

Visual Comparison of AMS and DMS Models



- DMS models of PLL block have about the same quality of AMS models.
  - Left: AMS model behavior. Right: DMS model behavior.
  - Top two traces are up (v(up)) and down (v(dn)) control signals from the phase detector.
  - The red trace is the VCO turning voltage control signal output from the loop filter.
  - From PLL enable (pll_en) to PLL lock (pll_lock), the two models spend about the same time.

A Case when Both V and I Needed



- A PLL test case that requires SV real net to have both voltage and current.
  - In the case of “clock loss”, the discharging current will gradually be turned off by sensing the voltage feedback

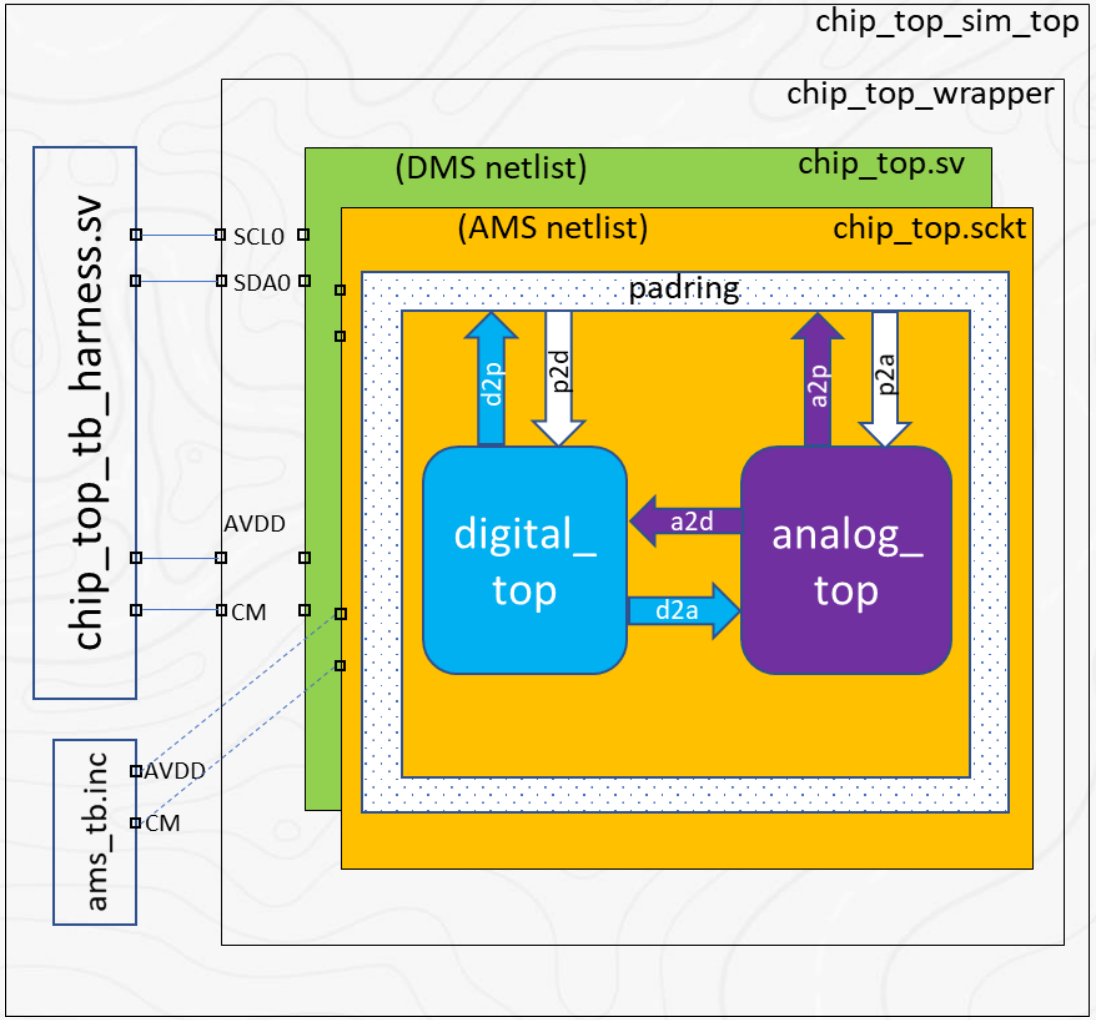
MSDV with a Hybrid Use of AMS and DMS Models

Blocks	DMS vs. AMS	Applications
Padring, Reference, Level Shifters, Crystal oscillator drivers	DMS 100% modeled (AMS 100%)	SVRNM models can be quickly developed for functionality and connectivity check
PLL	DMS 100% modeled (AMS 100%)	PLL has a significant digital design part that needs a full set of DMS model to facilitate digital design process and digital DV tasks.
Digital Powergen (LDO + charge pump regulator)	DMS 80% modeled (AMS 100%)	A detailed digital power supply generation from the LDO, together with the power-on-reset process are critical for digital DV's PMU verification and UPF based low power flow.
Analog Front End (AFE) (PGA + ADC)	DMS 60% modeled (AMS 100%)	More than 70% of verification tasks are using AMS models in the AMS flow, these include performance metrics, detailed clocking and control sequences, verification of digital islands.
Analog Back End (ABE) (DAC, class-D amplifier)	DMS 20% modeled (AMS 100%).	More than 90% of verification tasks are using AMS models with the AMS flow. As this block is from a silicon-proof design, digital verification requirement is largely reduced.

MSDV: Leveraging the Best of AMS and DMS

Tasks	Flow Choice
UVM testbench bring up with the first A-D integration	Use DMS because more relevant and efficient
Low-power simulation (LPS)	
Gate level simulation (GLS)	
Design for Test (DFT)	
A-D interface with Formal Verification	
Connectivity check	Use a combination of AMS and DMS depending on model availability and quality
Functional verification of design units with A-D interactions.	
Analog detailed behavior hard to capture or model in digital way	
Analog performance measurement	
Register map coverage	
Multiple power supplies or multi-level voltage domains verification	Use AMS as electrical simulation required
Device checking or safe operation area (SOA) check	
Full chip transistor-level sanity check test	

AMS and DMS Unified Under One Infrastructure



- MSDV focuses on
  - Padring (white frame)
  - Analog design blocks (analog_top, purple block)
  - Interfaces between analog and digital (a2d, d2a).
- AMS flow (orange):
  - AMS netlist (schematics, AMS models)
- DMS flow (green)
  - SV netlist with SV real number models
- AMS shares the same UVM infrastructure as DMS
  - Re-use digital test bench (chip_top_harness.sv)
  - AMS can have its own pure analog inputs (supplies, ADC inputs, etc.)

MSDV: A SPECIALIZED DISCIPLINE

- Only until recent years that MSDV has been identified as a separate and dedicated discipline
  - MSDV engineer as a new career path
  - A team of special work force that is capable of and responsible for the AMS and DMS workflows
- Common activities and responsibilities of an MSDV team:
  - Full-chip verification testbench creation.
  - Modeling of analog circuits.
  - Netlist release.
  - Test development.

Conclusions

- The popular industry adoption of DMS flow for the full chip functional verification does not imply that it is a full replacement of the AMS flow.
  - AMS was the only dominant flow at the early years of mixed-signal verification
  - DMS flow is unlikely to become the sole flow in MSDV, perhaps both AMS and DMS will co-exist for the foreseeable future.
  - At least, AMS flows are needed for DMS model validation process and in full chip transistor level verification (electrical sanity check for basic power up process).
- There is a trade-off between the time DMS models can save in simulation and the time for the models to be produced.
  - AMS models that are easier to develop or already available from an analog design team can compensate for the disadvantage of DMS models for the verification of detailed analog behavior and critical analog performance.
- MSDV, comprising of AMS and DMS, is becoming an emerging separate discipline that requires
  - solid understanding of analog design
  - good experience in the state-of-art digital verification methodologies.

Acknowledgment

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Questions?