2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Machine Learning Based Verification Planning M ethodology Using Design and Verification Data

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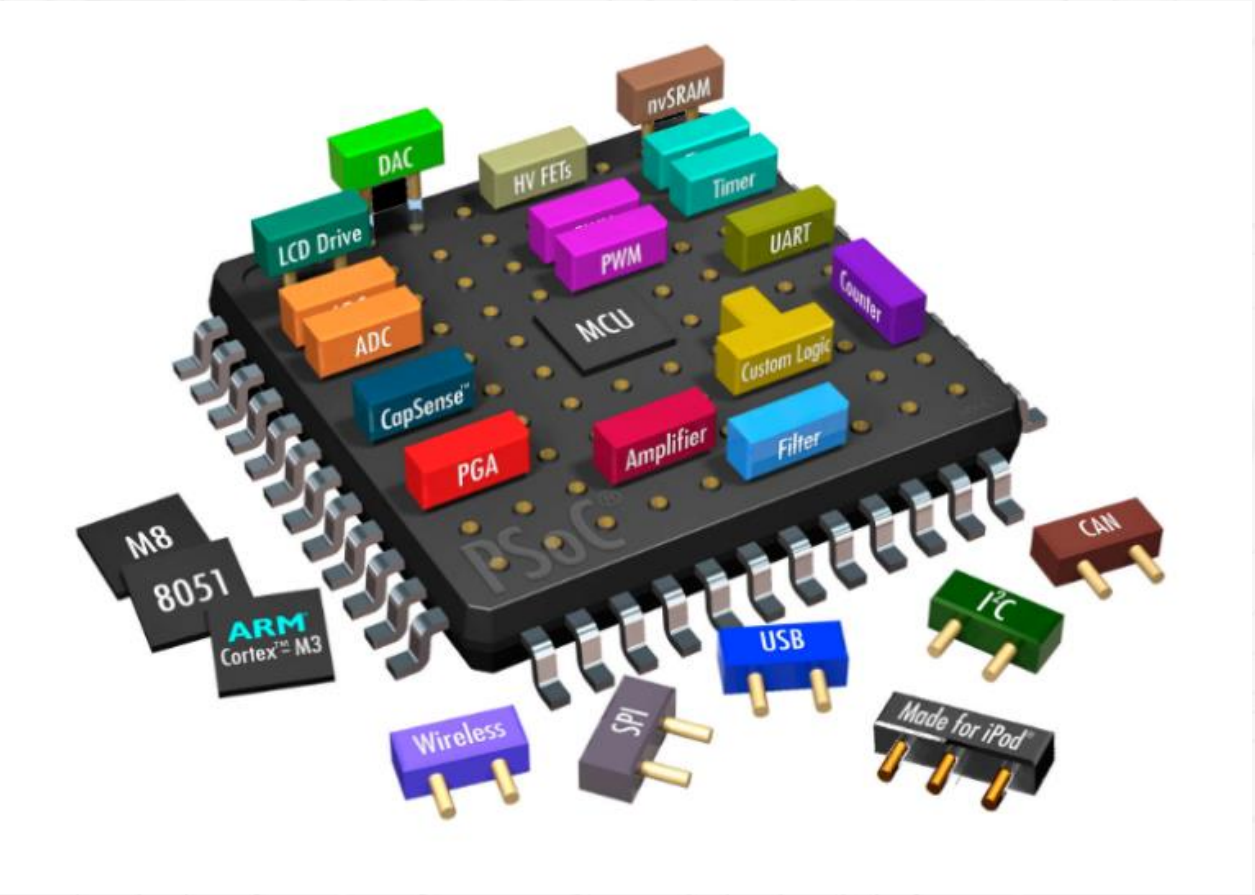
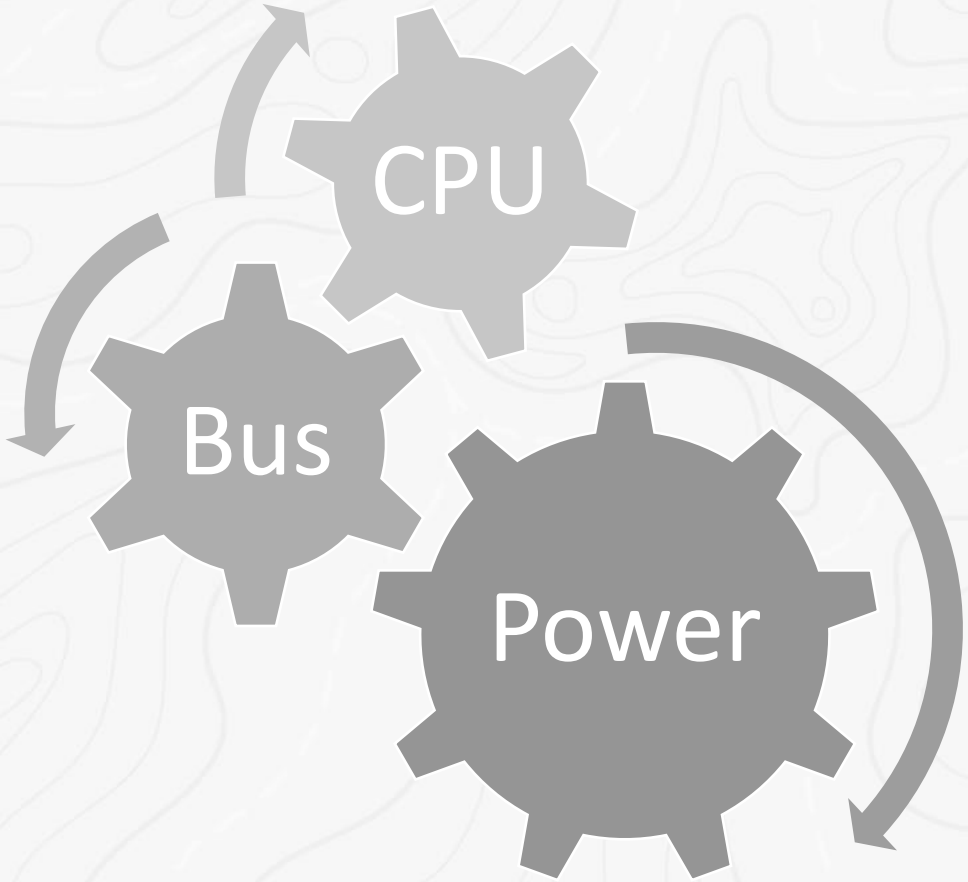
accellera SYSTEMS INITIATIVE

Various and complicate

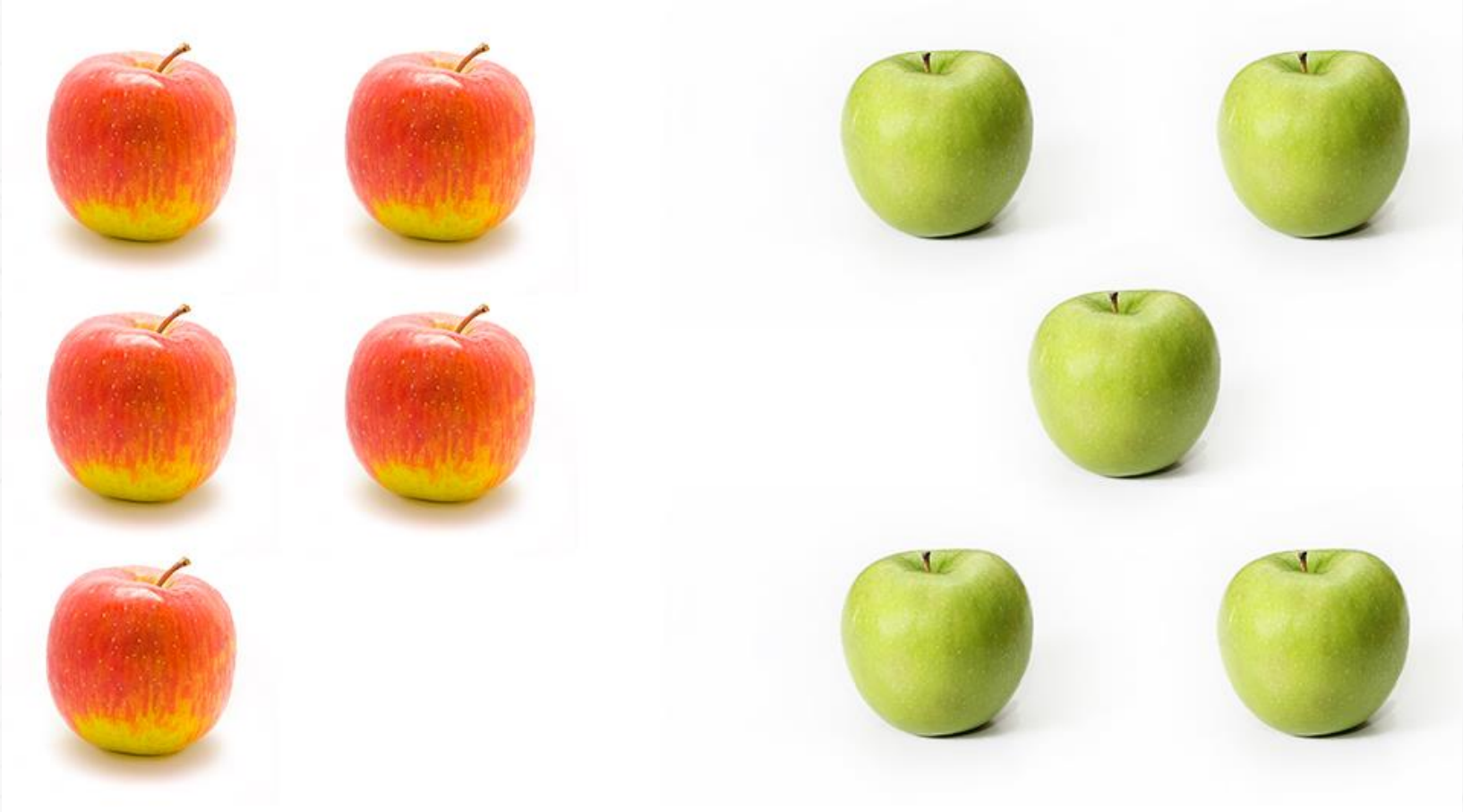


https://m.post.naver.com/viewer/postView.naver?volumeNo=8860727&memberNo=1834

Communicate with data

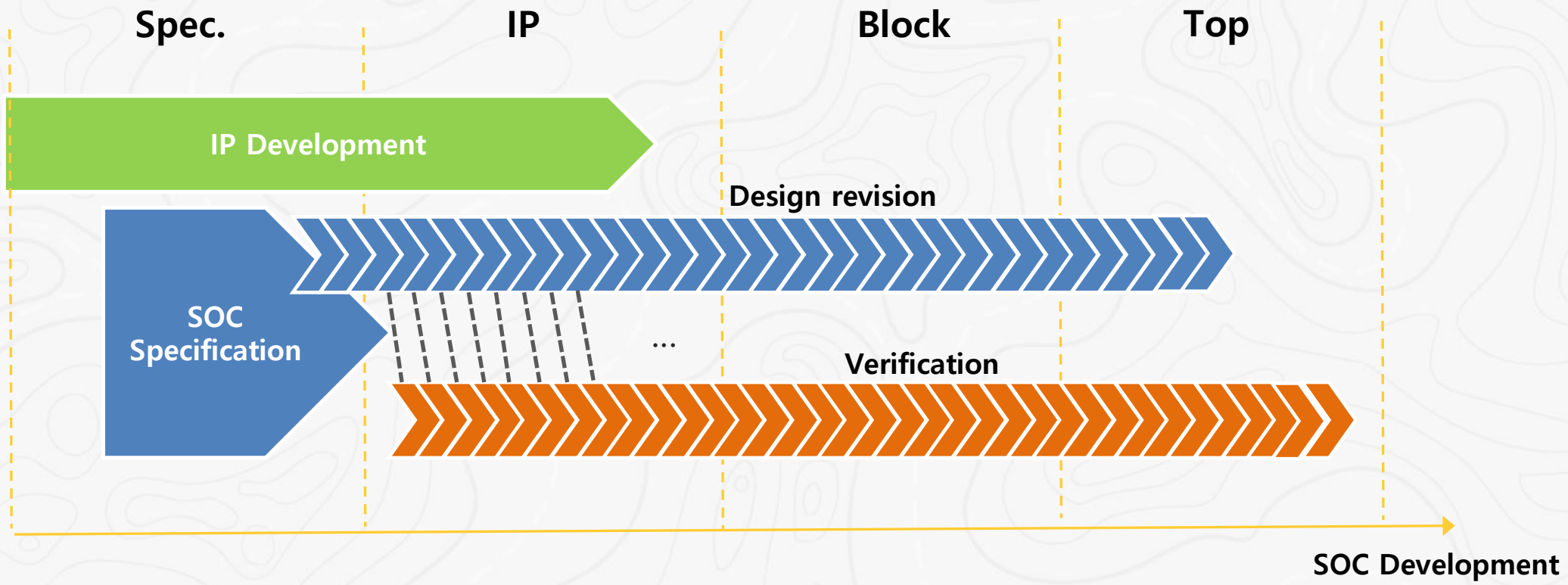


Same but different : Design and Verification

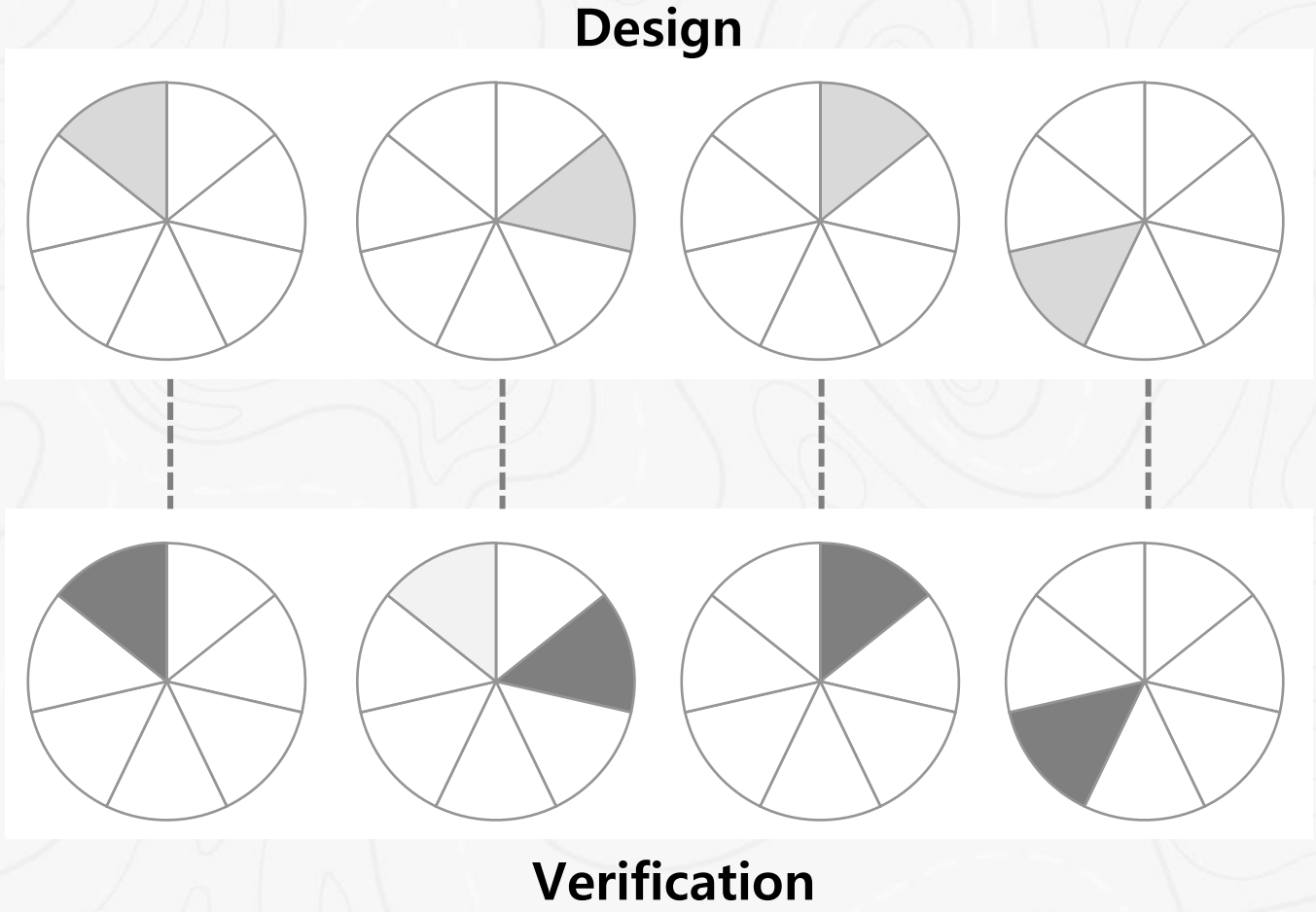


https://www.samebutdifferentmath.com/early-numeracy

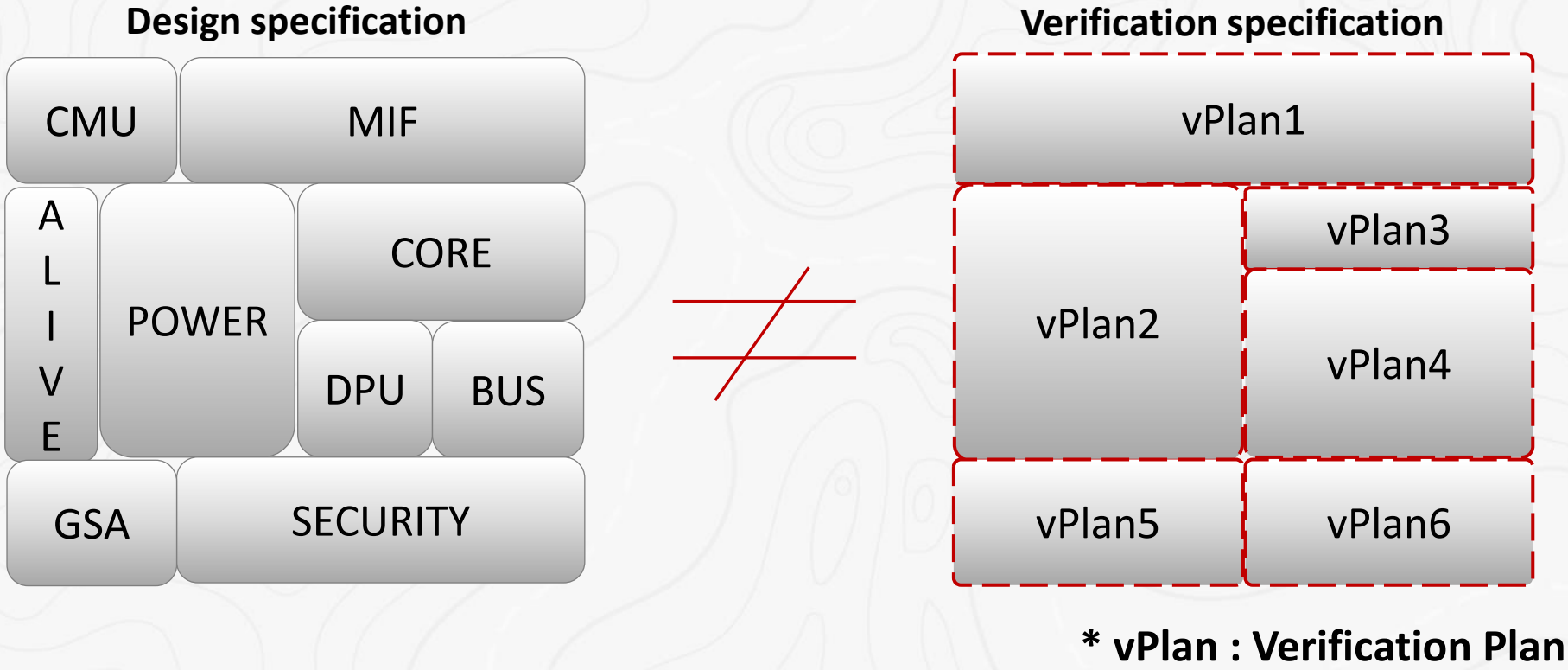
How can find faster?



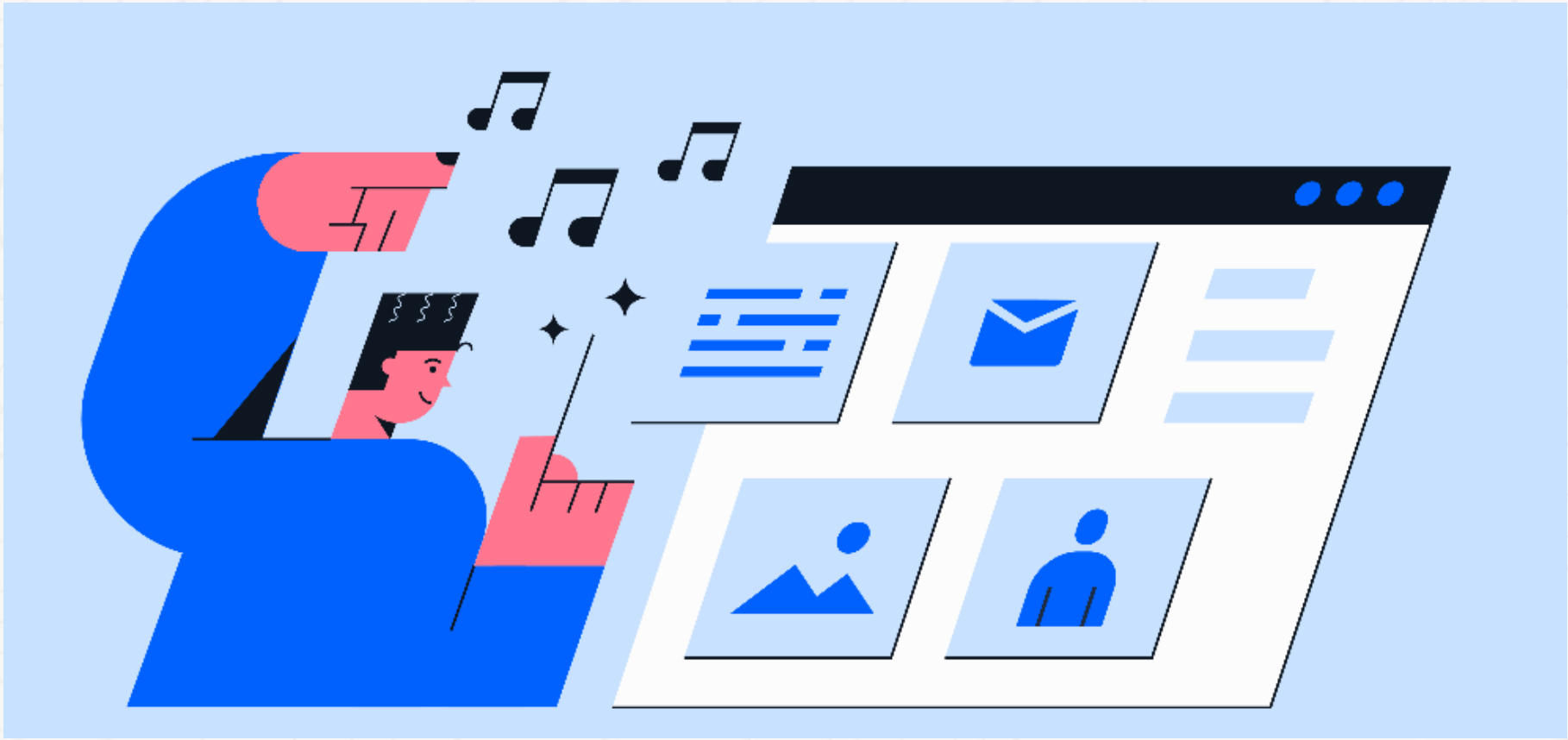
Focus on difference



Plan between Design and Verification

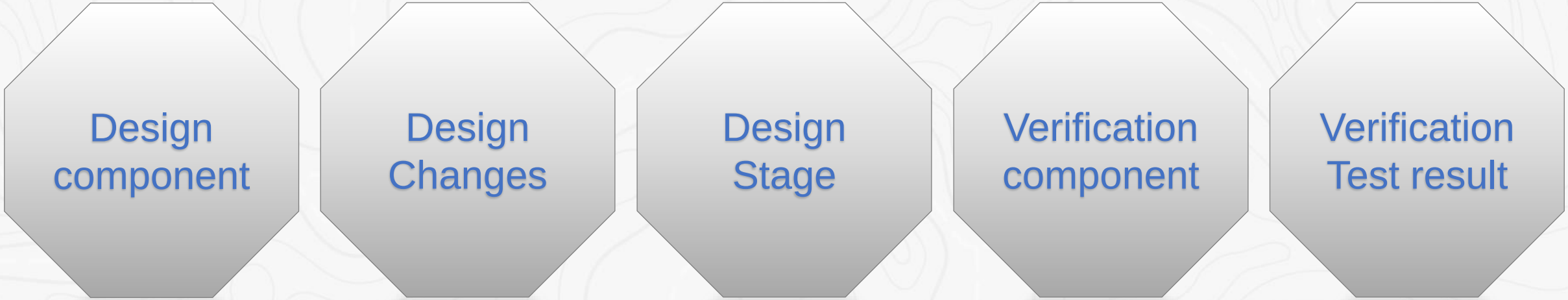


Data orchestration : Using ML



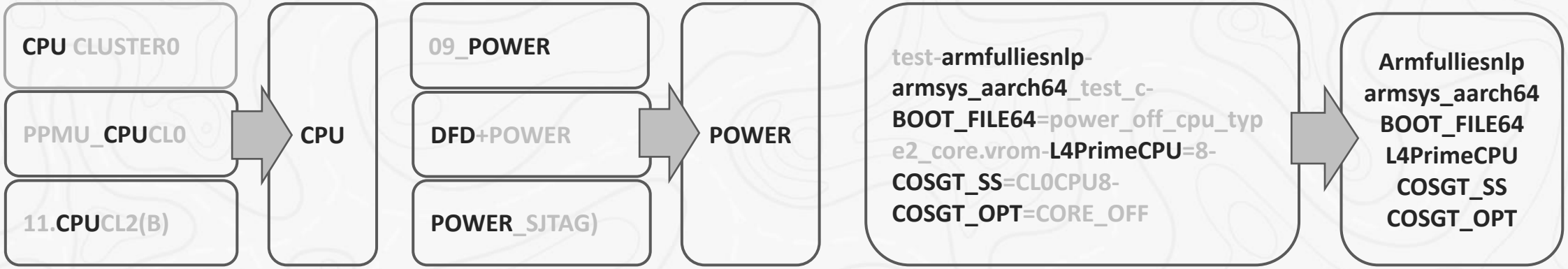
https://blog.stackadapt.com/data-orchestration/

Data for analysis



Data pre-processing

- Hash mapping and cleaning

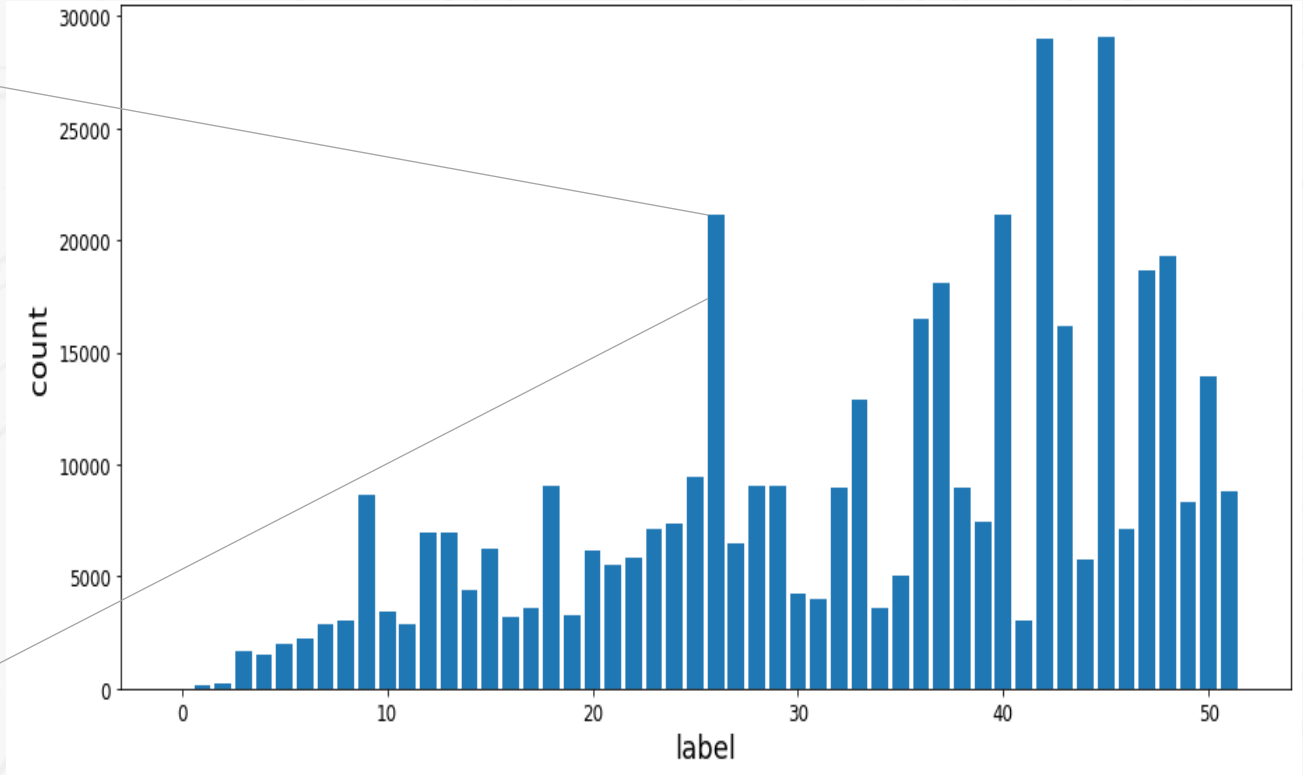


- Vectorize

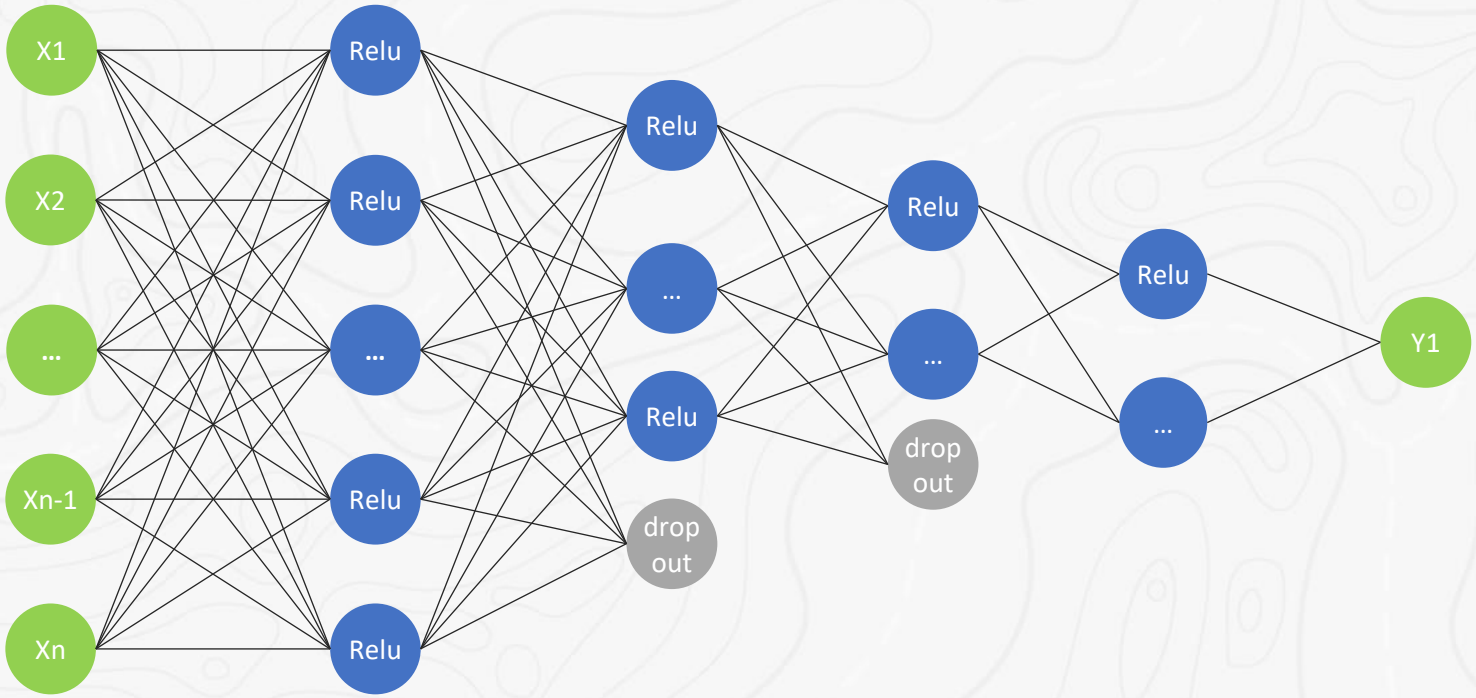
aarch	abox	acc	access	addr	aes	…	alive	ap	apg	apm	armsys	aspm	Run_time
0	0	0	0.213673	0	0	…	0	0.357441	0.370710	0	0	0	229.79
0	0	0	0	0	0	…	0	0	0	0	0.23861	0	427.73
…	…	…	…	…	…	…	…	…	…	…	..	…	…
0.187469	0	0	0	0	0	…	0	0	0.571612	0	0	0	89.44
0	0	0.165631	0	0	0	…	0	0	0	0	0	0	16.81

Clustering result

15142	CTRL CLOCK HSI USBCADHOST USBCADHOST USB B...	26
15188	USBLINK CLOCK HSI USBCADDEV USBCADDEV USB ...	26
15191	USBLINK CLOCK HSI USBCADHOST USBCADHOST USB ...	26
15257	HSI CORE HSI USB USB USB BASIC USB ...	26
15258	HSI CORE HSI USBCADDEV USBCADDEV USB BASI...	26
15260	HSI CORE HSI USBCADDEV USBCADDEV USB BASI...	26
15262	HSI CORE HSI USB USB USB BASIC USB ...	26
15303	USB DRD REGISTER ACCESS HSI HSI HSI COMMO...	26
16913	USBDPPHY POWER HSI USBCADHOST CPUSTUBIESNLP ...	26
16914	USBDPPHY POWER HSI USB DEV CPUSTUBIESNLP US...	26

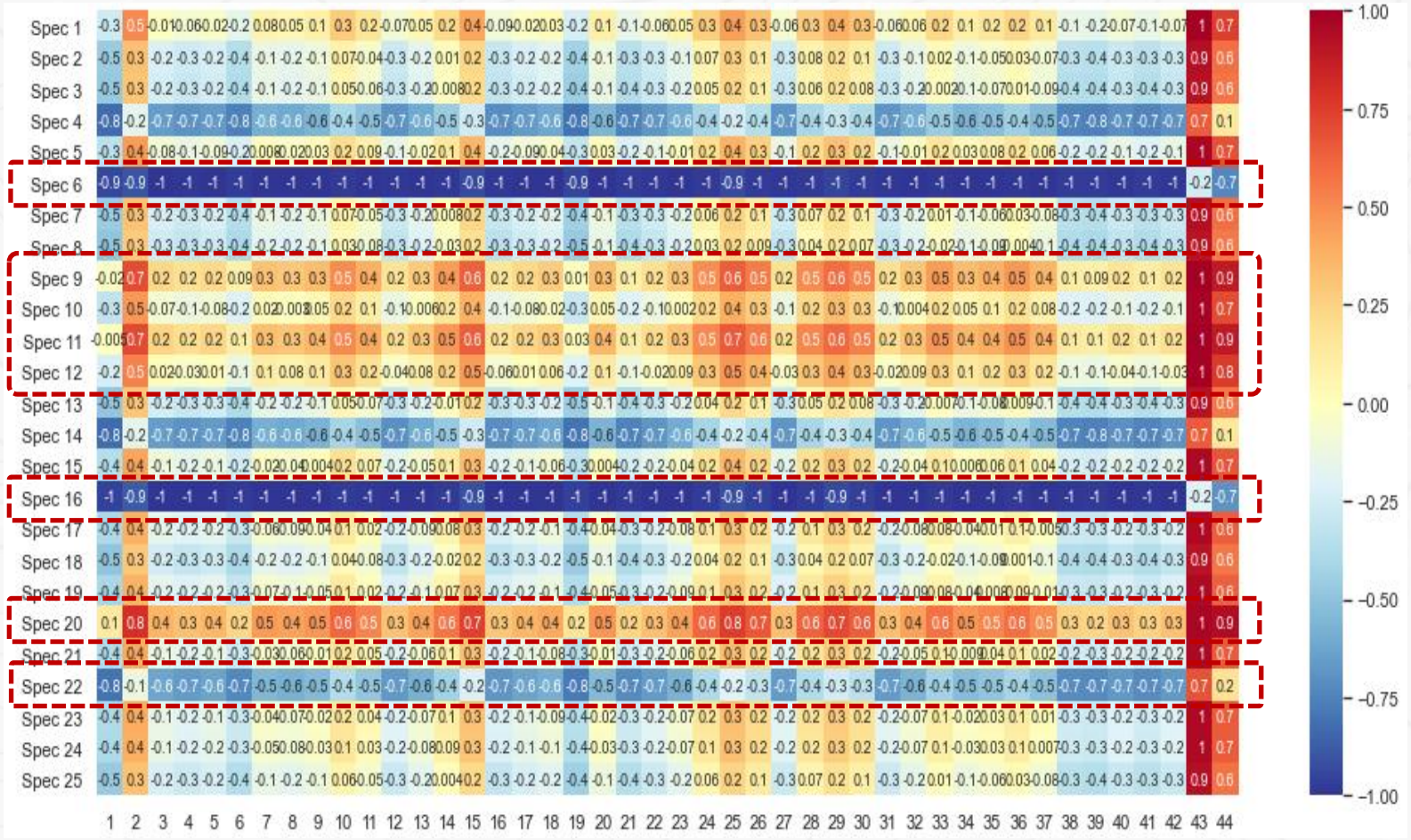


Verification test classification model



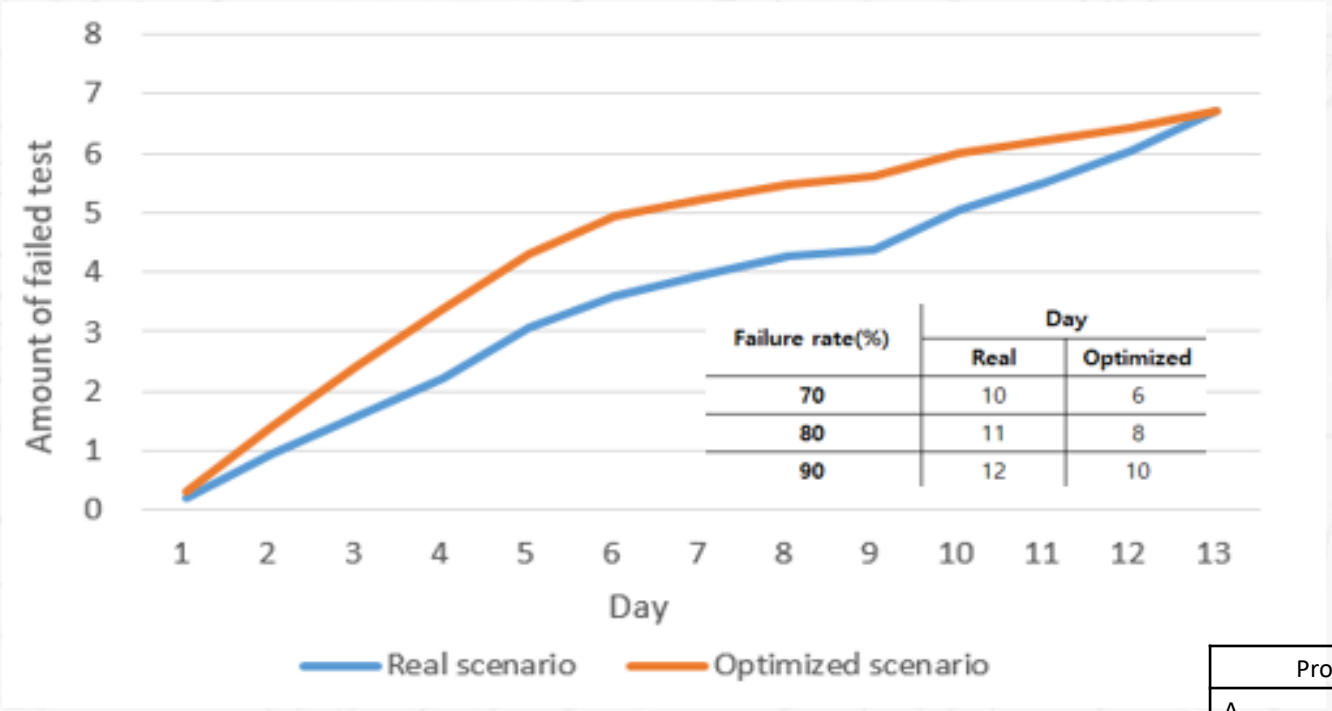
AI Algorithm	Deep learning
epoch	500
Learning rate	0.001
Batch	512
Activation function	Relu
Optimizer	AdamW
Accuracy	31/35

Design & Verification correlation analysis



Class Order	Verification Stage		
	VL2	VL3	VL4
1	43	19	34
2	44	1	4
3	2	13	37
4	25	44	24
5	15	35	1
6	29	5	15
7	26	18	31
8	30	22	23
9	14	28	17
10	28	17	7
11	10	8	20
12	33	12	6
13	24	42	32
14	36	36	36
15	35	4	38
16	11	10	21
17	37	16	19
18	34	40	39
19	20	9	29
20	9	2	18

Experimental result



Failure rate(%)	Day	
	Real	Optimized
70	10	6
80	11	8
90	12	10

Project	SOC Complexity	DV Silicon Bug KPI
A	0.52	11.5
B	0.88	5.7
C	1.00	n/a
D	0.67	11.9
E	**0.65**	**0.0**

Conclusion

- Goal
  - Shortening TAT and improving completeness on verification
- Idea
  - The failure pattern generated at each design stage is similar for each project
- Result
  - A verification plan can be established by defining a class using machine learning and failure can be detected early
- additional research
  - Preserve more data
  - Maximize machine learning model performance

Thank you