The CHIPS ACT and Its Impact On The Design & Verification Markets

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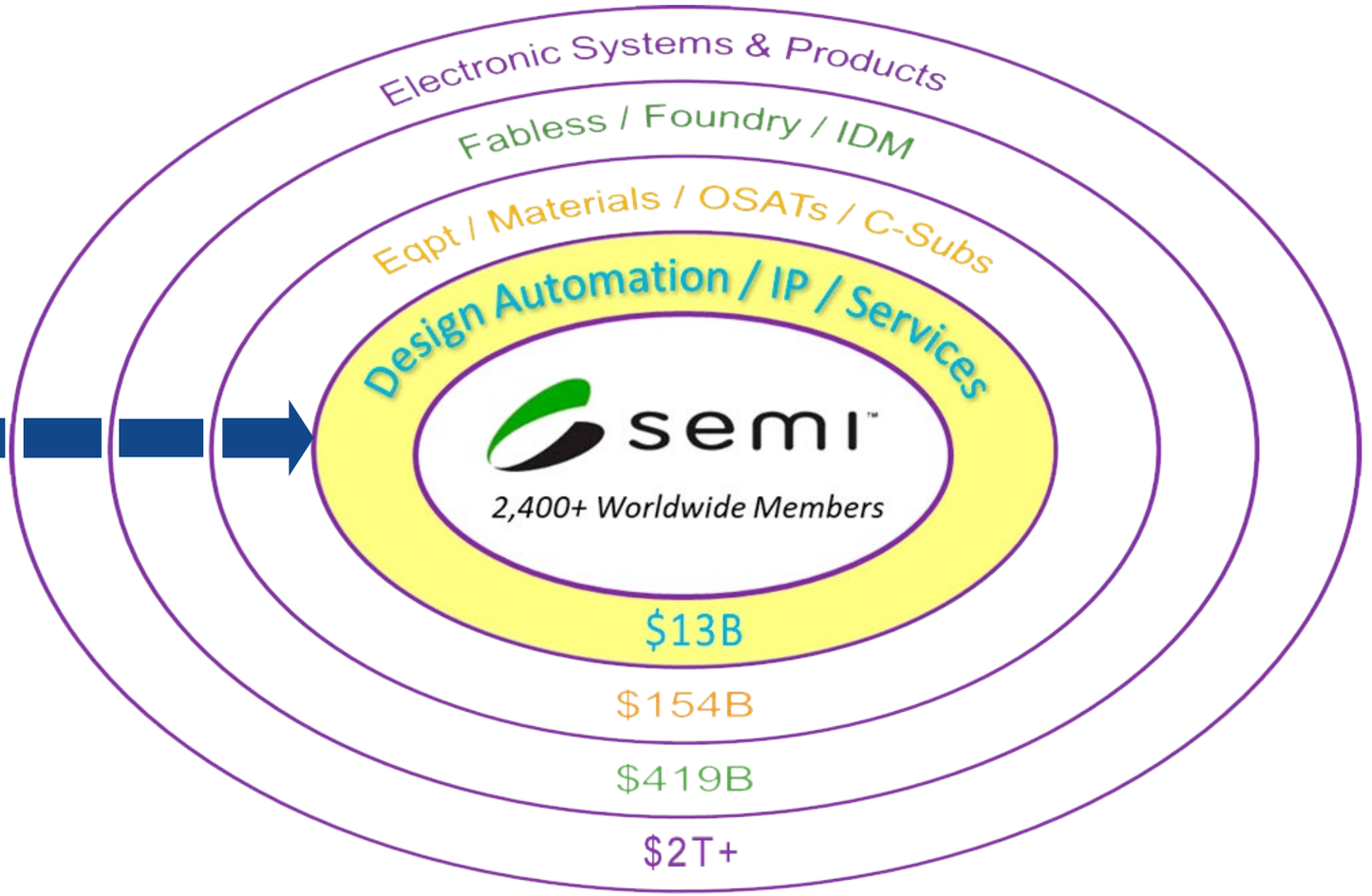
Agenda

- The Design Ecosystem
- Background Info
  - What is the CHIPS Act?
  - What is the mission and scope?
  - Where is the funding being allocated?
- Commerce, NSTC and the IAC
  - What roles do they play?
- Where does the Design Ecosystem fit?
  - Opportunities

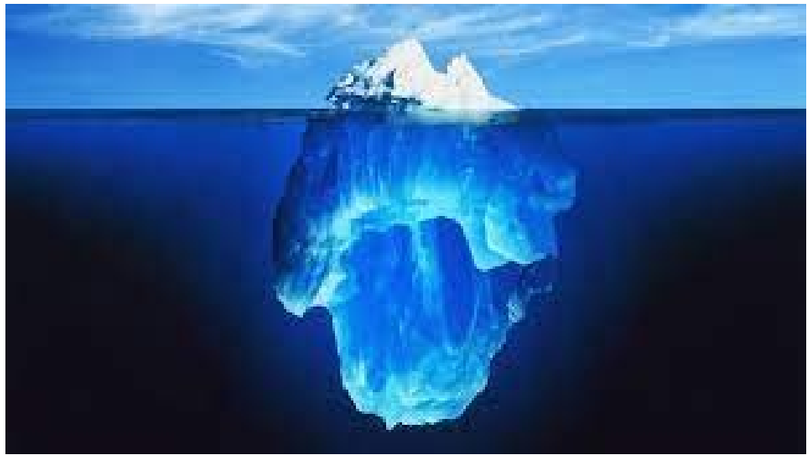
The Design Ecosystem

Electronic System Design Alliance

A SEMI Technology Community



Disclaimer



- Not affiliated directly with the activities going on under the CHIPS Act
- My opinions and observations are based solely on publicly available documents and data
- Your mileage may vary!

What Is the “CHIPS Act?”

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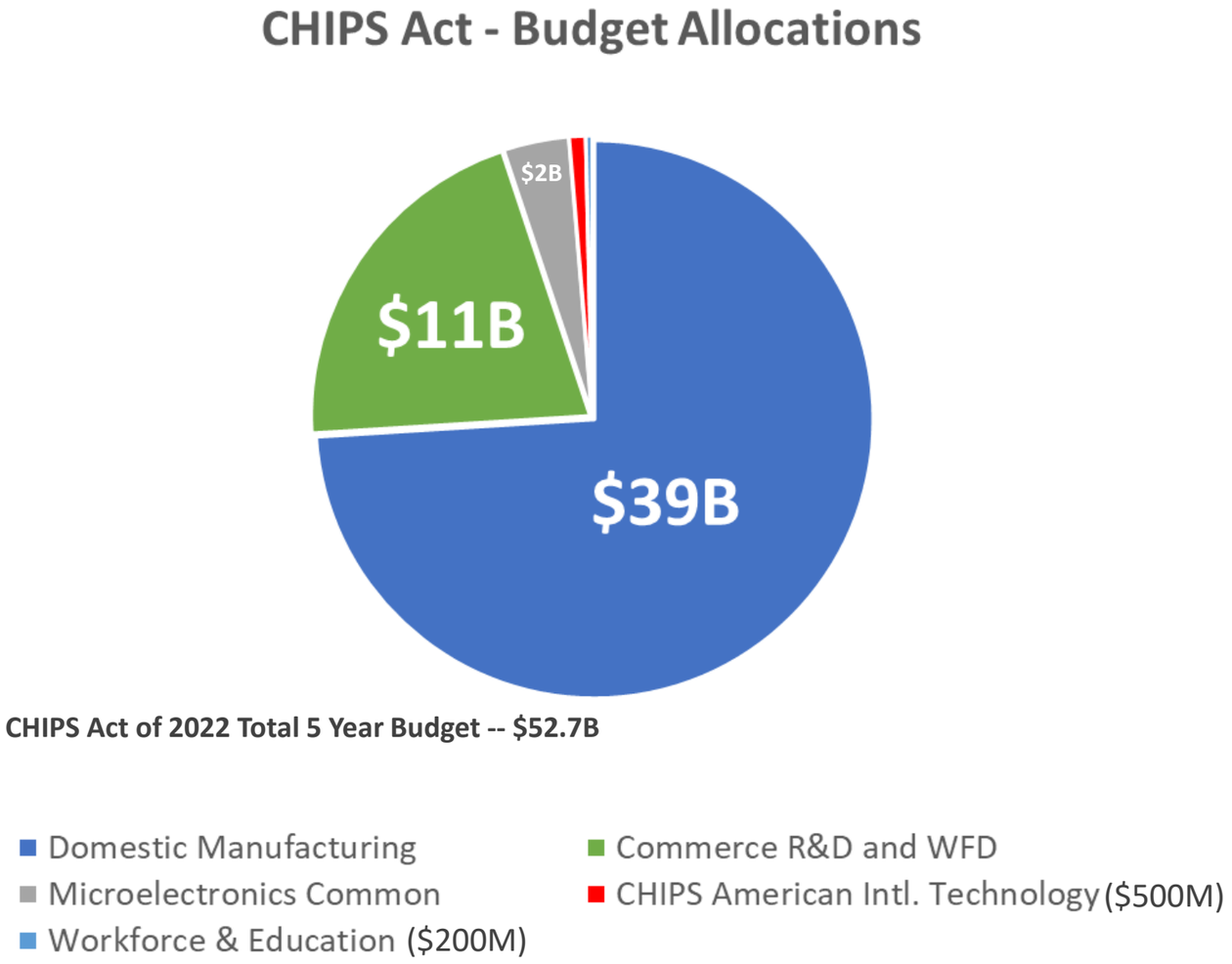
- Acronym: **C**reating **H**elpful **I**ncentives to **P**roduce **S**emiconductors
- Official Name: CHIPS and Science Act of 2022
  - Short name: CHIPS Act of 2022
- The CHIPS Act was signed into law in August, 2022

Mission and Priorities

- **Strengthen & Revitalize …**
  - Semiconductor R&D
  - Semiconductor manufacturing
  - Investment in American workers
- **Priorities**
  - Meet economic and national security needs
  - Ensure long term leadership in the sector
  - Strengthen and expand regional clusters
  - Catalyze private sector investment
  - Generate benefits for a broad range of stakeholders and communities
  - Protect taxpayer dollars

Follow the Money …



Domestic Manufacturing

- Incentives to develop domestic semiconductor manufacturing including “legacy” chip production

Commerce R&D and Workforce Development

- National Semiconductor Technology Center
- National Advanced Packaging Manufacturing
- Other R&D and Workforce Development Programs

Microelectronics Common (CHIPS for America Defense Fund)

- University-based prototype to fab semiconductor technology transition
- DoD unique applications
- Workforce training

CHIPS for America International Technology Security and Innovation Fund

- Coordinate with foreign govts. to coordinate security, supply chain and communications

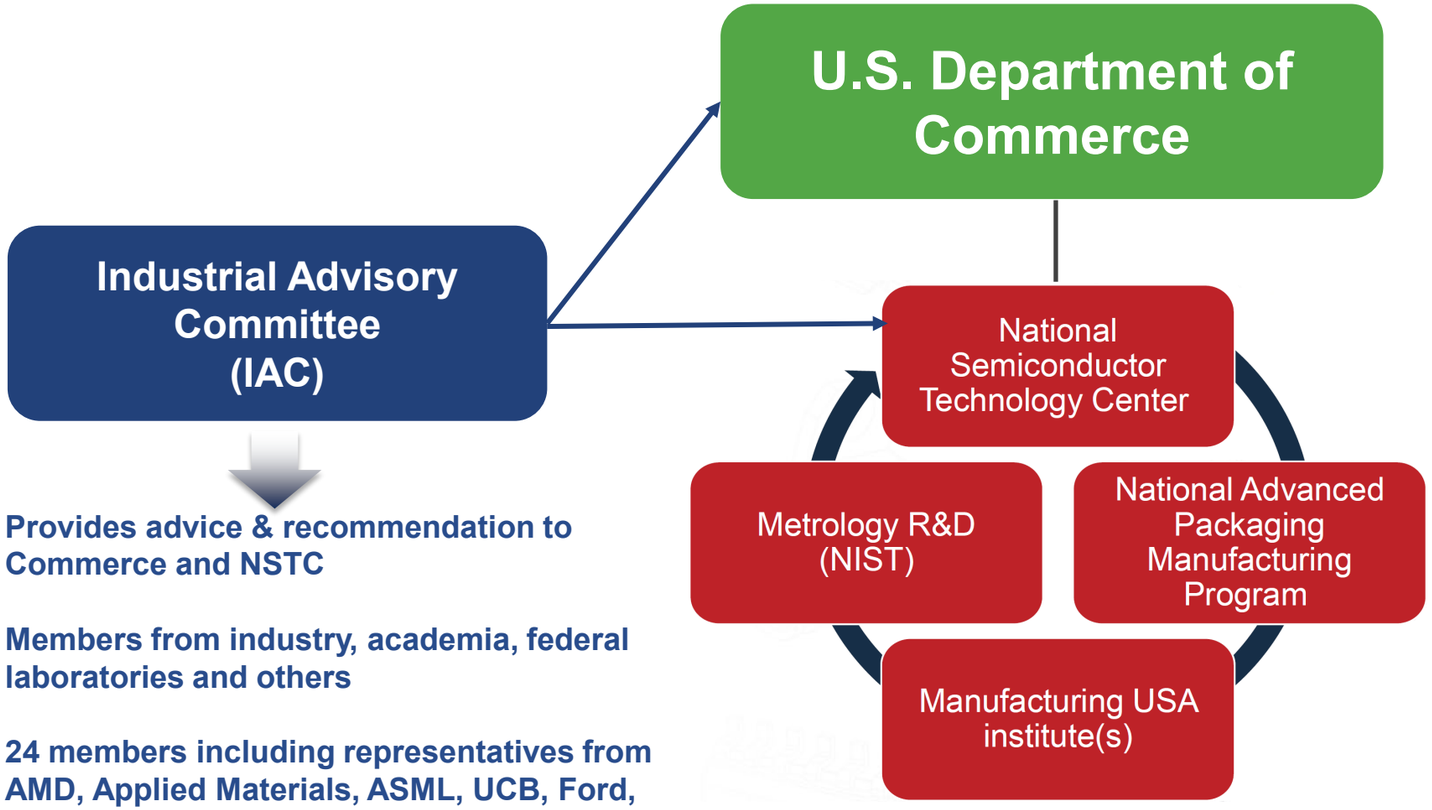
CHIPS for America Workforce and Education Fund

- 90,000 new domestic workers needed by 2025

Where Do Design & Verification Fit In?

- The CHIPS Act of 2022 (full text)
- Document search results for design ecosystem terms
  - Verification – 0
  - EDA – 0
  - Design automation – 0
  - Automation – 0
  - Intellectual property – 1 (but in a context unrelated to our industry)
- Other search results
  - Manufacturing – 39
  - Space – 33
  - Semiconductor – 23
  - Materials – 11
  - Mars – 6
  - Moon – 5
  - Supreme Court – 2

Dig Deeper …



- **Provides advice & recommendation to Commerce and NSTC**
- **Members from industry, academia, federal laboratories and others**
- **24 members including representatives from AMD, Applied Materials, ASML, UCB, Ford, Intel, Micron, Microsoft, Stanford, Synopsys, Texas Instruments, …**

NSTC

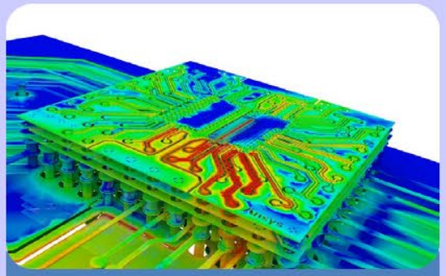
Vision: Will serve as the focal point for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.

NAPMP

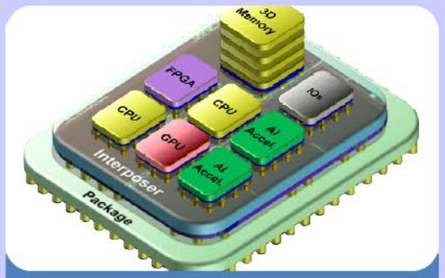
Vision: Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem. Includes ***heterogeneous integration***, ***tooling and automation***, wafer/panel and substrate technology.

Getting Closer

- **NAPMP Target Areas**

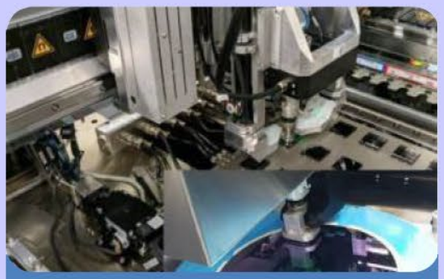


Co-design and simulation

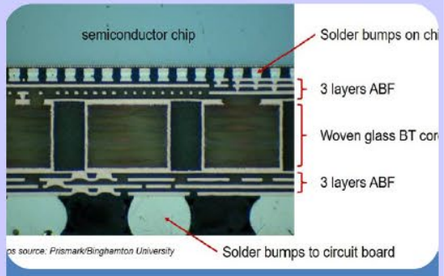


Chiplets

Pilot packaging facilities



Tooling and automation

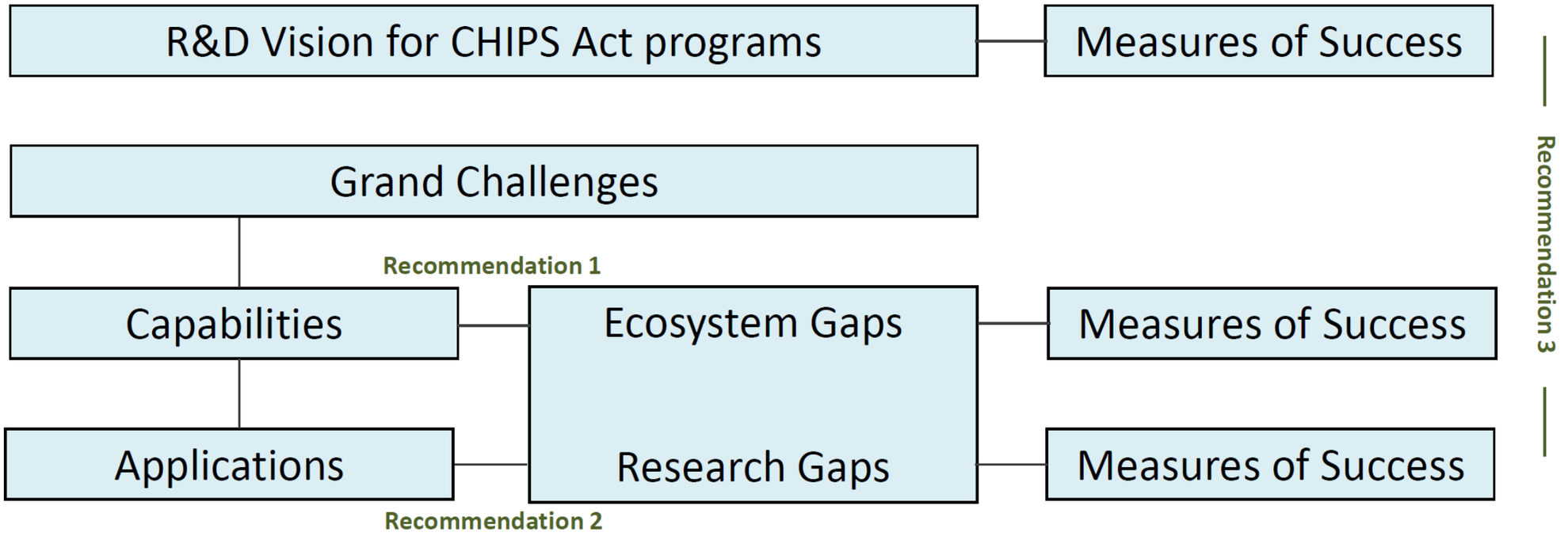


Materials and substrates

Source: Update on CHIPS Research and Development; IAC Meeting, Feb-7-2023

IAC Recommendations

- **IAC R&D Gaps Working Group - Framework**



Source: Presentation from R&D Gaps Working Group; IAC Meeting, Feb-7-2023

IAC Recommendations

- **Recommendation 1**

1) Establish easily accessible prototyping capabilities in multiple facilities and enact the ability to rapidly try out CMOS+X at a scale that is relevant to industry

2) Create a semiverse digital twin

3) Establish chiplets ecosystem and 3D heterogeneous integration platform for chiplet innovation and advanced packaging

4) Build an accessible platform for chip design and enable new EDA tools that treat 3D (monolithic or stacked) as an intrinsic assumption

5) Create a nurturing ecosystem for promising startups

Source: Presentation from R&D Gaps Working Group; IAC Meeting, Feb-7-2023

Conclusion Caveats

- The IAC's role is to provide input and make recommendations
  - The IAC does not make policy or rules – it is only an advisory body
  - But, the IAC clearly recognizes the need for new design and verification automation tools that will be needed to support the missions of the NSTC and NAPMP (among others)
- First order effects
  - Direct effects that the CHIPS Act would have on the design ecosystem (EDA, IP, etc.)
- Second order effects
  - Positive benefits and opportunities that arise from the U.S. focus on re-tooling domestic semiconductor manufacturing capabilities

Conclusions

- **First order effects**
  - The CHIPS Act recognizes that the future of semiconductor design is moving to chiplets and heterogeneous integration
  - The need for new automation tools for design and verification is clearly recognized as being essential
  - Opportunity exists for new technologies and commercial solutions

- **Important to follow the direction of the NSTC (hub for CHIPS Act activities and organizations) and the NAPMP**
  - Join the mailing list for the CHIPS Act – stay informed

CHIPS for AMERICA

https://www.nist.gov/chips

Conclusions

- **Potential second order effects**
  - **WFD programs should help address the chronic shortage of talent across our industry**
  - **Expansion of domestic manufacturing capability should lead to more on-shoring of design activities which would require automation tools**
  - **R&D programs in various projects under the CHIPS Act/NSTC will require tools and may offer partnerships or collaboration to solve critical challenges in advancing the state of the art**
  - **There are likely many others since the scope of the CHIPS Act is so broad**

THANK YOU!