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Left shift catching of critical low power bugs with Formal Verification

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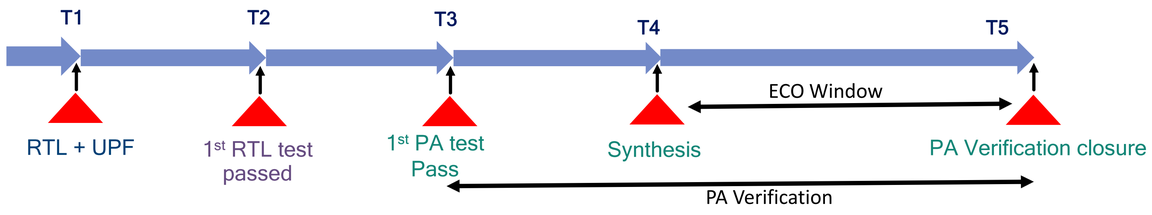
Problem Statement/Introduction

- ❑ With increasing complexity of power-aware designs (100+ collapsible domains), it is challenging to validate all the power features within project timelines.
- ❑ PA simulation is delayed due to prerequisites - Passing RTL sims, and PA TB developed
- ❑ Creating Power aware TB is resource and time consuming



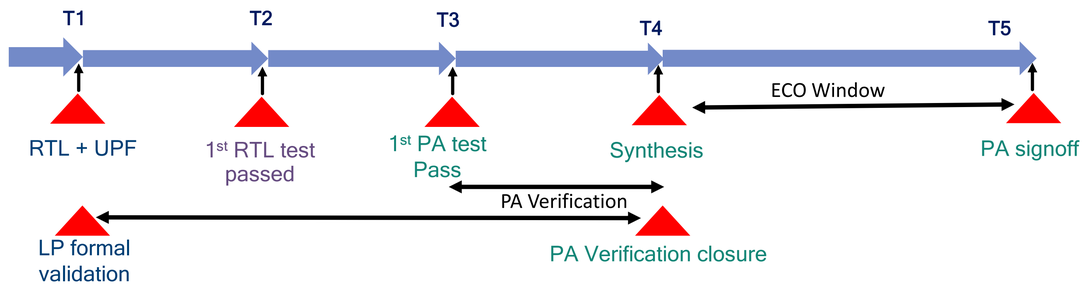
- ❑ PA testcases at SOCs take days to complete
- ❑ Difficult for PA verification test suite to ensure completeness
- ❑ Late verification in low power often leads to costlier ECOs
- ❑ Need for methodologies that addresses current challenges in PA verification

Proposed Methodology

- ❑ Enablement of Formal methodologies for low power verification
- ❑ Verification of power aware checks using formal
- ❑ Verification of custom checks for low power elements(isolations, retentions) using information model

Advantages:

- ✓ Early interception: Formal flows for low power can be enabled as soon as RTL+UPF is available

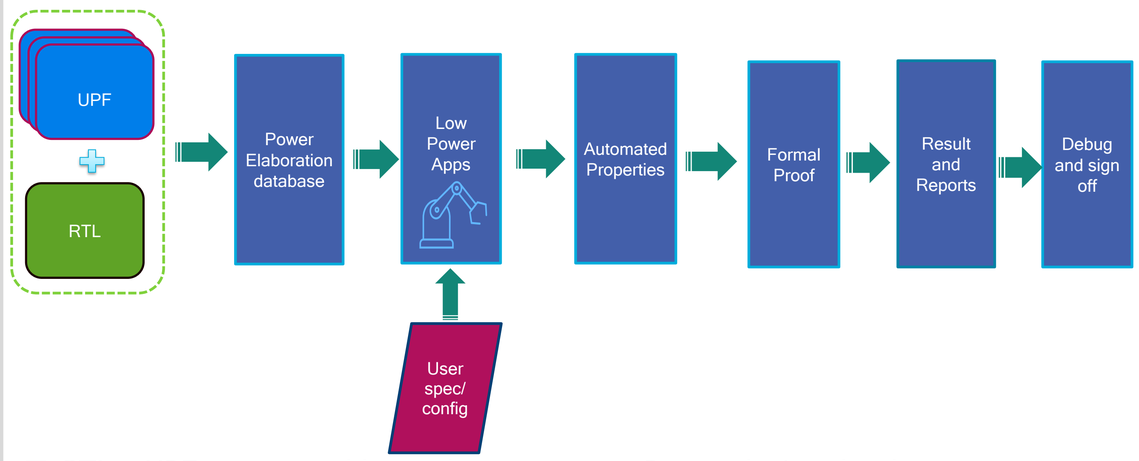


- ✓ Bugs caught even before PA TB is developed
- ✓ Highly mature low power design available for PA sims
- ✓ Reduction of costly ECOs

Methodology evolution/Challenges

1. Collaboration with vendors to support UPF and liberty constructs
2. Formal tools should adapt to continuously evolving UPF constructs
3. Scalability is a challenges for bigger SOCs – optimizations done to restrict compute requirements to an acceptable limit
4. Worked with vendors to model connectivity scenarios in low power
5. Collaboration with vendors to define and validate information model support.
6. Formal COI complexity on bigger SOCs was addressed. Scope for more improvement

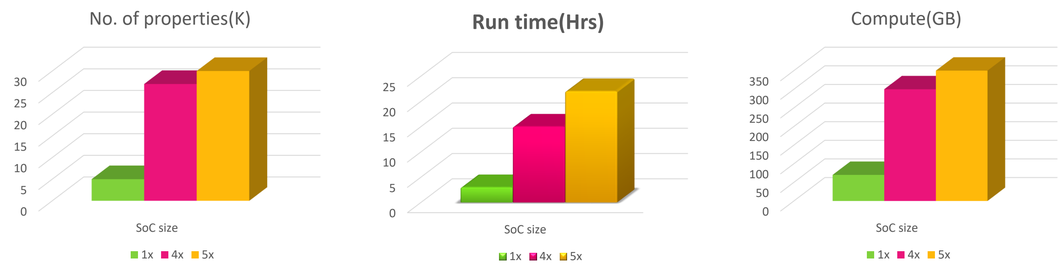
Implementation Details



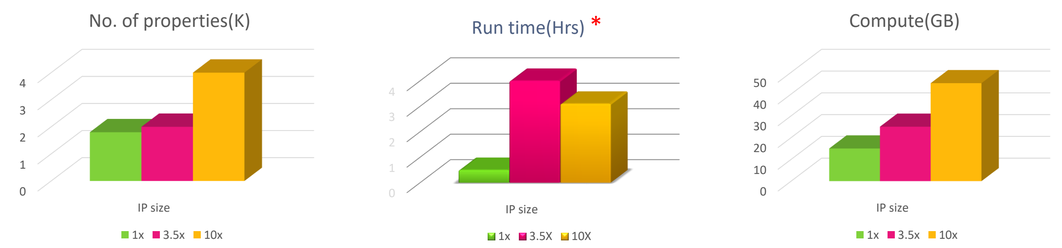
- ❑ RTL + UPFs processed by tools to generate Power design database
- ❑ Automated SVA properties using information model query APIs
- ❑ Power aware connectivity models for SoC integration scenarios
- ❑ User friendly configuration and reporting formats

Results Table

Connectivity checks



Auto checks



Conclusion

- Formal validation of low power. Powerful information model checks
- Early enablement – Reduction of ECOs
- Improved UPF quality through exhaustive checks
- Reduced effort in PA verification closure
- Move towards formal low power signoff

REFERENCES

IEEE Standard for Design and Verification of Low-Power, Energy-Aware Electronic Systems, IEEE Std 1801™-2015