Leaping Left: Seamless IP to SoC Hand-off

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Agenda

• Problem Statement
• Packaging Options Explored
• Packaging Objectives
• Inner Workings: Export_IP QA + Orion QC
• Challenges & Solutions
• Results
• In Conclusion...
• Questions?
Problem Statement

Integrating Graphics IPs into SoC would take up to 4 weeks per IP drop

• Too many integration bugs! Lack of standard flow, inefficient package generation
• Long TTM due to undocumented hacks/workarounds
• Non-existent IP QA/QC infrastructure

End Goal: Continuous Integration + Refined TFM = 3 days per IP drop
Packaging Options Explored...

Legacy IP Packaging
- Pros: Extensive customization, Easy to incorporate SoC feedback
- Cons: Minimal standardization, Heavily tied to TFM

Export_to_SoC
- Pros: Better centralization, Improved package structure
- Cons: Expensive customization, Heavily tied to TFM again

Lack of Portability & Quality Assurance = High Integration Bugs and TTM
Packaging Objectives

- Quality
- Scalable
- TFM Agnostic
- Small TTM

- Compiles Standalone
- Self Contained Package
- Meets IPSOC Handoff criteria

Balance of Customization & Standardization, with Uncompromising Quality
Inner Workings : Export_IP & QA

Key Takeaways

- Industry Standard
- HIP and SIP Compliant
- Rigorous Quality Checks
- Always-alive through Continuous Integration
- Excellent Collaboration between IP, TFM, SoC
Inner Workings : Orion QC

<table>
<thead>
<tr>
<th>Category</th>
<th>Intent</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front-End</td>
<td>Basic VCS elaboration checks, illegal cells, macro definition, illegal macro usage</td>
</tr>
<tr>
<td>Back-End</td>
<td>No interface level latches, no undriven pins, CTECH compliance</td>
</tr>
<tr>
<td>Soft IP Compliance</td>
<td>Usage of global macros or vendor-specific macros, LRM compliance</td>
</tr>
<tr>
<td>Emulation</td>
<td>Multi-platform compliant (Zebu, Veloce, etc.)</td>
</tr>
<tr>
<td>File Existence</td>
<td>Additional/meta files (CDC abstracts, Lint reports, Integration guides, etc)</td>
</tr>
<tr>
<td>Custom</td>
<td>Unique IP specific checks per IP &amp; SoC requirements</td>
</tr>
</tbody>
</table>
Challenges & Solutions

Large IPs size affecting compute efficiency

Build and validate on tmp disk to limit file I/O

High TAT due to elaboration dependencies

Smart build of necessary dependencies and parallelizing various independent checks

Unwarranted RTL & Val inter-dependability

Separation with flattened RTL library and a library for RTL + Validation

Lack of reusable features

Consolidate and streamline common features across IPs and house in central release area
### Challenges & Solutions - Improvements

#### Compute Efficiency and Parallelization

<table>
<thead>
<tr>
<th>IP</th>
<th>Previous</th>
<th>Current</th>
<th>% Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display</td>
<td>58 min</td>
<td>24 min</td>
<td>59%</td>
</tr>
<tr>
<td>Media</td>
<td>164 min</td>
<td>117 min</td>
<td>29%</td>
</tr>
<tr>
<td>GPU</td>
<td>363 min</td>
<td>280 min</td>
<td>22%</td>
</tr>
</tbody>
</table>

#### Smart Build

<table>
<thead>
<tr>
<th>IP</th>
<th>Previous</th>
<th>Current</th>
<th>% Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display</td>
<td>86 min</td>
<td>29 min</td>
<td>66%</td>
</tr>
<tr>
<td>Media</td>
<td>104 min</td>
<td>60 min</td>
<td>42%</td>
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</tbody>
</table>

#### Consolidated Enhancements

<table>
<thead>
<tr>
<th>IP</th>
<th>Previous</th>
<th>Current</th>
<th>% Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display</td>
<td>137 min</td>
<td>53 min</td>
<td>61%</td>
</tr>
<tr>
<td>Media</td>
<td>268 min</td>
<td>104 min</td>
<td>61%</td>
</tr>
<tr>
<td>GPU</td>
<td>490 min</td>
<td>407 min</td>
<td>17%</td>
</tr>
</tbody>
</table>
## Results

<table>
<thead>
<tr>
<th>Domain</th>
<th>IP</th>
<th>Before Export_IP</th>
<th>After Export_IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP Packaging TAT prior to SoC Hand-off</td>
<td>Display</td>
<td>3-4 Days</td>
<td>1-2 Hours</td>
</tr>
<tr>
<td></td>
<td>Media</td>
<td>1 Week</td>
<td>1-2 Hours</td>
</tr>
<tr>
<td></td>
<td>GPU</td>
<td>1 Week</td>
<td>2-3 Hours</td>
</tr>
<tr>
<td>Front-End SoC Integration TAT post Hand-off</td>
<td>Display</td>
<td>2-3 Weeks</td>
<td>1-2 Days</td>
</tr>
<tr>
<td></td>
<td>Media</td>
<td>3-4 Weeks</td>
<td>1-2 Days</td>
</tr>
<tr>
<td></td>
<td>GPU</td>
<td>3-4 Weeks</td>
<td>2 Days</td>
</tr>
</tbody>
</table>

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**Old PLC**

Ver1  Ver2  Ver3  Ver4  Ver5

**IP Packaging + SoC Integration**

**Time Saved**

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**New PLC**

Ver1  Ver2  Ver3

**Time Saved**

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In Conclusion...

Fast and high-quality IP delivery

- **80% Faster TTM** for packaging and integration to SoC
- Exceeded IP quality standards by ~90% fewer **SoC Integration bugs**
- About **50% reduction in headcount** from Integration teams

Continued Focus on Quality

- Reference SoC/TB
- Increased LRM compliance
- Online reporting dashboard and indicators

Shift Left Success

- Reduced burden on SoC during IP integration
- IPs own delivery of Quality drops
Acronyms

• PLC – Product Life Cycle
• TTM – Time To Market
• TFM – Tools, Flows and Methodologies
• HIP – Hard IP
• SIP – Soft IP
• TAT – Turn Around Time
• QA – Quality Assurance
• QC – Quality Check
• SD – Structure Design
• SoC – System on Chip