



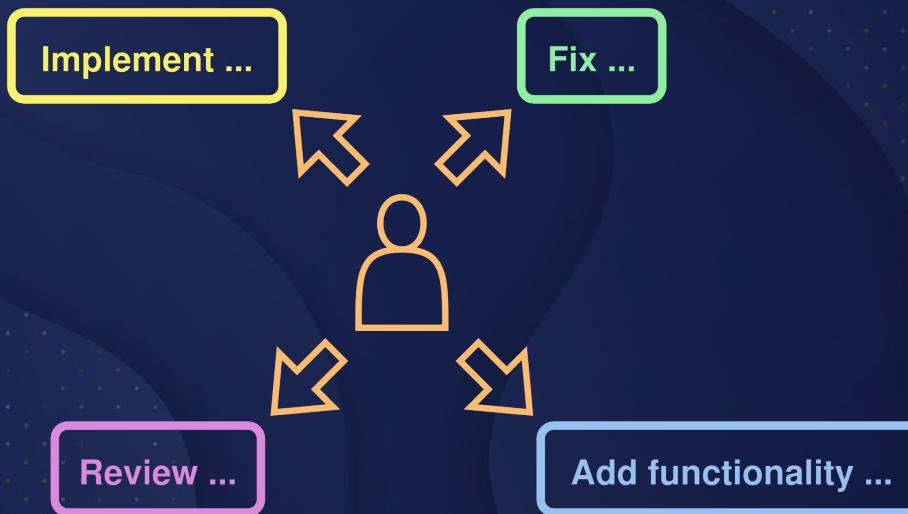
# LLM-based Functional Coverage Generation and Auto-Evaluation Framework

Ján Labuda, Marcela Zachariášová, Zdeněk Matěj

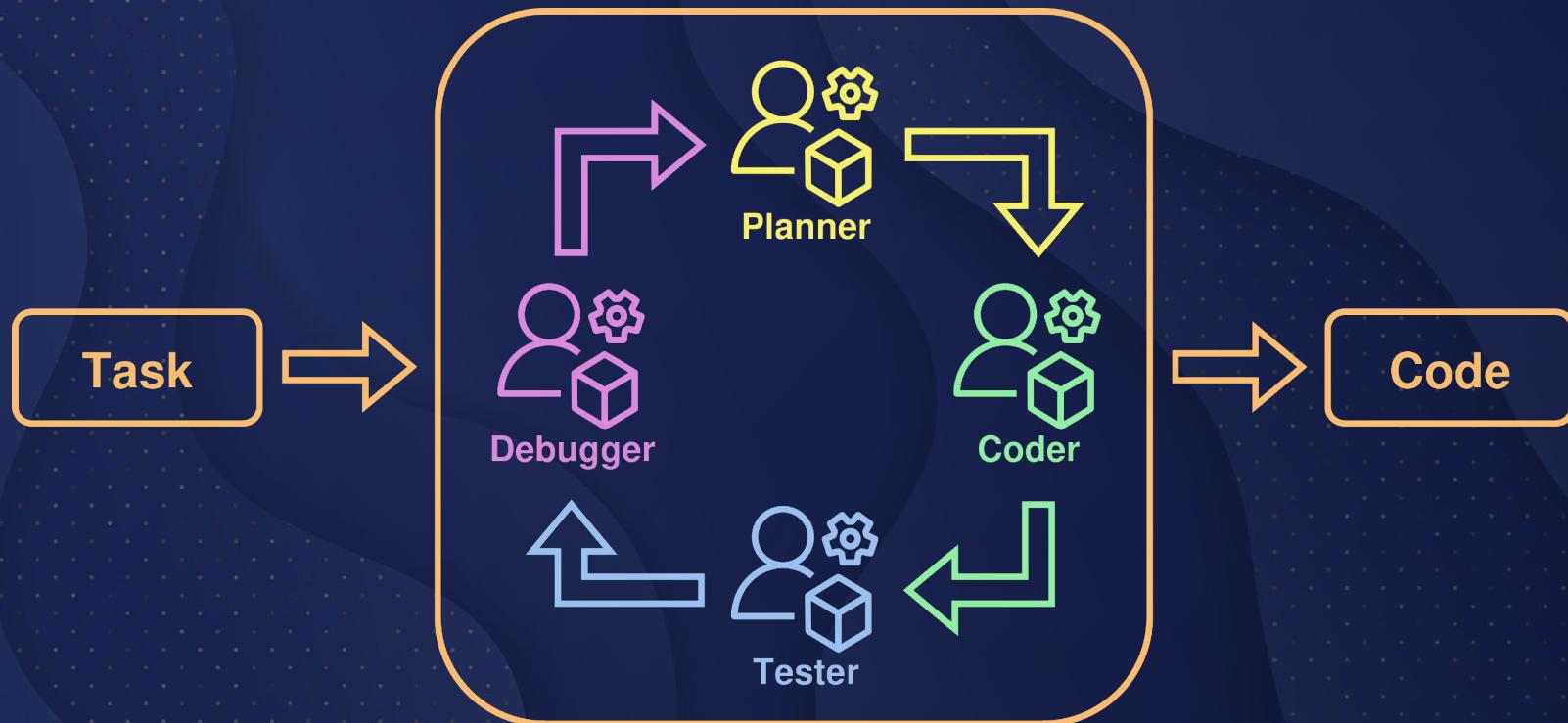


# Daily interaction with LLMs

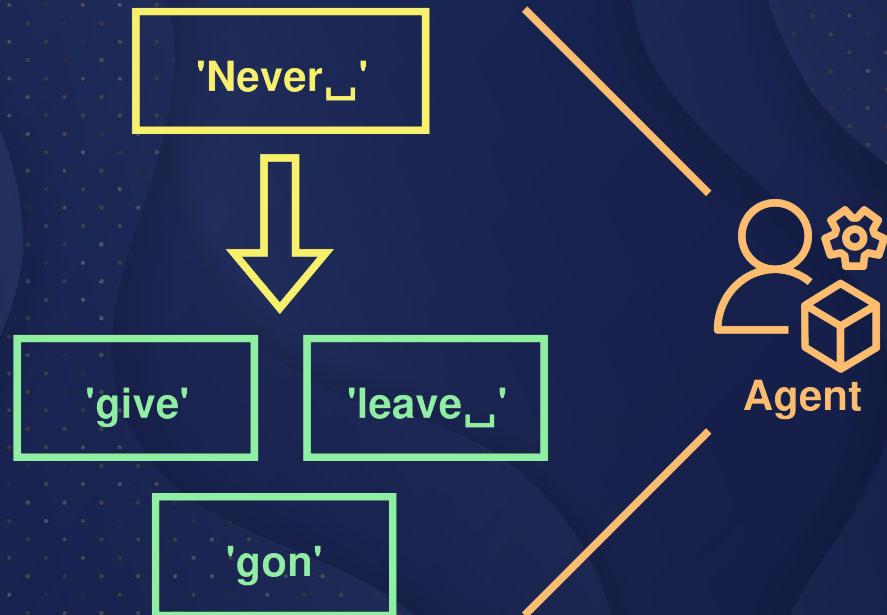
- Access to almost any solution from the Internet within seconds.
- How often have you argued with an LLM?



# Raise of Agentic Systems



# Deconstruction of Agentic Systems



# Deconstruction of Agentic Systems



# AI driven Chip Design

- Used in random stimuli generation, floor planning, and debug.
- Lacking a large quantity of good quality data to train LLMs.
- Application of agentic systems is still under the research.

# AI driven Chip Design

**DvCon USA 2025:** Configurable  
Graph-Based Task Solving with the Marco  
Multi-AI Agent Framework for Chip Design

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**NVIDIA:** Configurable  
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# AI driven Chip Design

**DvCon USA 2025:** Configurable  
Graph-Based Task Solving with the Marco  
Multi-AI Agent Framework for Chip Design

**DeepMind:** AlphaEvolve:  
A Gemini-powered coding  
agent for designing advanced  
algorithms

**NVIDIA:** Configurable  
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# LLMs and Functional Verification

- Topic still in the research.
- EDA vendors proposing new agentic systems.
- Initial experiments shown that LLMs struggle with UVM testbenches.

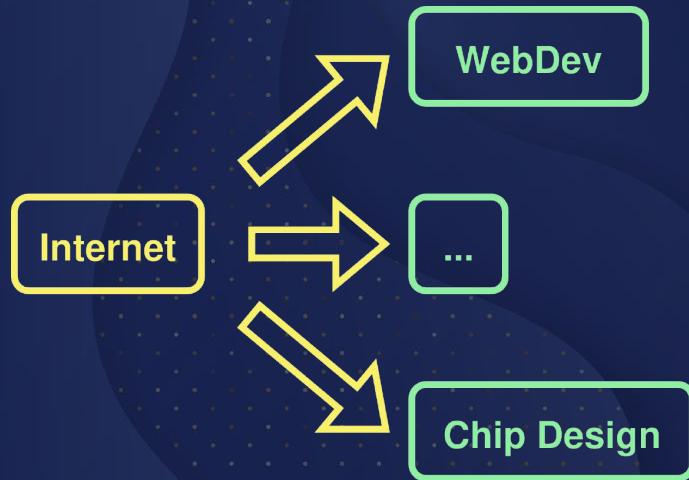
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Internet

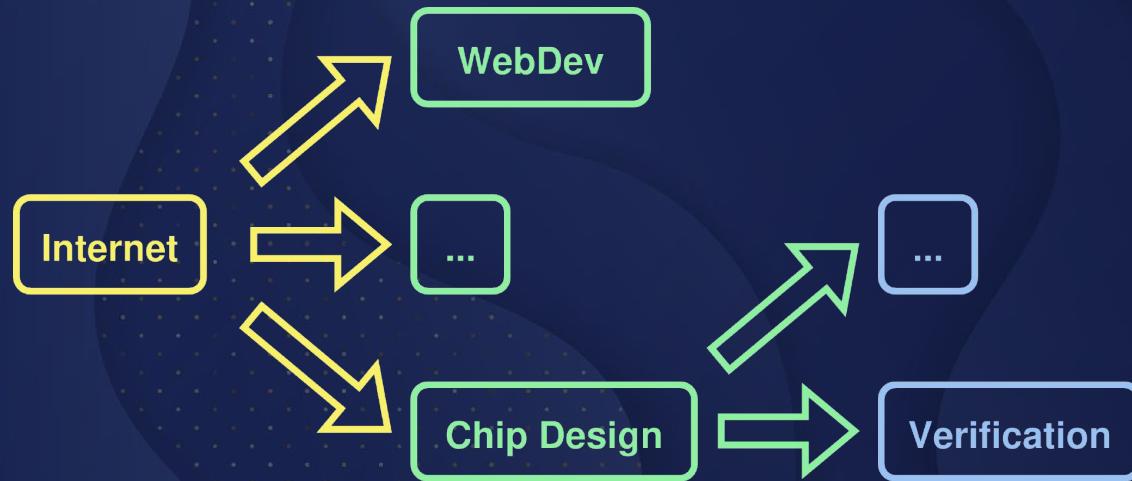
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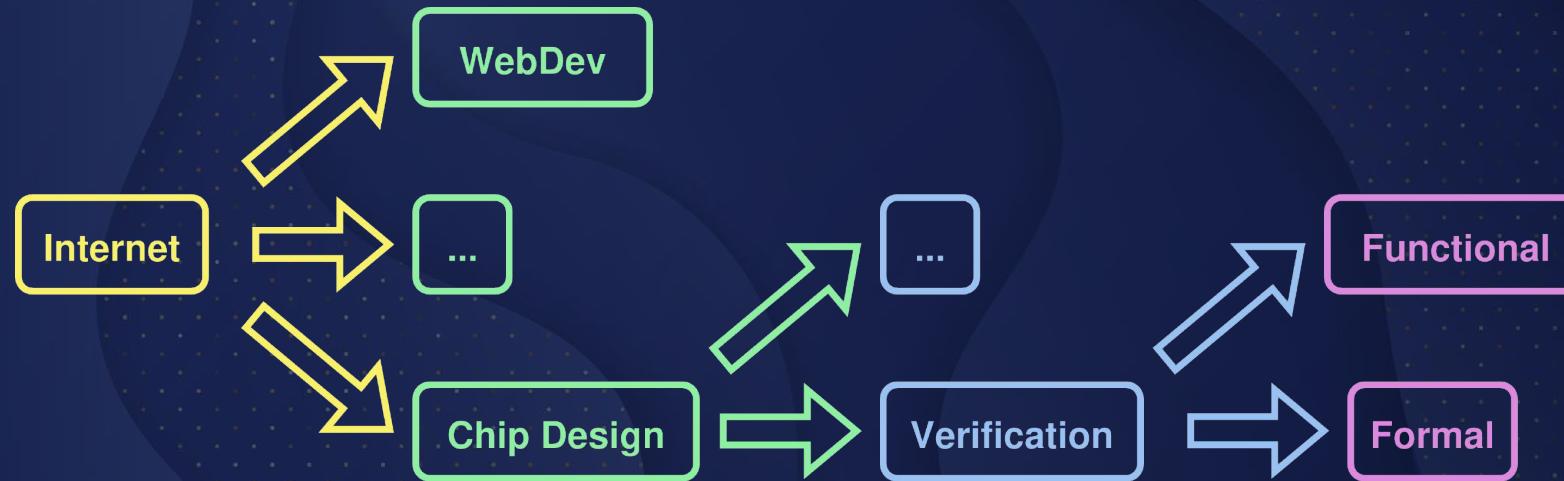
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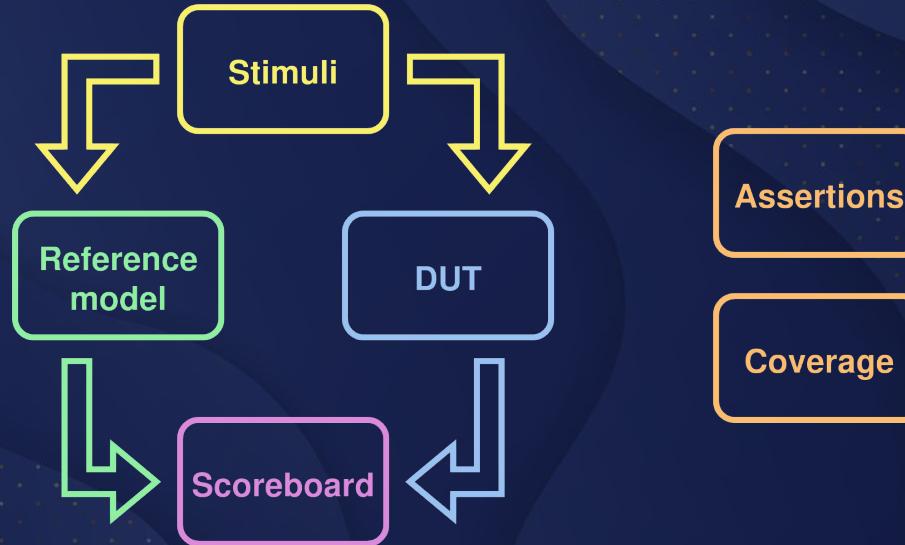


# LLMs and Functional Verification

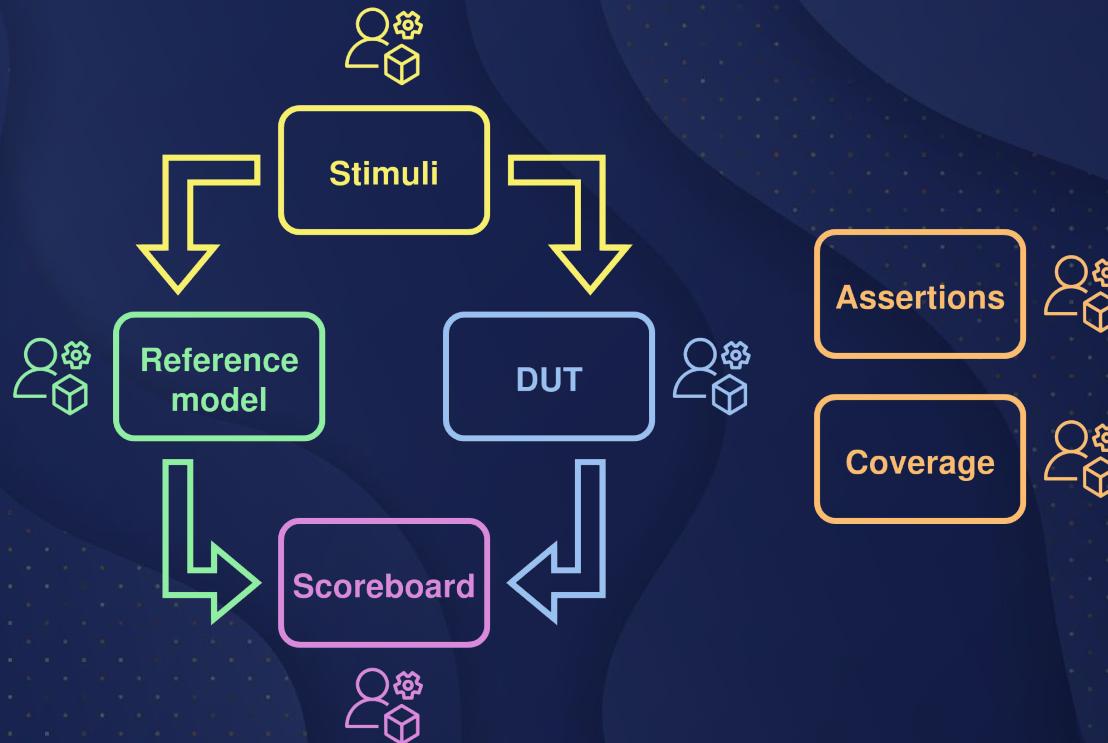
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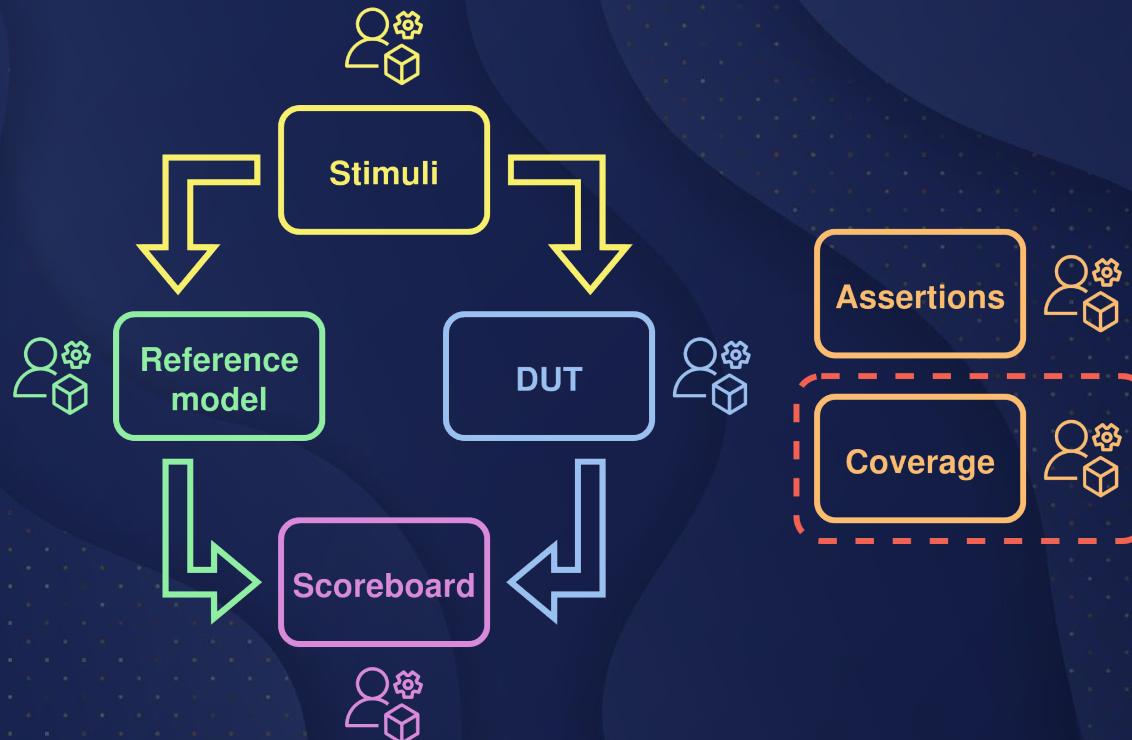
# Decomposition of Functional Verification



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# Decomposition of Functional Verification

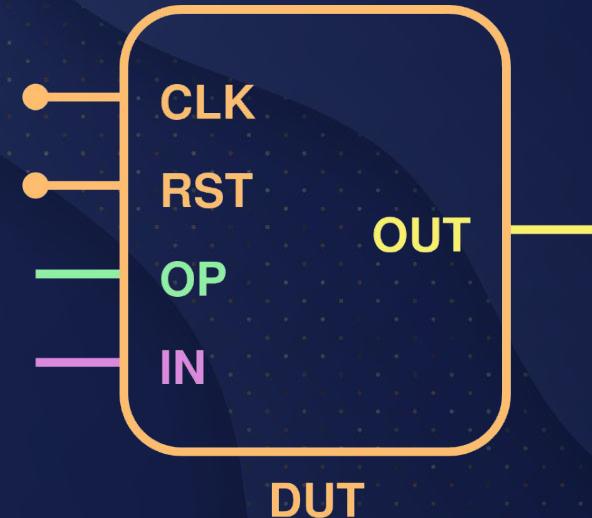


# Why Functional Coverage?

- Engineers are a bit sceptical towards LLMs.
- Coverage is a non-critical part of the testbench.

# Functional Coverage illustration

Bins	OUT	
Sequence	OP	
Cross	OP x IN	

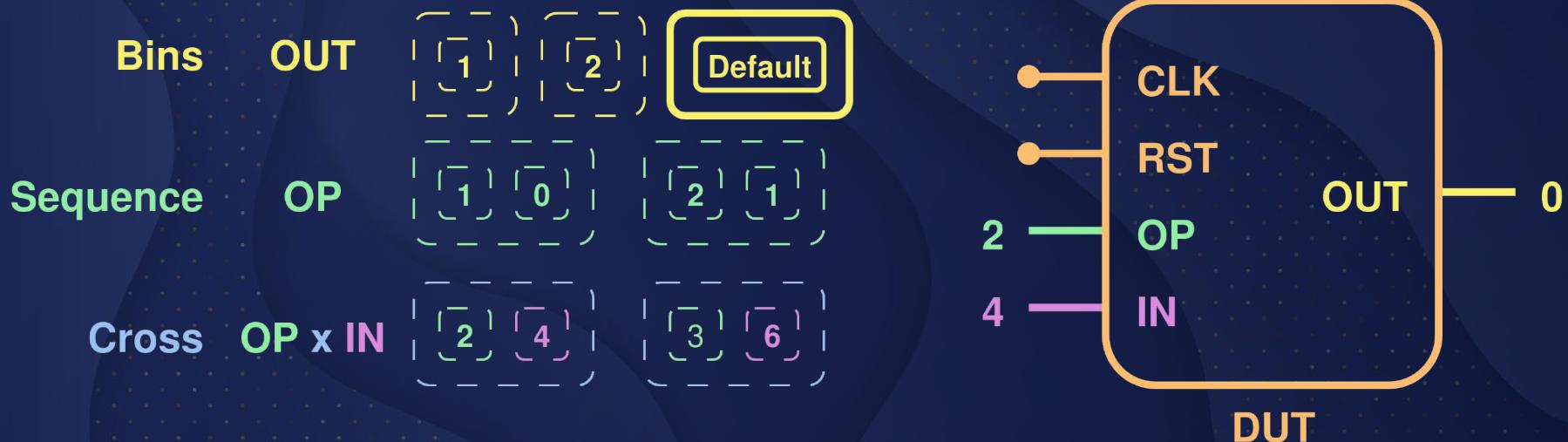


# Functional Coverage illustration

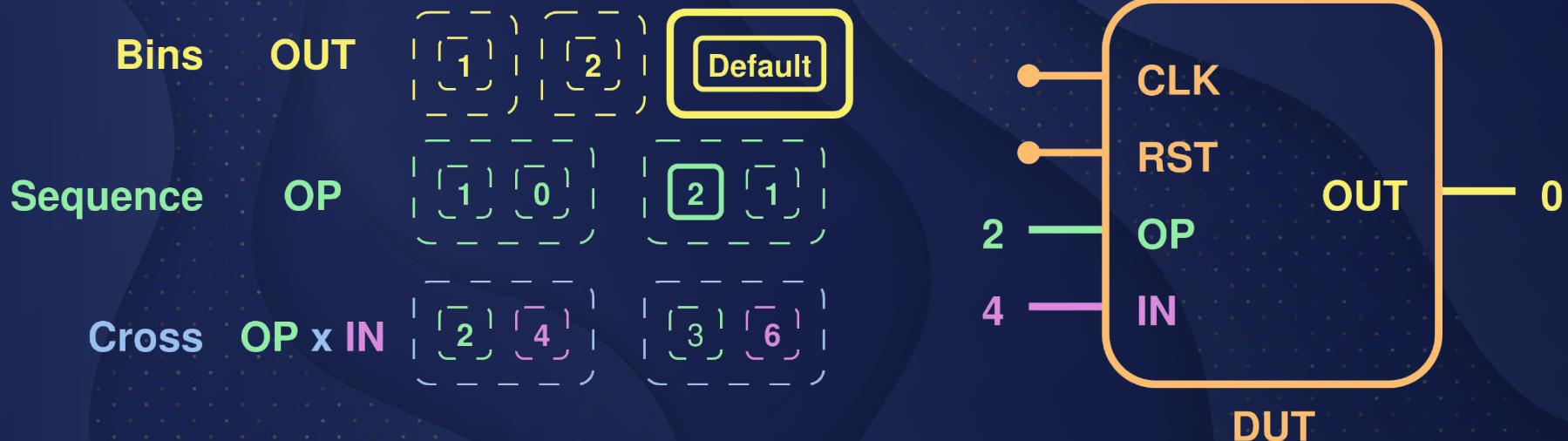
Bins	OUT	<table border="1"><tr><td>1</td><td>2</td><td>Default</td></tr><tr><td>1</td><td>2</td><td></td></tr><tr><td>1</td><td>2</td><td></td></tr></table>	1	2	Default	1	2		1	2				
1	2	Default												
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Sequence	OP	<table border="1"><tr><td>1</td><td>0</td><td>3</td><td>1</td></tr><tr><td>1</td><td>0</td><td>3</td><td>1</td></tr><tr><td>1</td><td>0</td><td>3</td><td>1</td></tr></table>	1	0	3	1	1	0	3	1	1	0	3	1
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Cross	OP x IN	<table border="1"><tr><td>2</td><td>4</td><td>3</td><td>6</td></tr><tr><td>2</td><td>4</td><td>3</td><td>6</td></tr><tr><td>2</td><td>4</td><td>3</td><td>6</td></tr></table>	2	4	3	6	2	4	3	6	2	4	3	6
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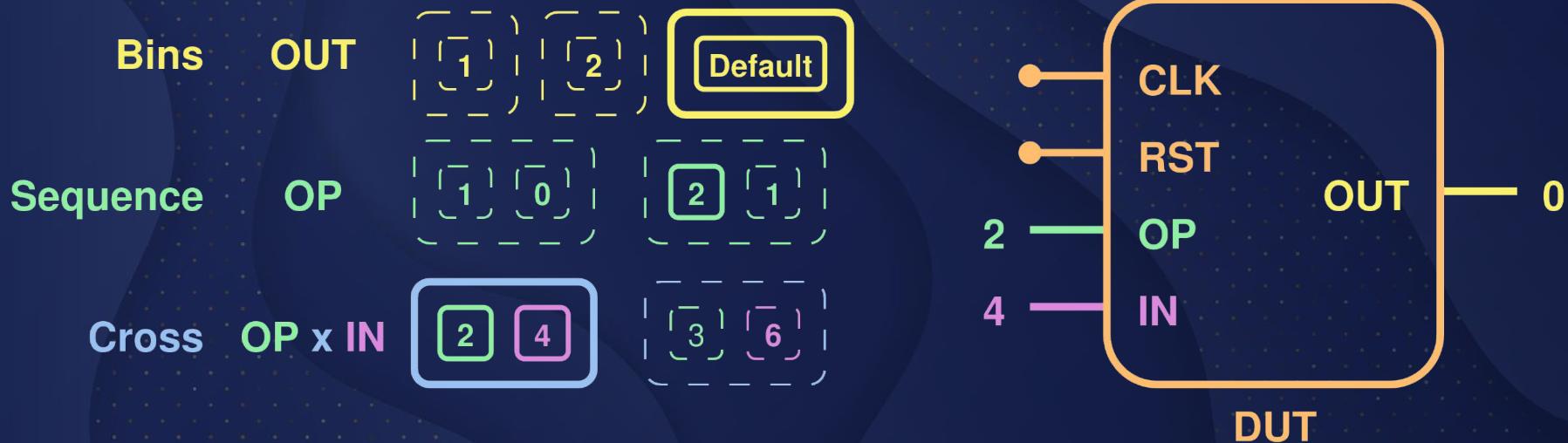
# Functional Coverage illustration



# Functional Coverage illustration



# Functional Coverage illustration



# Functional Coverage and LLMs

- Initial attempts generated code in SystemVerilog.
- Smaller LLMs struggled to generate syntactically correct code.
- How then evaluate LLMs knowledge about functional coverage?

# Our Functional Coverage implementation

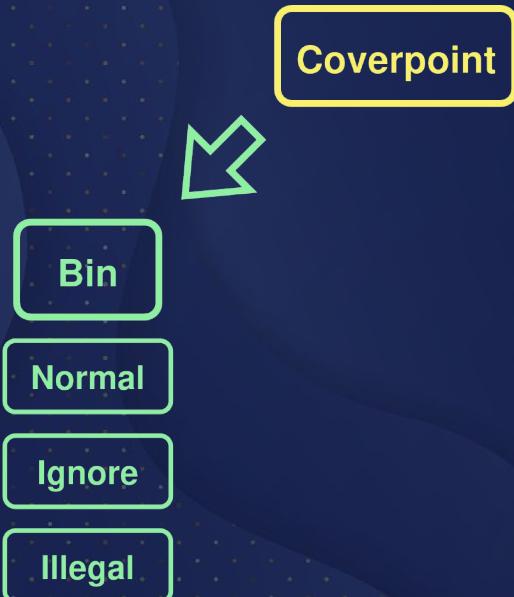
- Python is better understood by LLMs than SystemVerilog.
- Problem: no native support in CoCoTB.
- Available 3rd party package mimicking SystemVerilog.



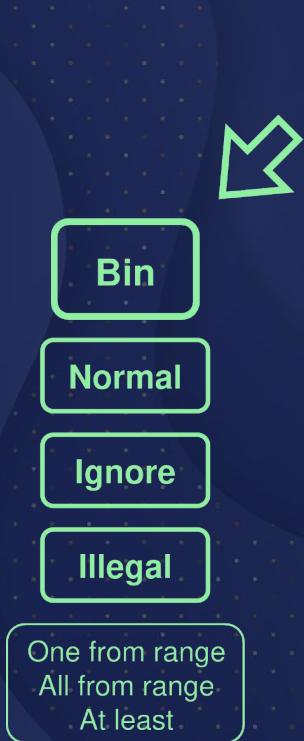
# Functional Coverage API

Coverpoint

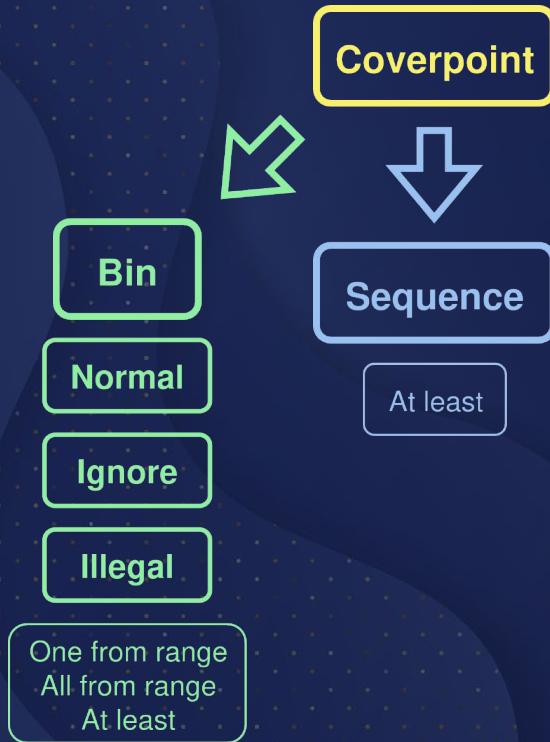
# Functional Coverage API



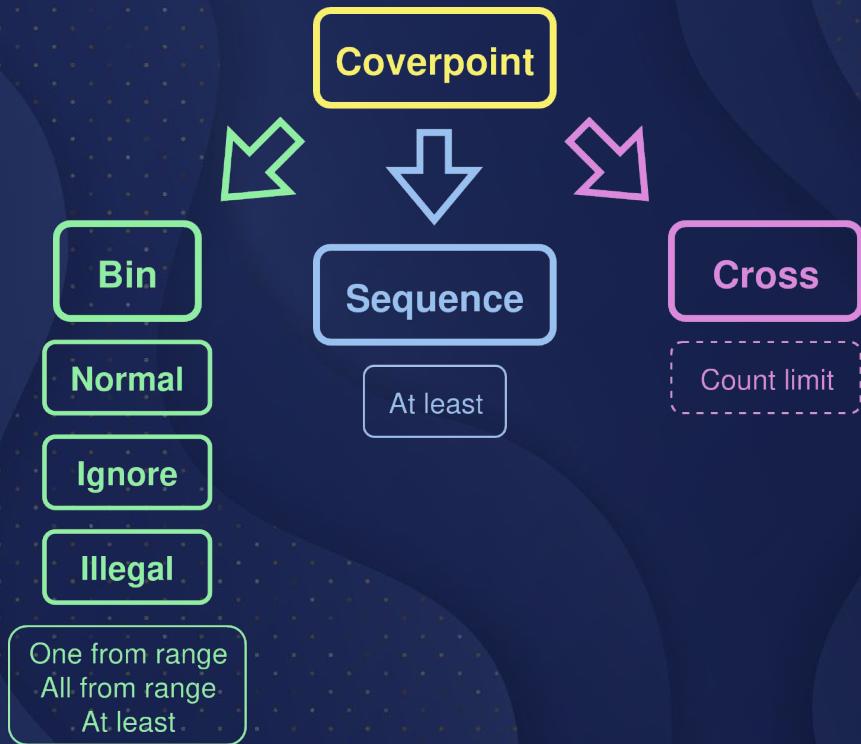
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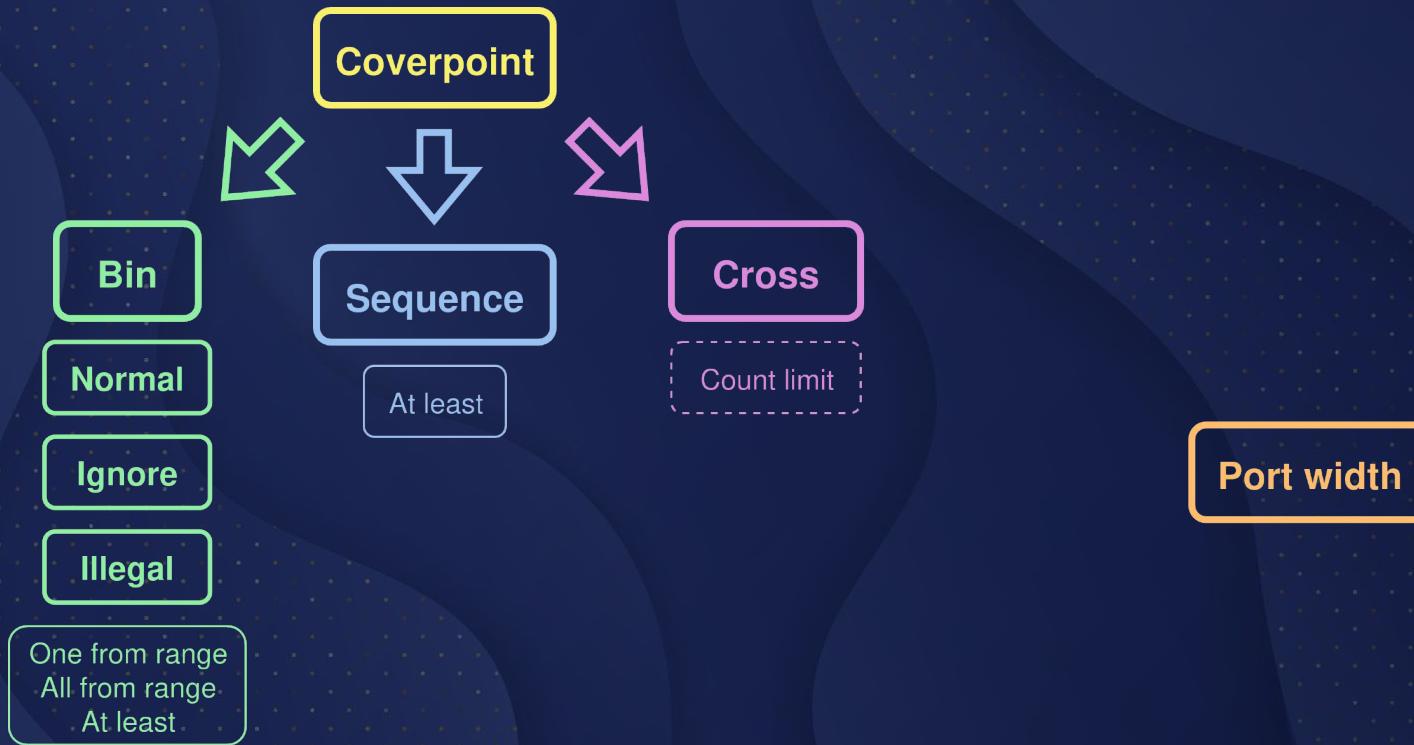
# Functional Coverage API



# Functional Coverage API



# Functional Coverage API



# What was tested?

- Top 3 most popular open weight models from Ollama:
  - Deepseek-r1
  - Gemma 3
  - Qwen3
- Various model sizes up to 14 billion parameters.

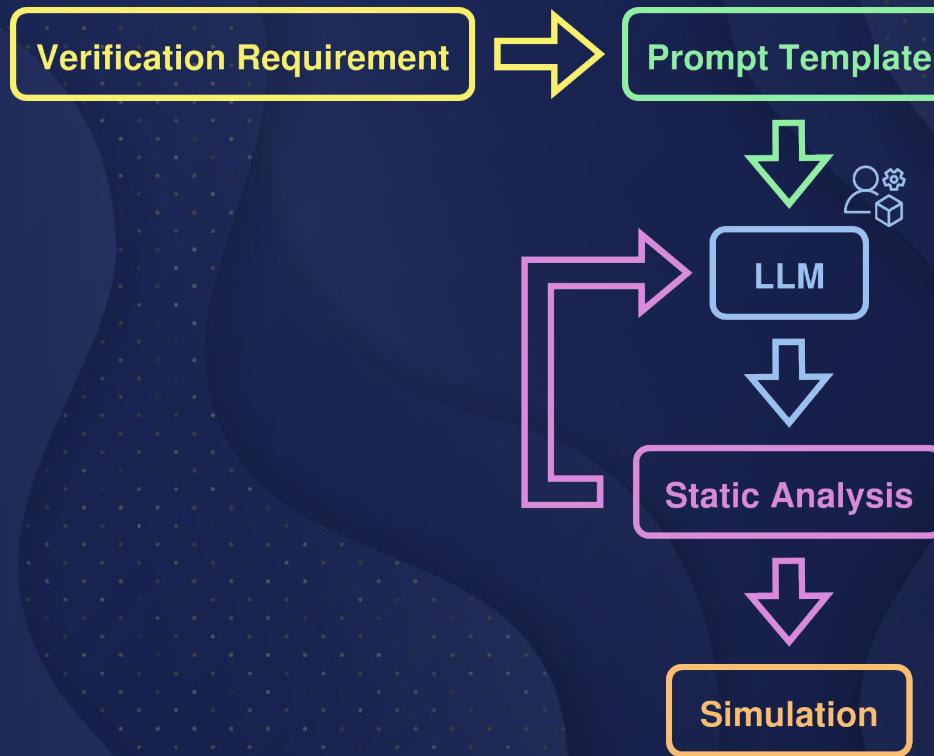
# How it was tested?

- Initial experiments used natural language specification as an input. (Not successful)
- Shift to natural language verification requirements. (way to go)

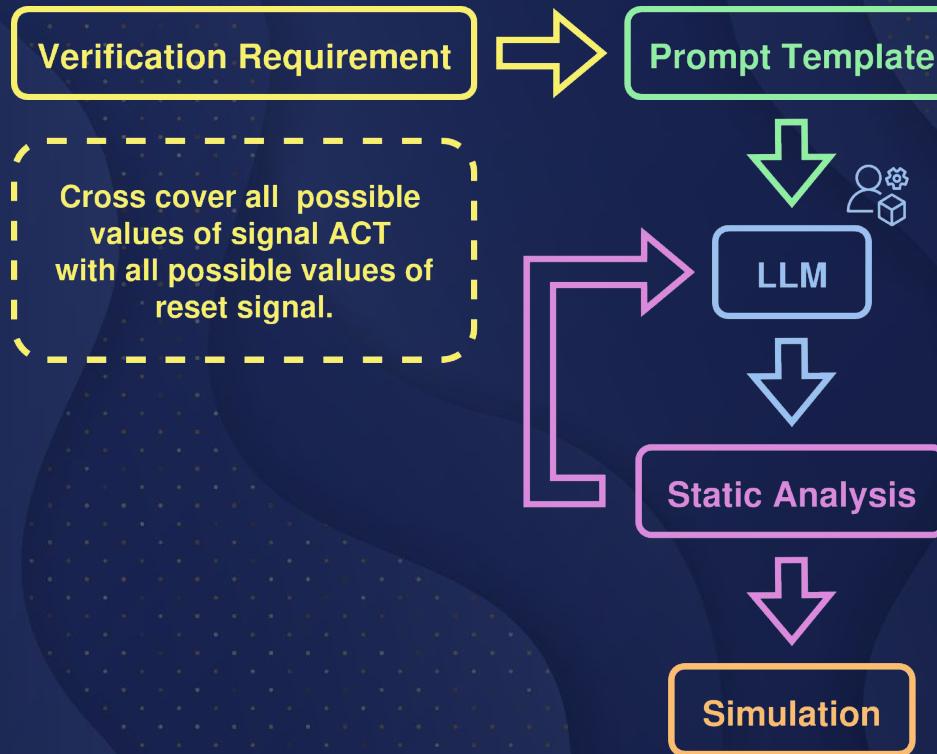
# How it was tested?

- Initial experiments used natural language specification as an input. (Not successful)
- Shift to natural language verification requirements. (way to go)
- A verification expert provided:
  - 16 verification requirements based on original specification (ALU).
  - Desired functional coverage code.
- Each model with distinct size had 5 attempts that were aggregated.

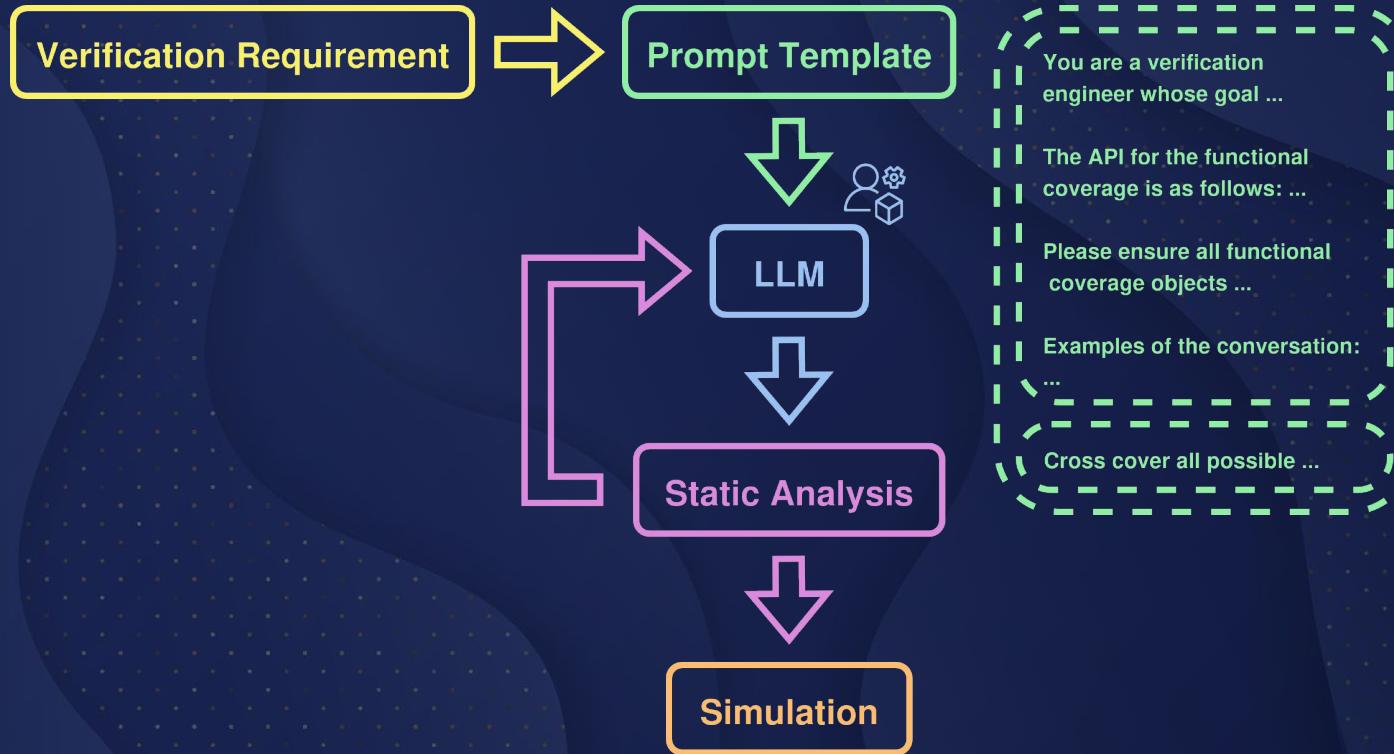
# Generation of Functional Coverage



# Generation of Functional Coverage



# Generation of Functional Coverage



You are a verification engineer whose goal ...

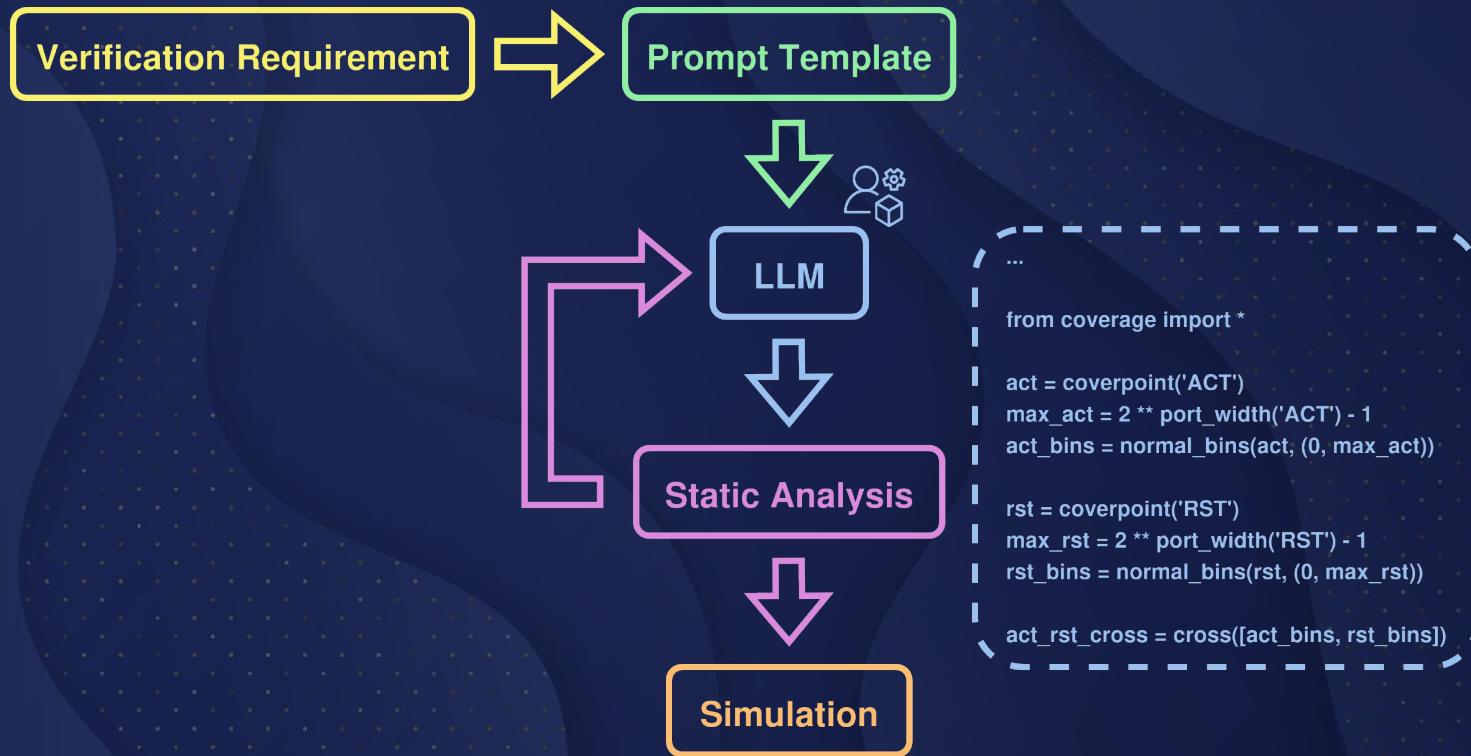
The API for the functional coverage is as follows: ...

Please ensure all functional coverage objects ...

Examples of the conversation:

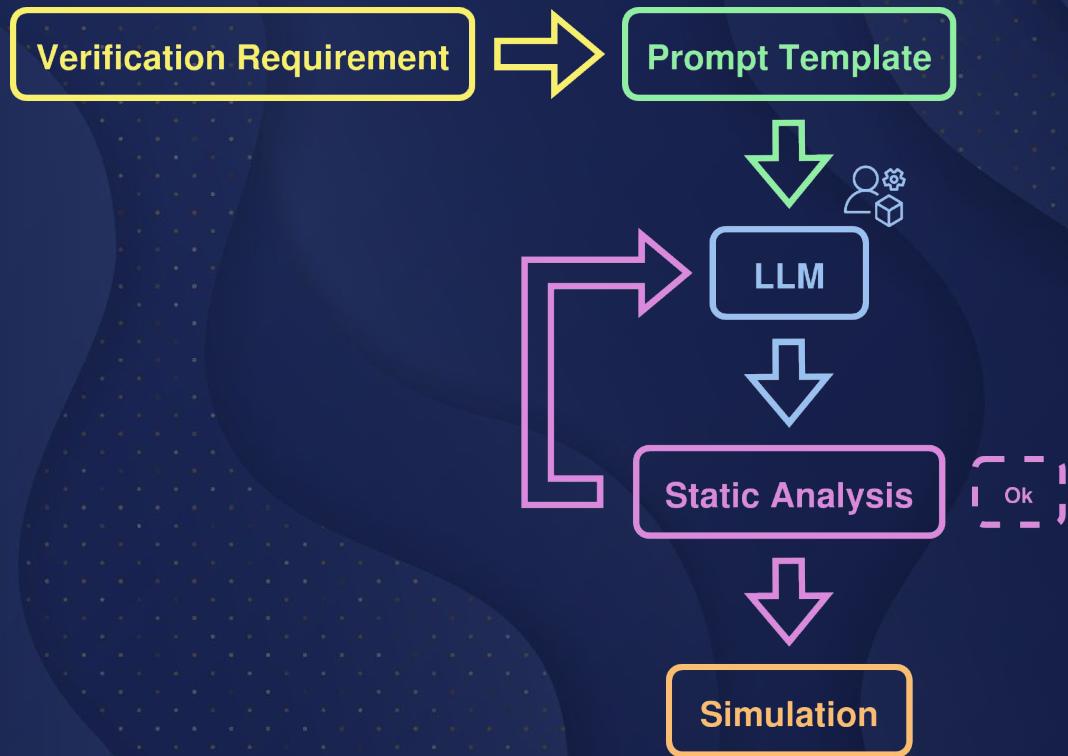
...  
Cross cover all possible ...

# Generation of Functional Coverage

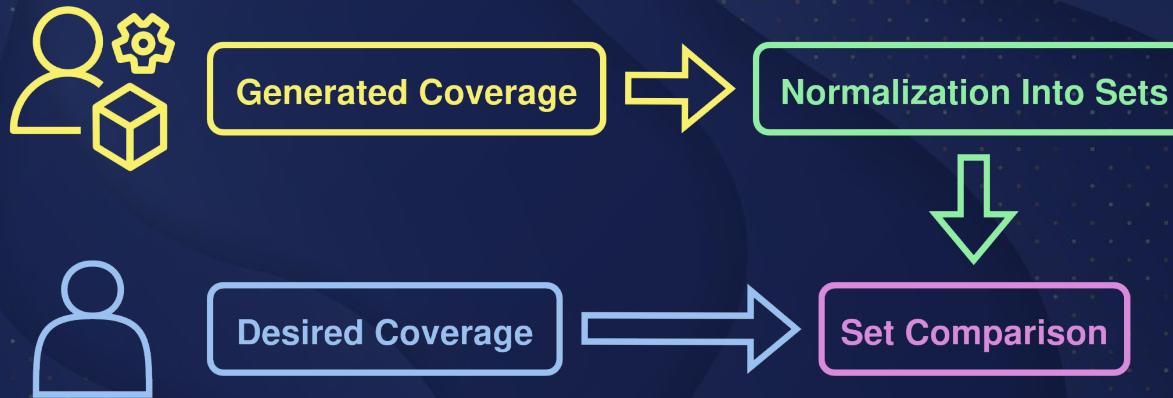


```
...  
from coverage import *  
  
act = coverpoint('ACT')  
max_act = 2 ** port_width('ACT') - 1  
act_bins = normal_bins(act, (0, max_act))  
  
rst = coverpoint('RST')  
max_rst = 2 ** port_width('RST') - 1  
rst_bins = normal_bins(rst, (0, max_rst))  
  
act_rst_cross = cross([act_bins, rst_bins])
```

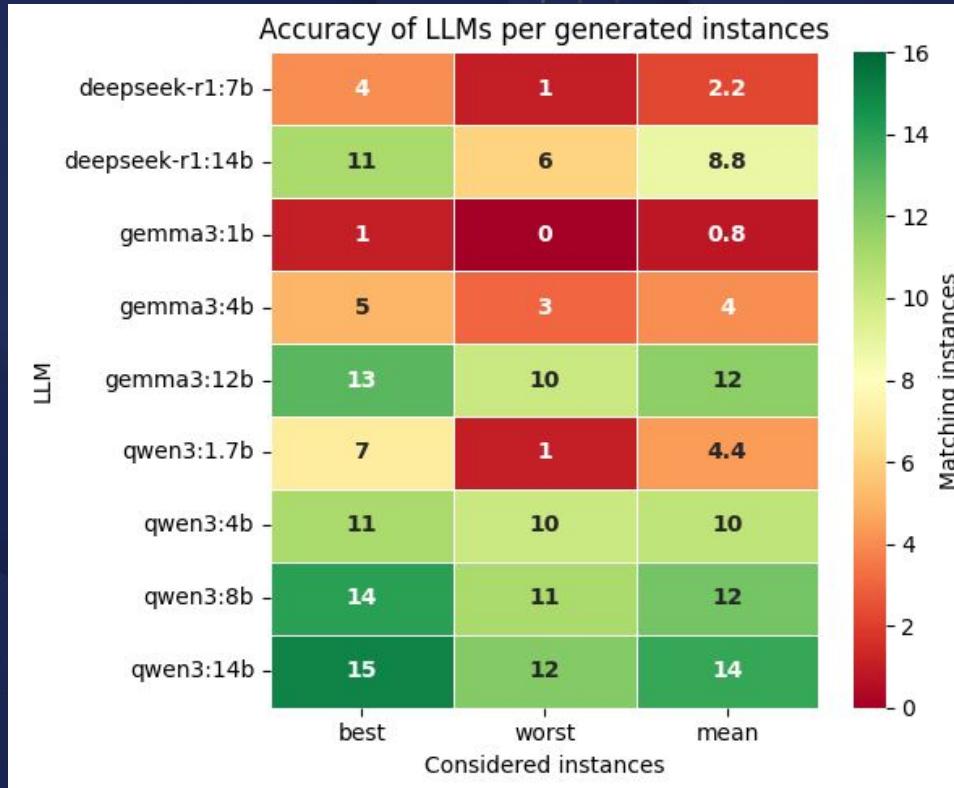
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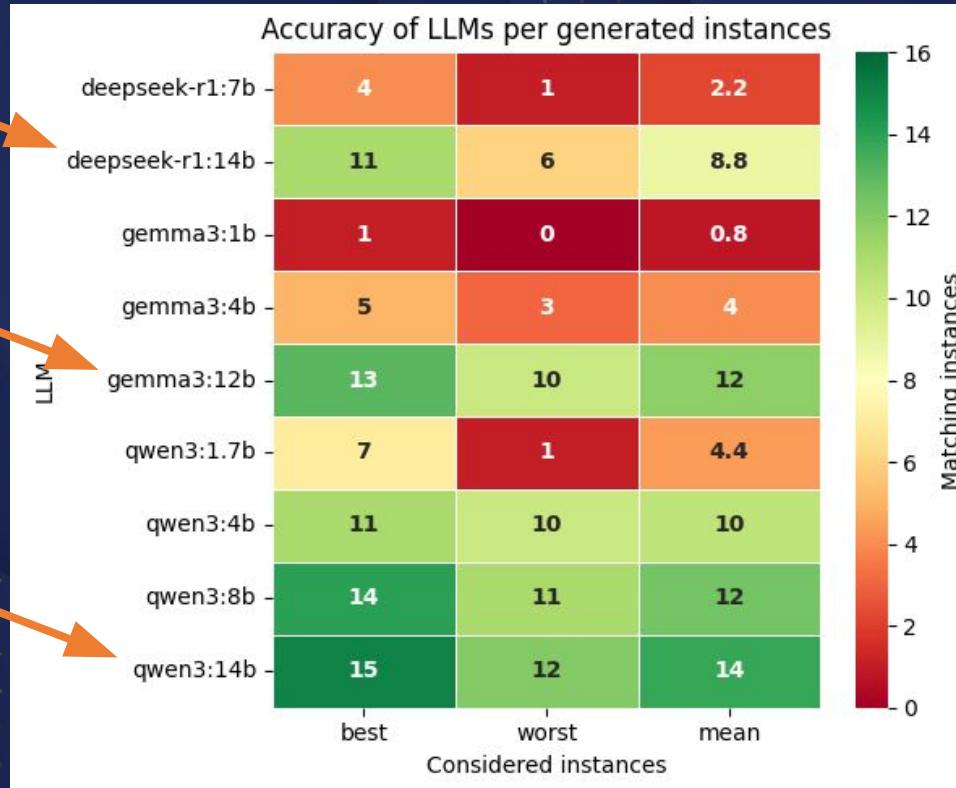
# Comparison of Functional Coverage



# Results

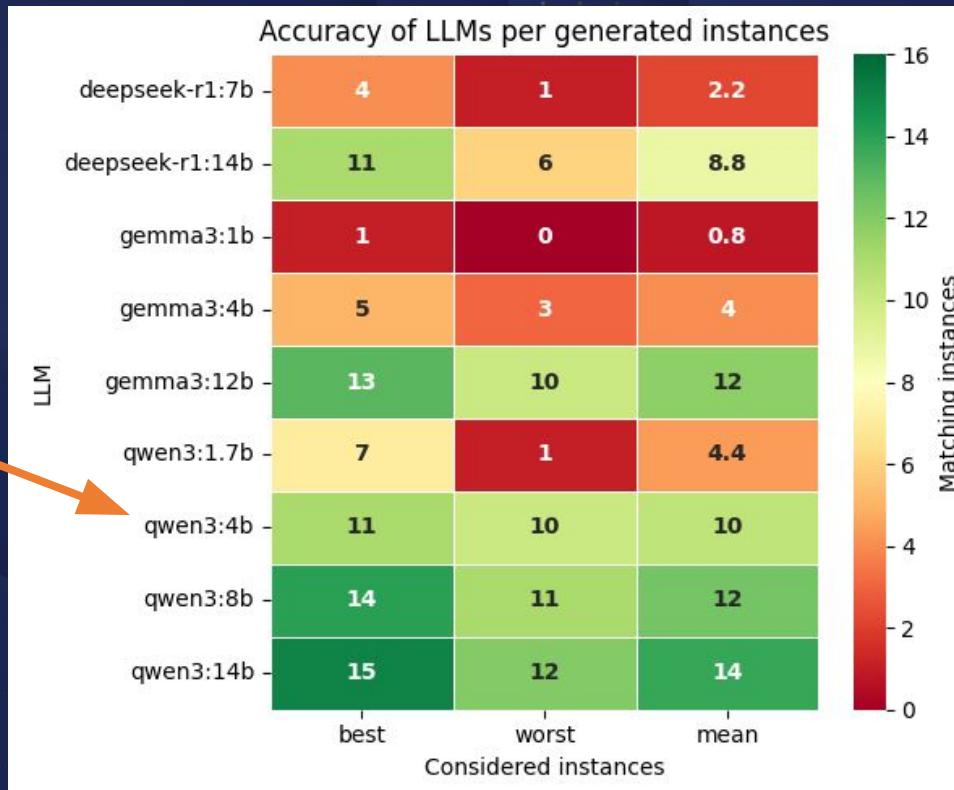


# Results

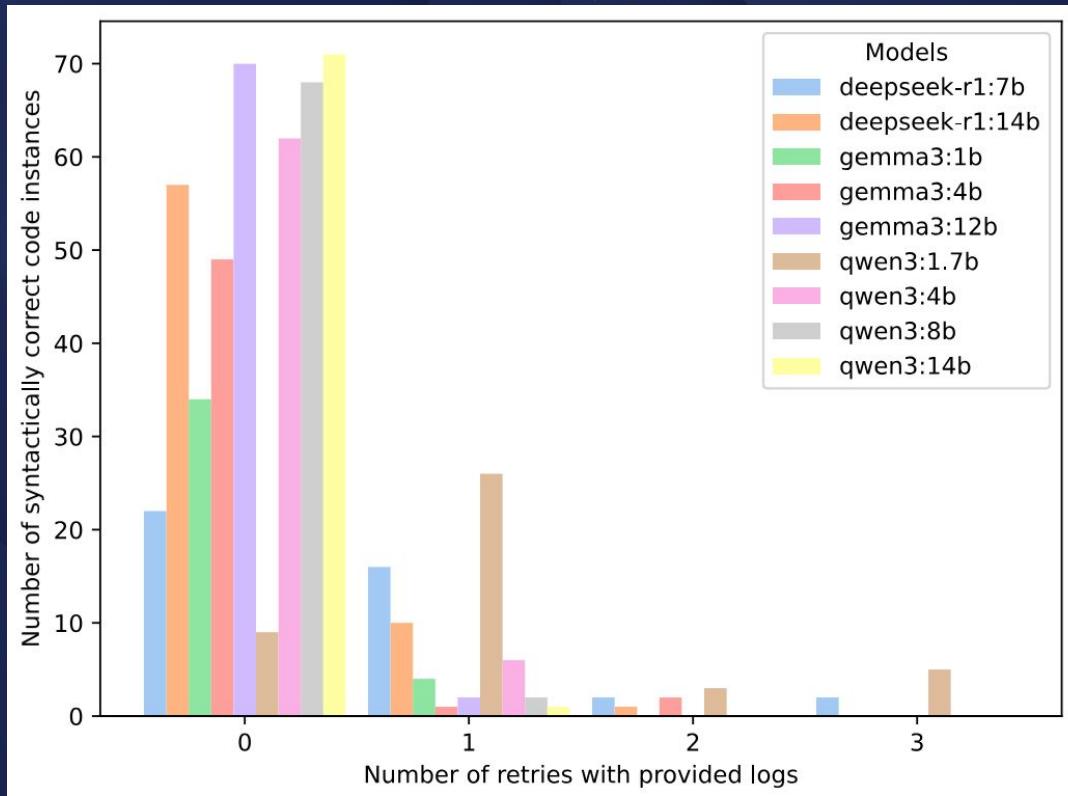


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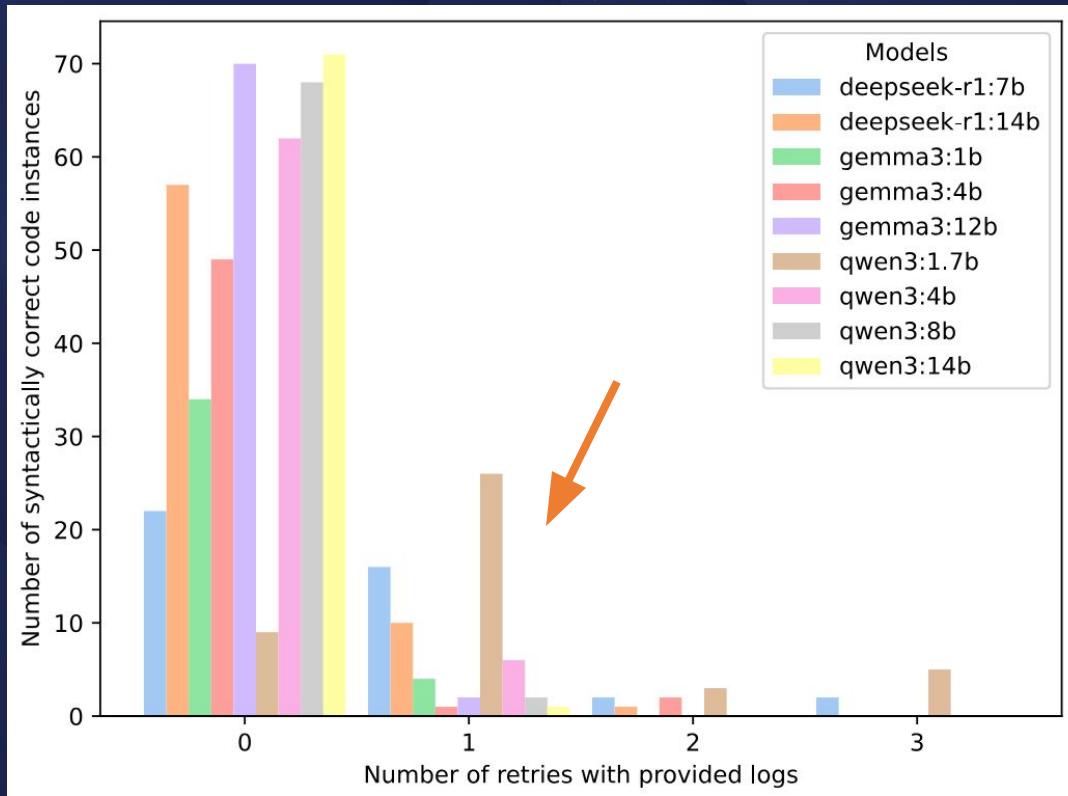
2.5GB VRAM



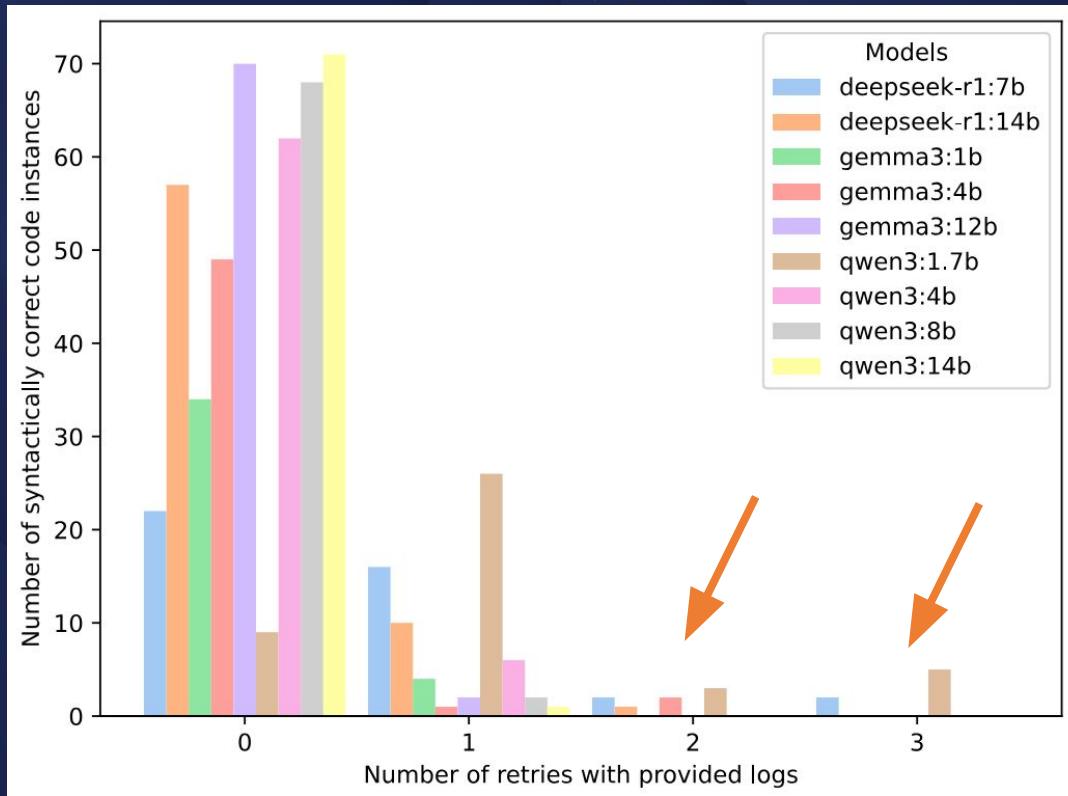
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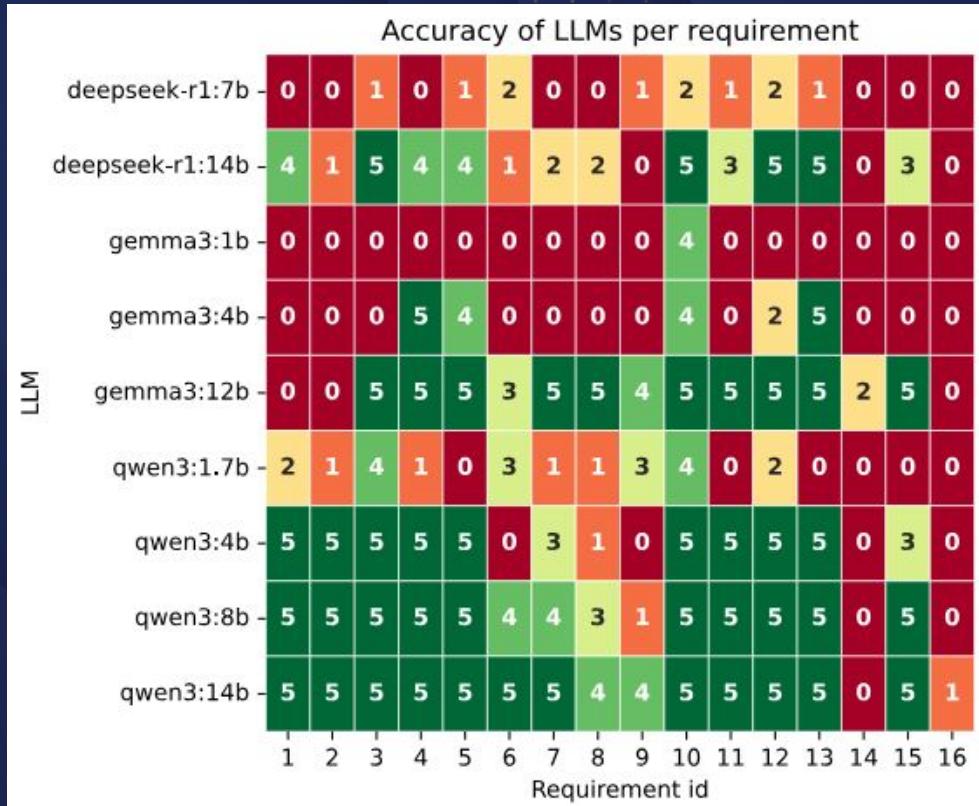
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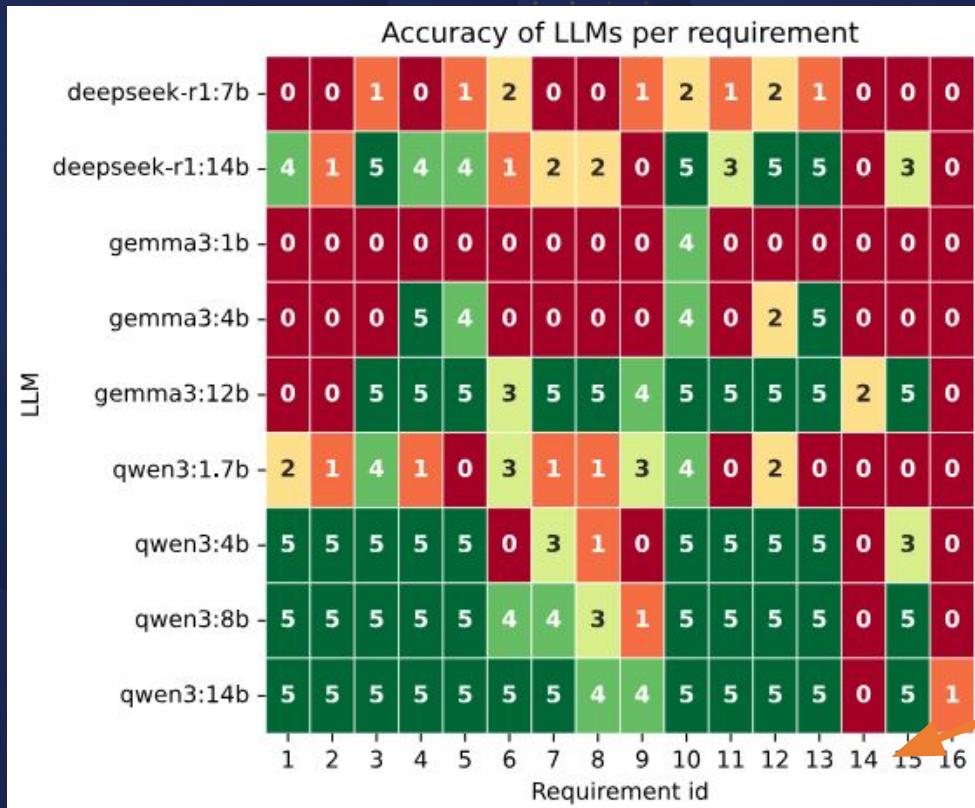
# Results



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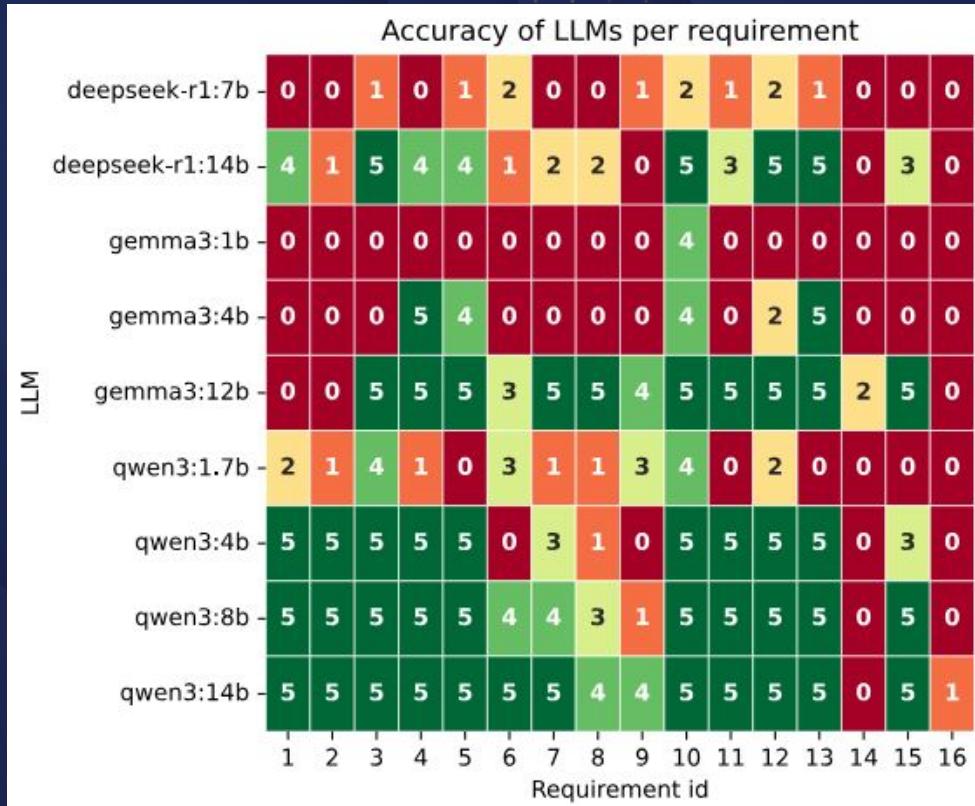


# Results



Generated too  
many bins

# Results



Cross coverage  
was too large

# What now?

- Future plans:
  - Enhance our open source dataset with more samples.
  - Evaluate generation of the SystemVerilog functional coverage.
  - Pre-train and finetune LLMs on synthetic data.
- Looking for a PhD research stay - let's discuss!
- Try the code from [github.com/Northeus/coge](https://github.com/Northeus/coge)
- Contact: [jan.labuda@mail.muni.cz](mailto:jan.labuda@mail.muni.cz)

