Hybrid Flow: A smart methodology to migrate from traditional Low Power Methodology

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 Agenda

• Low Power Overview
• Low Power Optimization in Design
• Intel Client Low Power Methodologies
• Motivation : Traditional Vs Proposed
• Power Intent Body
• Introduction to hybrid Methodology
• Challenges in Hybrid Flow
• Advantages of Hybrid Methodology
Low Power

• Power Management is Critical Today
• Driving for finer process technology
  – Smaller, lighter products
  – Longer battery life
  – More functionality
• Dynamic power
  – Signal switching consumes energy
  – Was the major contributor to power consumption
• Static power
  – Static leakage can consume 50% of power!
  – Now the major concern for power optimization
Motivation: Traditional Vs Proposed

- Complexity of the Design
- IP Sourced from multiple vendor – Internal, External & Hard IPs.
- Need of the hour is Abstraction
- Physical Design Limitation
- Multiple Flows for Functional Verification vs Implementation
- Large Number of Power and Voltage Domains
- Adoption of new feature of latest power intent
Power Intent Body

- Top level domain definition
  Supply Interfaces (creating supply sets, ports, nets)
  Connecting Supplies

- Loading of UPFs

- Defining low power strategies
  Defining the level shifter strategies, isolation strategies & retention control strategies

- Defining SRSNs strategies

- Defining PSTs

The PST describes all the valid combinations of voltage states that can exist in the design.

create_supply_net "vcc_in"
create_supply_port -direction "in"
create_supply_net "vcc_in" -ports "vcc_in" create_supply_net "vcc_out"

connect_supply_net "vcc_in" -ports "vcc_in" create_supply_net "vcc_out"

create_power_domain "vccsta_domain_merge"
  -supply [extra_supplies_1 VCCSA]
  -supply [extra_supplies_2 VCCSTL]

set_isolation punit_vccsa_vccstl_iso_dummy
  -domain "vccstl_domain_merge"
  -isolation_supply_set "VCCSTL"
  -isolation_signal "punit_wrap/punit/tppcbclk/tppcbclk_soft_supply"
  -isolation_sense "low"
  -location "self"
  -elements [list "punit_wrap/punit/tppcbclk/PliXclkSyncFnn4H"

set_port_attributes -ports [join $iov_clamp_value_1_elements] -clamp_value

add_power_state "VCCSA" -state "ps_VCCSA_LV" -supply_expr [power == \(\text{FULL\_ON},0.65\)] -simstate NORMAL
Introduction to Hybrid Methodology

SoC Design

Partition with hierarchical and UPF 2.x

Hierarchical UPF 2.x power intent is used for FV and implementation Flow

Unit Level- U21, U22...U2n. Units are wrapper around IPs.

Soft IPs (UPFs + Libs)

Hard IPs (UPFs + Libs)

Merge Flow (All the power domains are merged to 1. All the SIPs are merged into single domain)

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Soft IPs

Hard IPs

Hierarchical Partition UPF

Partition with merged UPF

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Soft IPs comes as a synthesizable module in hardware description languages (HDL) such as SystemVerilog or VHDL. Ex – CPU, Power Control Module etc

Hard IPs is a predesigned layout with all power management functionality built into the IP itself. Ex - DDR PHYs, USB PHYs, PLLs etc.

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Hard IPs (UPFs + Libs)
Intel’s SoC Design Integration Flow

Low Power Specs are defined as Micro Power Architect and it included top interfaces, partitions level interfaces, crossing table & bump details.

IP Level
(UPFs, Libs)

- Developed power intent
- Quality sign off for all stages
- Static, functional verification, emulation, implementation

Unit Level
(Load UPFs for SIPs & HIPs)

- UPF Owner are supposed to load the unit UPFs and build the hierarchal power intent.
- Unit is essentially a wrapper around for SoC usage

Partition Level
Partition Level has 2 flavors of power intent

- Collage integrates IP UPFs into FE model
- Auto generation of merged partition UPFs for the implementation
- Hierarchical flow is mainly used for the functional verification flow

SoC Level
(Different SoC Flows are used for Functional Verification & Implementation)

- SOC designs are verified with 2 different methodology because of the traditional flow limitation. Functional verification and emulation flow is build for SoC Level whereas Implementation Flow quality is being checked at partition level and SoC Level
Hybrid Flow Implementation

- Client SoC with more than 1 billion gates design
- SoC Contains 34 partitions with memories, power management, PCI, CPU, Display blocks
- 5 different partition design blocks
- Multiple Flows for Functional Verification vs Implementation
- Large Number of Power and Voltage Domains
- Adoption of new feature of latest power intent

<table>
<thead>
<tr>
<th>Block Type</th>
<th>Cell count</th>
<th>Number of power domains</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power management</td>
<td>~48000</td>
<td>3</td>
</tr>
<tr>
<td>Legacy</td>
<td>~24000</td>
<td>3</td>
</tr>
<tr>
<td>Fabric</td>
<td>~87000</td>
<td>3</td>
</tr>
<tr>
<td>IOP</td>
<td>~17000</td>
<td>3</td>
</tr>
<tr>
<td>MC Main</td>
<td>~4000</td>
<td>3</td>
</tr>
</tbody>
</table>
Challenges of Hybrid Methodology

- In Source-Sink isolation strategy, “HETEROGENEOUS_FANOUTS” Warning (Isolation is skipped).
- Here same signal out1 is given as input to PD2 block and also for PD3 block ..
- Sinks related to PD2 are not real sinks and sink PD3 is a real one. Would like to exclude sinks related to PD2.

```
set_design_attribute -elements <list of elements> -attribute SNPS_treat_as_unconnected TRUE
```
Challenges in Hybrid Flow Implementation

Terminal boundary issue:

Isolation cell with source and sink strategy got matched but isolation cell is not placed due to crossover contain a wire which belongs to terminal boundary.

But due to terminal boundary set on BLK1 element and signal is crossing via wire which is used in BLK1 is breaking this connection.

Attribute used: set_design_attributes -elements {soc_tb/soc/par_punit/punit_wrap/punit/assert_xcheck_punit soc_tb/soc/par_punit/punit_wrap/punit/assert_ifc_stability_check_punit} -attribute SNPS_treat_as_unconnected TRUE
Physical Design challenges...

- Power switch insertion issues

```
create_power_switch sw_northpeak_vccsa_PGD -domain northpeak_wrap/northpeak/pd_northpeak_vccsa_PGD
```

- Shadow domain solution for optimization

Errors: Supply net northpeak_wrap/northpeak/vccsa cannot be connected to the pin

```
ps_pg питания CELL_segment_wrap/pg_pb_bottoms_snaps_pn_northpeak_vccsa_PGD_sw_northpeak_vccsa_PGD_snaps_w05pawrl6enlgjih6_90_909/vcc_in
in domain ps_pg_wrap_cell_segment_wrap/pg_pg_pg_wrap_cell_segment_wrap. [OFF-031]
```

Errors: Problem in contact_supply_set.

Use error_info for more info. (CMD-813)
Physical Design Challenges..

- IC Compiler 2 demands matching between states in top level PST and sub hierarchy PST. The solution for this is to disable lower level PST.
Physical Design challenges

• **Missing supply states issue:** A group of hierarchical PDs in the same VA will share same primary supplies but if there is a mismatch in secondary domains, as long as at least one domain contains the required supply as available supply, tool can use the hierarchy of the domain to put the cell anywhere in the VA physical shape.
Advantages of Moving to Hybrid flow

• Hierarchical methodology with hybrid flow supports partitioning, parallel development, and reuse.
• The UPF complexity is very much reduced.
• Supply sets provides an abstraction and allows designers to define their power intent without having to create the actual supply nets.
• Usage of hierarchical flows at all the stages of design flow eliminates the usage of two different UPFs.
• Advantages of add_power_state
• The usage of set_design_attribute allows the propagation of power information to the lower levels of design hierarchy
Questions

Finalize slide set with questions slide