# Hybrid Flow: A smart methodology to migrate from traditional Low Power Methodology

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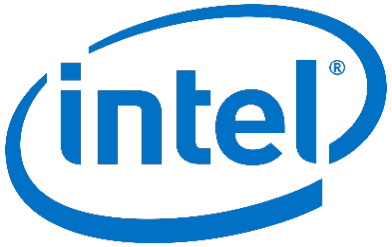



accellera SYSTEMS INITIATIVE

2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

# Agenda

- Low Power Overview
- Low Power Optimization in Design
- Intel Client Low Power Methodologies
- Motivation : Traditional Vs Proposed
- Power Intent Body
- Introduction to hybrid Methodology
- Challenges in Hybrid Flow
- Advantages of Hybrid Methodology

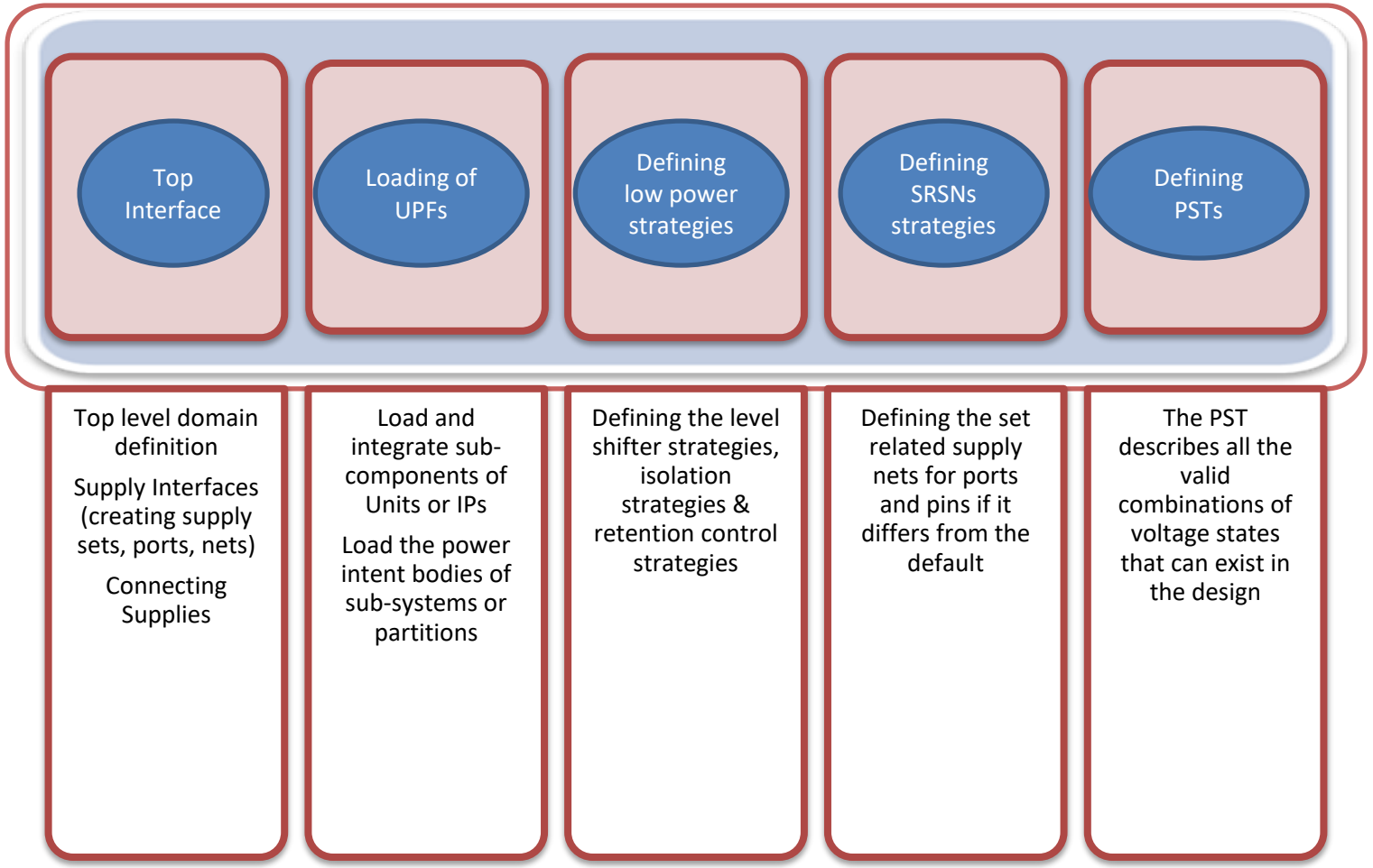
# Low Power

- Power Management is Critical Today
- Driving for finer process technology
  - Smaller, lighter products
  - Longer battery life
  - More functionality
- Dynamic power
  - Signal switching consumes energy
  - Was the major contributor to power consumption
- Static power
  - Static leakage can consume 50% of power!
  - Now the major concern for power optimization

# Motivation :Traditional Vs Proposed

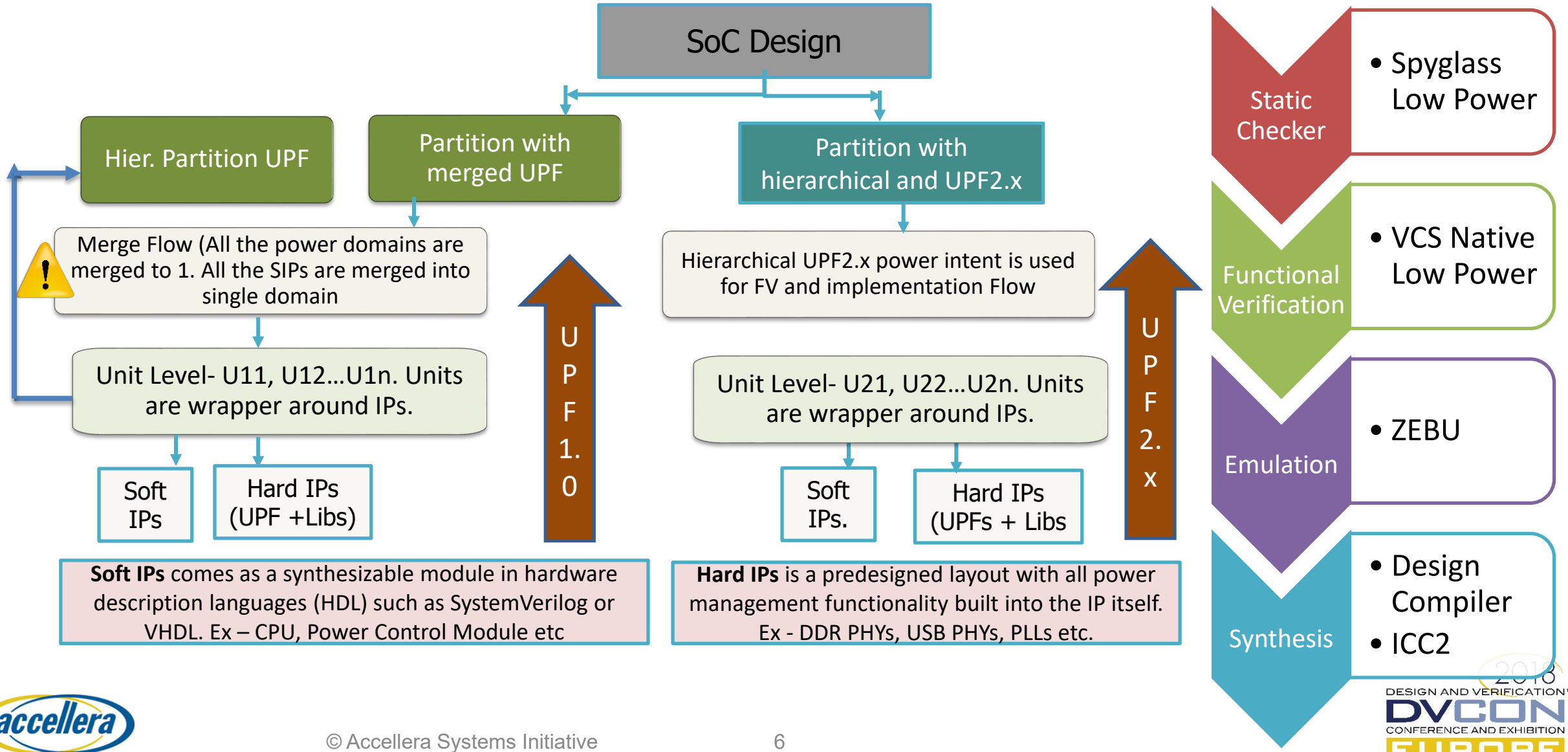
- Complexity of the Design
- IP Sourced from multiple vendor – Internal, External & Hard IPs.
- Need of the hour is Abstraction
- Physical Design Limitation
- Multiple Flows for Functional Verification vs Implementation
- Large Number of Power and Voltage Domains
- Adoption of new feature of latest power intent

# Power Intent Body



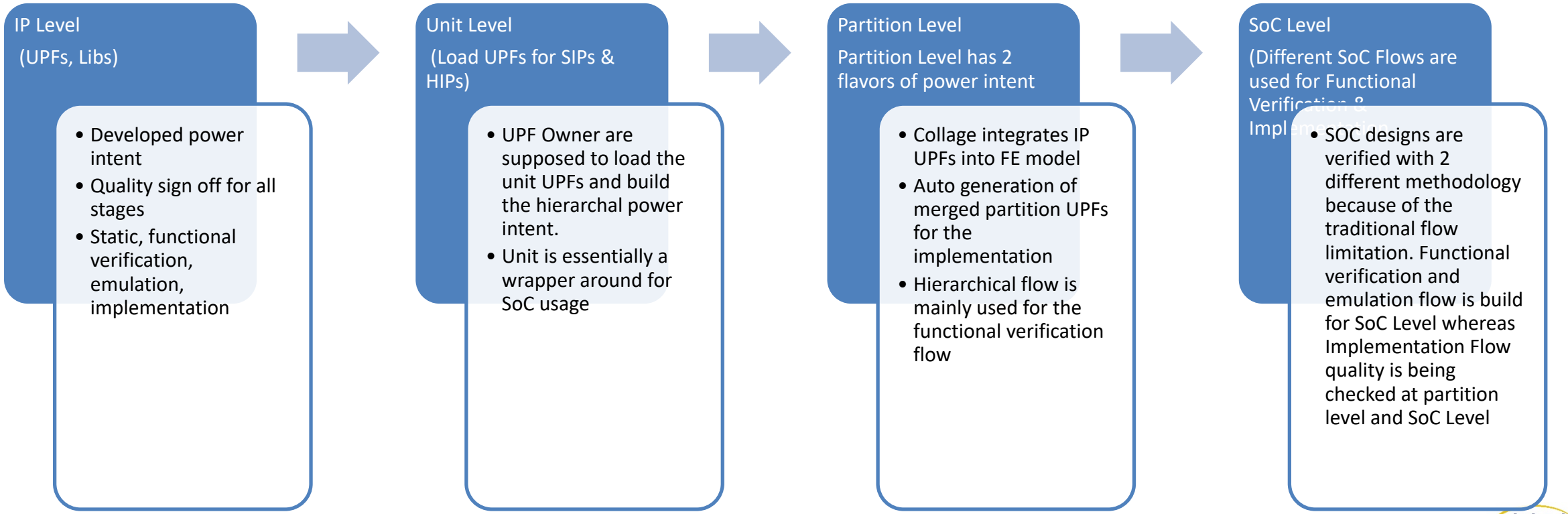

```
    create_supply_net
    "vcc_in"
    create_supply_port
    -direction "in"
    "vcc_in"
connect_supply_net "vcc_in" -ports "vcc_in" create_supply_net
"vcc_out"


    create_power_domain "vccsa_domain_merge" \
                -supply {extra_supplies_1 VCCSA} \
                -supply {extra_supplies_2 VCCSTL}


set_isolation punit_vccsa_vccstl_iso_dummy \
-domain              "vccstl_domain_merge" \
-isolation_supply_set   "VCCSTL" \
-isolation_signal
"punit_wrap/punit/ptpcbclk/ptpcbclk_soft_supply" \
-isolation_sense       "low" \
-location            "self" \
-elements [list \ "punit_wrap/punit/ptpcbclk/PllXclkSyncFnn4H"
\


set_port_attributes -ports [join
$iov_clamp_value_1_elements] -clamp_value

add_power_state "VCCSA" -state "ps_VCCSA_LV" "-supply_expr
\{power == `\{FULL_ON,0.65\}\} -simstate NORMAL
```

# Introduction to Hybrid Methodology



# Intel's SoC Design Integration Flow

Low Power Specs are defined as Micro Power Architect and it included top interfaces, partitions level interfaces, crossing table & bump details.



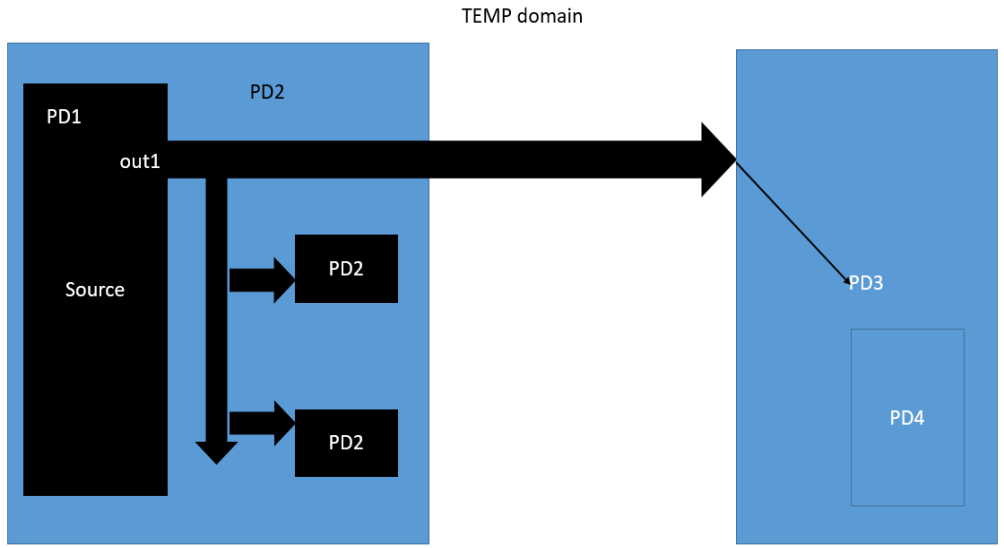
# Hybrid Flow Implementation

- Client SoC with more than 1billion gates design
- SoC Contains 34 partitions with memories, power management, PCI, CPU, Display blocks
- 5 different partition design blocks
- Multiple Flows for Functional Verification vs Implementation
- Large Number of Power and Voltage Domains
- Adoption of new feature of latest power intent

| Block Type | Cell count | Number of power domains |
|---|---|---|
| Power management | ~48000 | 3 |
| Legacy | ~24000 | 3 |
| Fabric | ~87000 | 3 |
| IOP | ~17000 | 3 |
| MC Main | ~4000 | 3 |

# Challenges of Hybrid Methodology

- In **Source-Sink isolation strategy**, "HETEROGENEOUS_FANOUTS" Warning (Isolation is skipped).
- Here same signal out1 is given as input to PD2 block and also for PD3 block ..
- Sinks related to PD2 are not real sinks and sink PD3 is a real one .Would like to exclude sinks related to PD2.

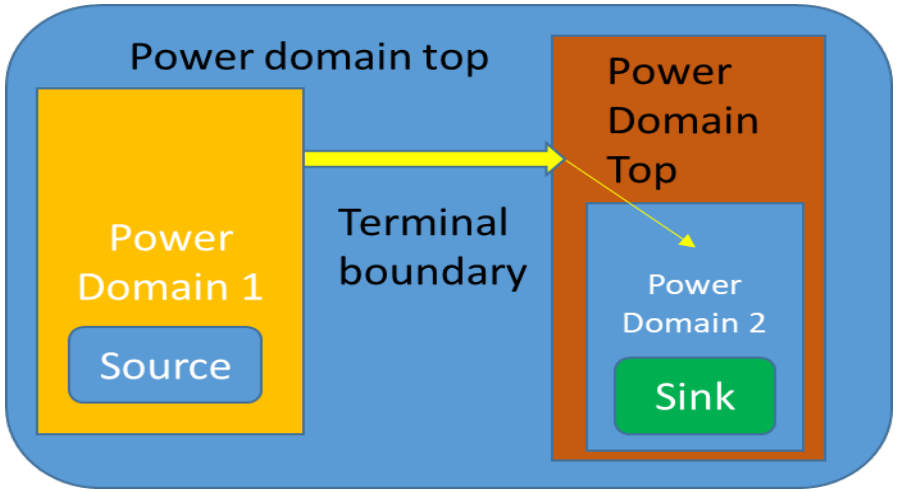



```
set_design_atribute -elements <list of elements> -attribute
SNPS_treat_as_unconnected TRUE
```

# Challenges in Hybrid Flow Implementation

**Terminal boundary issue:**

Isolation cell with source and sink strategy got matched but isolation cell is not placed due to crossover contain a wire which belongs to terminal boundary




But due to terminal boundary set on BLK1 element and signal is crossing via wire which is used in BLK1 is breaking this connection .

Attribute used: set_design_attributes -elements {soc_tb/soc/par_punit/punit_wrap/punit/assert_xcheck_punit soc_tb/soc/par_punit/punit_wrap/punit/assert_ifc_stability_check_punit} -attribute SNPS_treat_as_unconnected TRUE

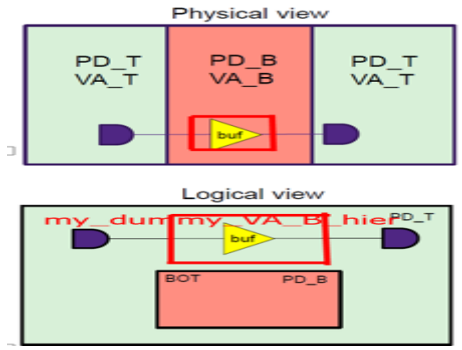
# Physical Design challenges…

- Power switch insertion issues

```
create_power_switch sw_northpeak_vccsa_PGD -domain northpeak_wrap/northpeak/pd_northpeak_vccsa_PGD
-output_supply_port {gtdout northpeak_wrap/northpeak/vccsagnpk} -input_supply_port {vcc_in northpeak_wrap/northpeak/vccsa}
-control_port {a northpeak_wrap/northpeak/pgcb_npk_vnn_fet_en_b} -on_state {ps_VCCSA_GT_LV vcc_in {!a}}
```

```
Error: Supply net northpeak_wrap/northpeak/vccsa cannot be connected to the pin
soc_pg_pwrup_cell_sagnpk_wrap/ps_ebb_bottom1__snps_pd_northpeak_vccsa_PGD__sw_northpeak_vccsa_PGD_snps_e05psbf16an1q13x5_R0_C0_308/vcc_in
in domain soc_pg_pwrup_cell_sagnpk_wrap/pd_soc_pg_pwrup_cell_sagnpk_wrap. (UPF-031)
Error: problem in connect_supply_net
       Use error_info for more info. (CMD-013)
```

- Shadow domain solution for optimization



# Physical Design Challenges..

- IC Compiler 2 demands matching between states in top level PST and sub hierarchy PST. The solution for this is to disable lower level PST.

```
--------------------------------------------------------------------------------
PST Name                :  pst
Scope                   :  / (top scope)
--------------------------------------------------------------------------------
Supplies                :  vccsa         | vccsagpsf1  | vccstg    | vss       |

States
 (1) S_VCCSTG_on_LV     :  ps_VCCSA_HV [1.100]  | ps_VCCSAGPSF1_HV [1.100]  | ps_VCCSTG_LV [0.650]  | ps_VSS_0p0 [0.000] |
 (2) S_VCCSA_on_LV      :  ps_VCCSA_LV [0.650]  | ps_VCCSAGPSF1_LV [0.650]  | ps_VCCSTG_HV [1.100]  | ps_VSS_0p0 [0.000] |
 (3) S_VCCSAGPSF1_on_LV :  ps_VCCSA_LV [0.650]  | ps_VCCSAGPSF1_LV [0.650]  | ps_VCCSTG_HV [1.100]  | ps_VSS_0p0 [0.000] |
 (4) S_VCCSTG_OFF       :  ps_VCCSA_LV [0.650]  | ps_VCCSAGPSF1_LV [0.650]  | ps_VCCSTG_OFF [off]   | ps_VSS_0p0 [0.000] |
 (5) S_VCCSA_OFF        :  ps_VCCSA_OFF [off]   | ps_VCCSAGPSF1_OFF [off]   | ps_VCCSTG_LV [0.650]  | ps_VSS_0p0 [0.000] |
 (6) S_VCCSAGPSF1_OFF   :  ps_VCCSA_LV [0.650]  | ps_VCCSAGPSF1_OFF [off]   | ps_VCCSTG_LV [0.650]  | ps_VSS_0p0 [0.000] |
 (7) S_ALL_RAILS_OFF    :  ps_VCCSA_OFF [off]   | ps_VCCSAGPSF1_OFF [off]   | ps_VCCSTG_OFF [off]   | ps_VSS_0p0 [0.000] |
--------------------------------------------------------------------------------
```

Fig. 3.5 Top level PST

```
--------------------------------------------------------------------------------
PST Name            :  ann_pst_psf20_top
Scope               :  psf1_wrap/psf20_icl_psf1
--------------------------------------------------------------------------------
Supplies            :  psf1_wrap/psf20_icl_psf1/vccsa  | psf1_wrap/psf20_icl_psf1/vccsagpsf1  | psf1_wrap/psf20_icl_psf1/vss |

States
 (1) psf_vcc_ACTIVE :  vcc_FULL_ON [0.650]  | vcc_gated_FULL_ON [0.650]  | gnd_FULL_ON [0.000] |
 (2) psf_vcc_SLEEP  :  vcc_FULL_ON [0.650]  | vcc_gated_OFF [off]  | gnd_FULL_ON [0.000] |
 (3) psf_vcc_OFF    :  vcc_OFF [off]      | vcc_gated_OFF [off]  | gnd_FULL_ON [0.000] |
--------------------------------------------------------------------------------
```

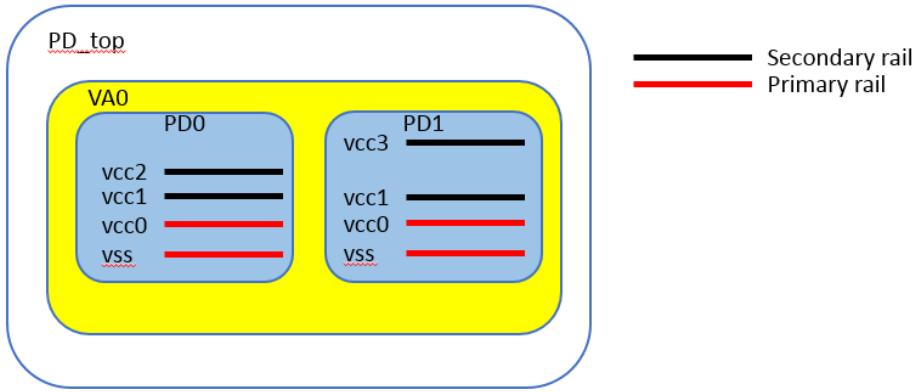
Fig 3.6 Missing 1.1 V modeling

```
--------------------------------------------------------------------------------
PST Name :  pst_psf20_top
Scope    :  psf1_wrap/psf20_icl_psf1
--------------------------------------------------------------------------------
Supplies :  psf1_wrap/psf20_icl_psf1/vccsa    | psf1_wrap/psf20_icl_psf1/vss  |

States
--------------------------------------------------------------------------------
```

Fig 3.7 No states at all

# Physical Design challenges

- **Missing supply states issue:** A group of hierarchical PDs in the same VA will share same primary supplies but if there is a mismatch in secondary domains, as long as at least one domain contains the required supply as available supply, tool can use the hierarchy of the domain to put the cell anywhere in the VA physical shape.



# Advantages of Moving to Hybrid flow

- Hierarchical methodology with hybrid flow supports partitioning, parallel development, and reuse.
- The UPF complexity is very much reduced.
- Supply sets provides an abstraction and allows designers to define their power intent without having to create the actual supply nets
- Usage of hierarchical flows at all the stages of design flow eliminates the usage of two different UPFs.
- Advantages of add_power_state
- The usage of set_design_attribute allows the propagation of power information to the lower levels of design hierarchy

# Questions

Finalize slide set with questions slide