Hybrid Emulation: Accelerating Software driven Verification and Debug

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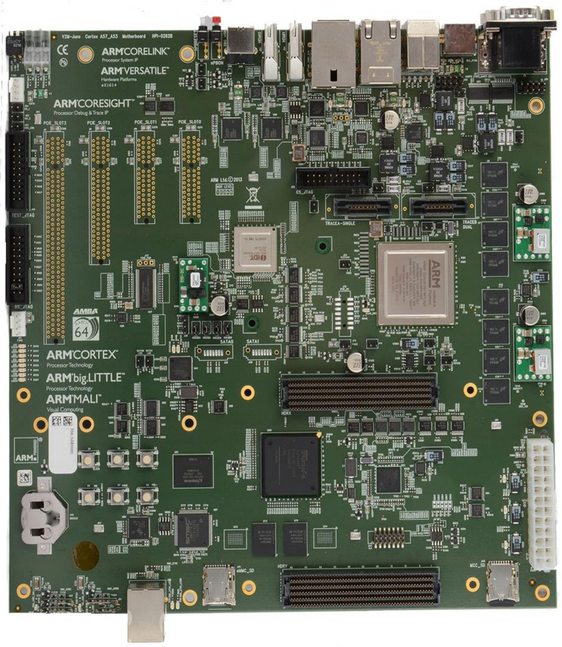
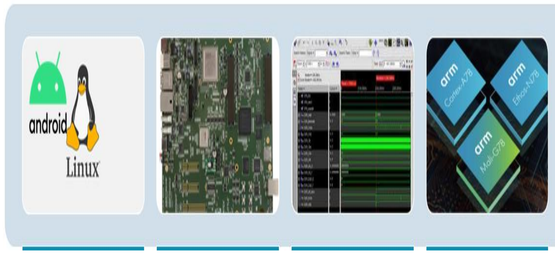
Existing Platform



- FPGA based Juno Platform
- Onboard FPGA where GPU will be configured
- Runs at GHz speeds

FPGA Platform Challenges

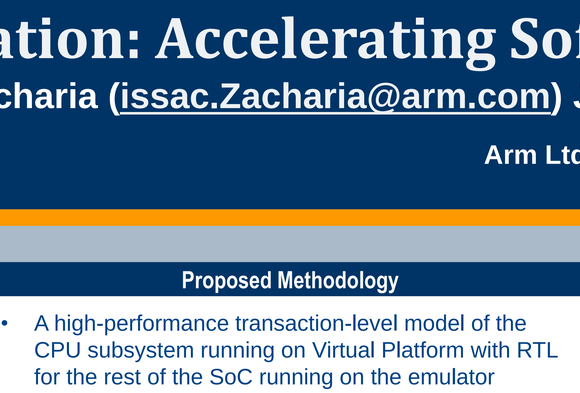


- Debugging HW/SW issues using real OS Apps on FPGA is challenging due to low design visibility
- Issues reported in different verification platforms/tools typically are not cross reproducible
- Complex real OS App issues could take weeks to generate the stimulus and reproduce at unit level simulation platforms
- Mali® GPU HW and SW live debug was challenging in present platform setup

Proposed Methodology

- A high-performance transaction-level model of the CPU subsystem running on Virtual Platform with RTL for the rest of the SoC running on the emulator
- Enables the software to execute at virtual platform speeds
- Higher performance for software-driven hardware verification even when RTL for critical blocks isn't available
- Early architecture validation and software development
- Easier platform upgradability and Much better design debug visibility
- Supports different debug methods over FPGA platform such as waveform, Smart memory debug tools, memory dump, tarmac, capture replay, monitors etc

Integration Block Diagram



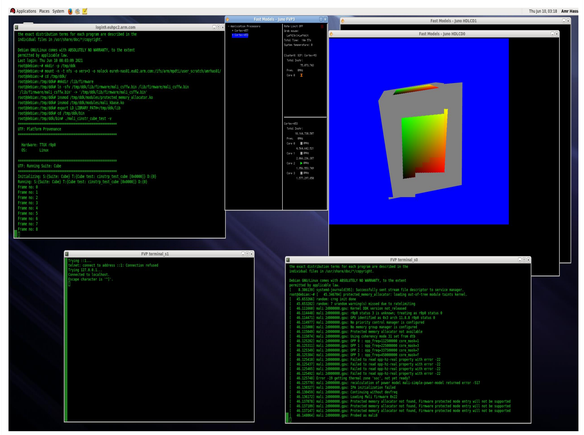
Platform Integration

- Replaced RTL CPU and GIC with Arm Cortex A55 and GIC 600 fast model on the virtual platform
- Converted RTL memory to smart memory to enable the CPU to access it via backdoor
- Smart memory acts as shared memory which is visible to both virtual and RTL platforms
- CPU access the memory within the virtual platform and other peripherals in the RTL through TLM bridge connected to the CCI550
- GPU access the memory through CCI550 bridge

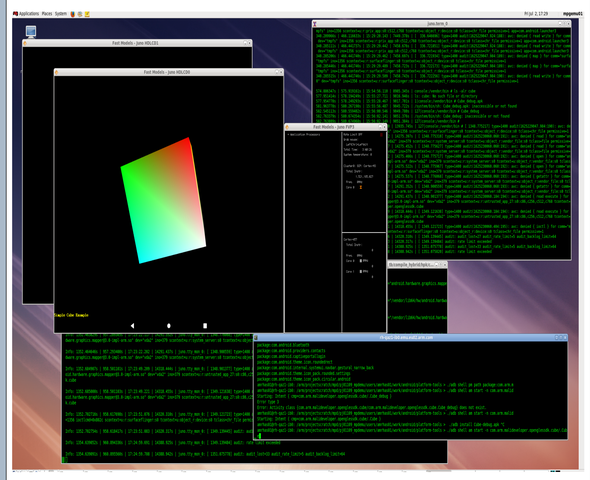
Platform Integration

- Integrated TLM bridges to facilitate the communication between virtual and RTL platform
- Built-in models available by EDA Hybrid toolchain to take care of RTL to virtual change in form of transactions to/from CPU.
- Internally, these models use SCEMI-DPI to transfer data back and forth on TLM channel across boundary
- The router on the virtual side is an EDA vendor specific interconnect, which can be configured to define the number of masters and slaves, width, address space etc. of the virtual components

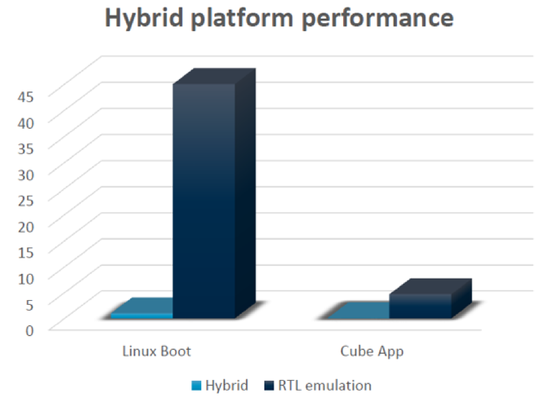
Cube application on Debian Buster 11



Cube Application on Android 10



Performance results



Test	Runtime
Linux Boot	62 sec
Android 10	2640 sec
Debian Buster 11	185 sec

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- Helped reproducing the hardware and software issues captured in FPGA platform which enables much better turnaround time for the debug and corresponding patch validation
- Caters an effective co-ownership of FPGA based challenges in Software development, therefore it is certainly not a replacement of our existing FPGA platform
- Observed significant gain with Hybrid usage in Emulator which led us to explore and deploy it on bigger ecosystems of Arm

Reference

Developer. Arm tools-and-software/development-boards/Juno-development-board