2022 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Hierarchical UPF: Uniform UPF across FE & BE

Dipankar Narendra Arya

Balaji Vishwanath Krishnamurthy

Aditi Nigam

Tahir Ali

intel

accellera SYSTEMS INITIATIVE

Agenda

- Introduction
- UPF Consumption across SoC
- PoC on Hierarchical UPF
- Guidelines for SoC team
- Summary and Current Status

Introduction

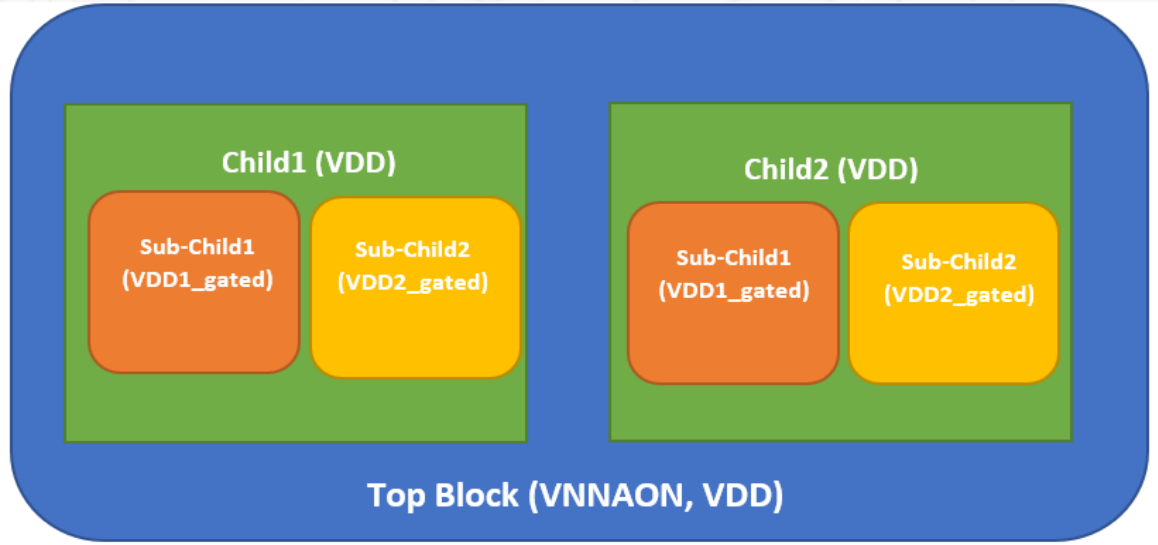
- Unified Power Format (UPF) – 1801 IEEE Std. – used for power intent specification
  - Tcl based
  - Verification and implementation of multi-well and power gating scenarios
- UPFs Styles
  - Hierarchical
  - Flat
  - Merged

Introduction (contd.)

- Hierarchical

```
create_supply_net VDD
…
create_suppy_port VDD
…
connect_supply_net VDD -ports VDD
…
create_supply_set  ss_VDD -function {power VDD} -ground {VSS}
create_power_domain PD -elements {.} -supply "primary ss_VDD"
```

```
...
load_upf child_block.upf -scope child1
load_upf child_block.upf -scope child2
...
```



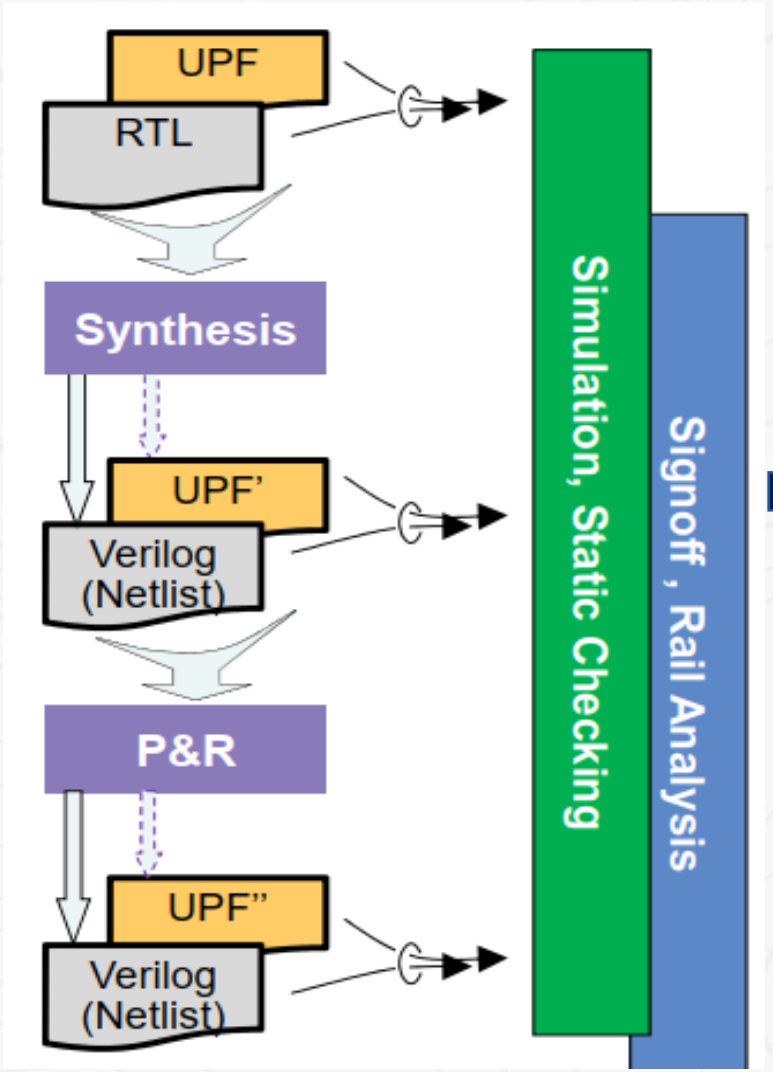
- Flat

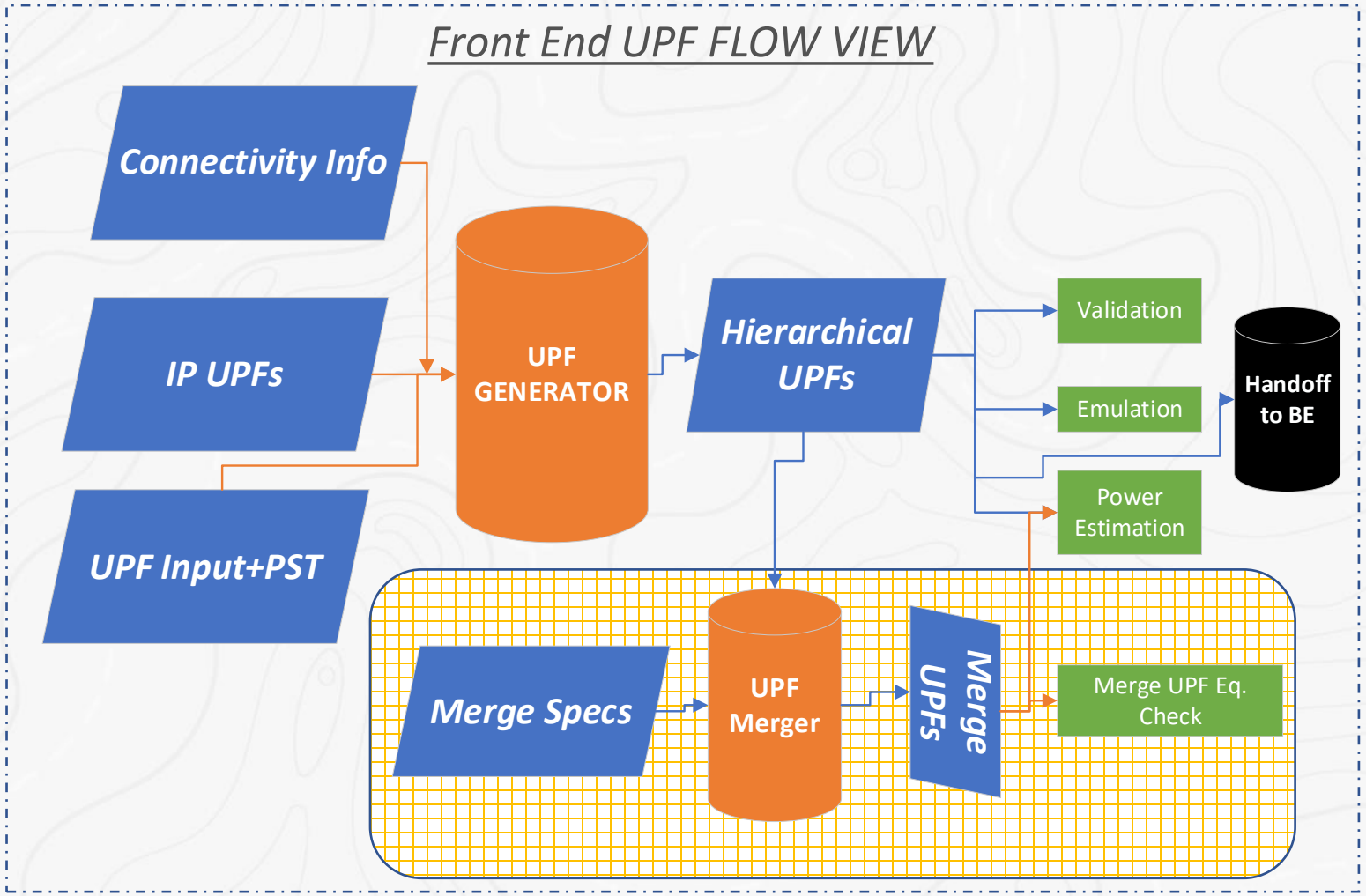
```
create_supply_net VNNAON
…
create_suppy_port VNNAON
…
connect_supply_net VNNAON -ports VNNAON
…
create_supply_set ss_VNNAON -function {power VNNAON} -ground {VSS}
…
create_power_domain PD_top -elements {.} -supply "primary
ss_VNNAON"
create_power_domain PD_child1 -elements {child1} -supply "primary
ss_VDD"
create_power_domain PD_child2 -elements {child2} -supply "primary
ss_VDD"
```

- Merged

```
create_power_domain PD_child_merged -elements {child1 child2} -supply
"primary ss_VDD"
```

UPF Consumption across SoC





UPF Consumption across SoC (Contd.)

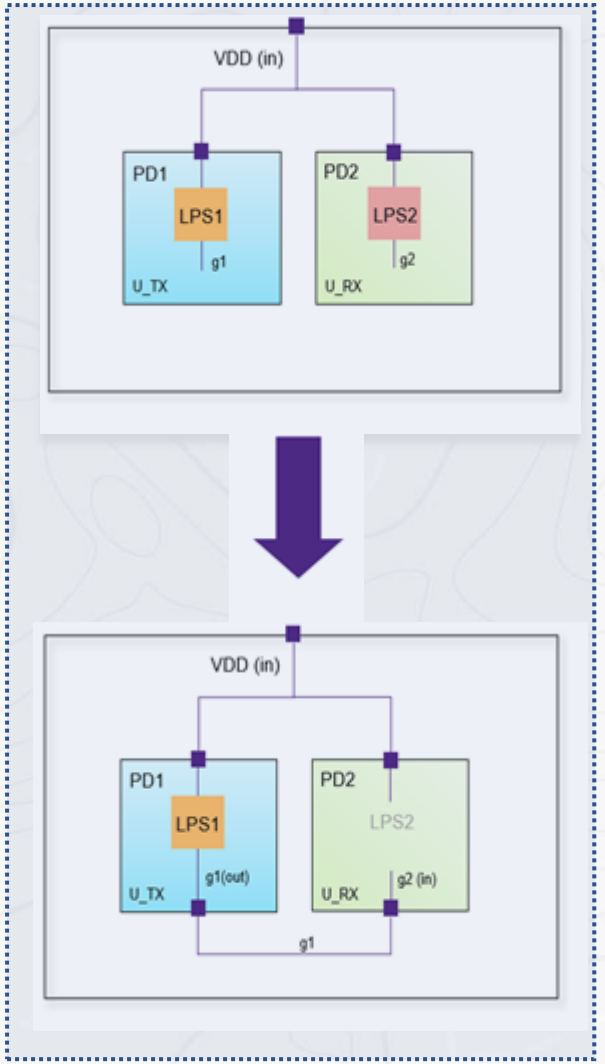
- RTL/TB integration tool stiches IP level UPFs and generates block level UPF – Hierarchical by default
- Back-end implementation can't consume hierarchical UPF files in past – issues seen in implementation tools
  - Difficulty in understanding IP level UPFs
  - PST conflict because of IP level PSTs
  - Power domain explosions
  - PDOI routing b/w child blocks is buggy
  - Power intent of Eq. gated power domain were not realized properly in APR tools
- Merged UPF is used – for ease of implementation
  - Generation is tedious – script based - too many configurations and manual interventions – error prone
  - TAT for initial setup – 7-8 weeks; 2-3 weeks for any subsequent updates
  - No industry standard tool available for generation
  - Can't be used for verification flows as stubbing not possible (selective enabling/disabling of blocks)
- Make sure Hierarchical UPF $\approx$ Merged UPF
  - Formal Eq. (FEV) checking tool – same RTL on both side- not full proof, bugs seen in the past.
  - Only Gate Level Simulation can confirm complete equivalence – late in the design cycle, around code freeze.

POC on Hierarchical UPF

- Consuming Hierarchical UPF for BE – same power intent everywhere – no additional overheads for validation – reduced TAT
- POC was done on a complex partition
  - Equivalent PSWs (would have already been merged in Merged UPF)
  - Isolation strategies – parent as well self
  - ELS
  - Multiple SIPs and HIPs
- All major tools and flows from FE to BE were run
- Learnings and Guidelines published for the next project

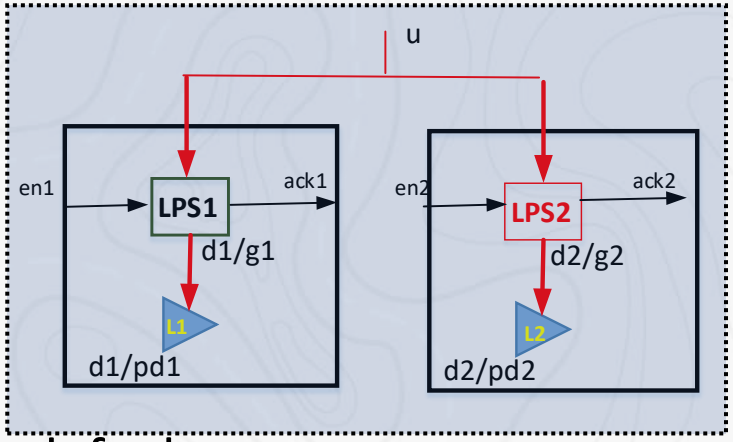
POC on Hierarchical UPF – Issues seen

- FE LP Static Checks – no issues
- FE Handoff synthesis
  - Unable to insert ISO at parent location in last gen synth tool; not an issue in next gen synth tool
  - Missing CSNs for internal – errors, as unable to derive the related voltage
- BE Handoff synthesis – same as above
- APR
  - Flow crashes initially – improper buffer/inverter placements
  - Additional option/attribute to merge eq. VA and PSW required

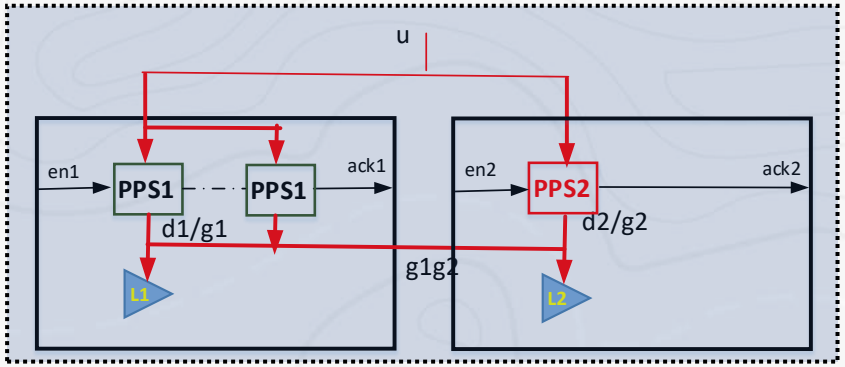


POC on Hierarchical UPF – Issues seen (Contd.)

- BE LP static checks
  - Bug related to shared VA attribute used in APR – fixed later
  - Many false violations related to PSW merging – waived



- LVS Check
  - Output nets of PSWs (distinct for the tool) are not shorted by default
  - Single VA can have one net only – logically connected to primary power but not physically connected – causing LVS opens
  - PSW supply nets need to be shorted in the UPF- use “set_equivalence” or port out to top and short
- RV Checks – no issues
- LP FEV
  - Expected power-grid violations related to PSW merging
  - Violations related to biasing



Guidelines for SoC team

- Use Localized UPFs – copy all child UPFs in a single dir. – replace paths with normalized paths – ease of shipping
- Strict compliance to Intel-wide UPF 2.1 templates – avoid mix-n-match of versions
- Well-biasing for supply sets in all the UPFs – LP static tool can not detect- Synthesis will fail
- Value of attribute in “set_design_attribute” command should be consistent – otherwise flow error
- Do not use legacy/deprecated constructs/switches – “set_domain_supply_net”, “extra_supplies_#”
- Port out gated supplies to block level UPFs – needed for eq. PSWs and SoC driven PSTs
- CSNs should be done for all the ports across the design – LP lint will throw violation and Synthesis will fail
- Add protection around IP level PSTs and add_power_state commands- SoC driven PST to minimize conflicts
- Bring IP internal nets to block level – to add fillers cells (if needed) during APR

Summary and Current status

- Successful PoC – no major hiccups/QoR degradation
- Decision taken to use hierarchical UPFs for the ongoing projects – Guidelines for SoC team published
- Initial bring-up/integration in FE took some effort – many legacy IPs were not as per guidelines
- Significant reduction in time and resource (as merged UPF generation/validation not required)
- TAT for UPF integration decreased by 60-70% - saving of 8-10 weeks for initial bring up – 2-3 days for subsequent drops
- Compliance to basic principle of consuming same UPF across the flows

Questions