

Has the performance of a sub-system been beaten to death

UVM Framework does it ALL!!

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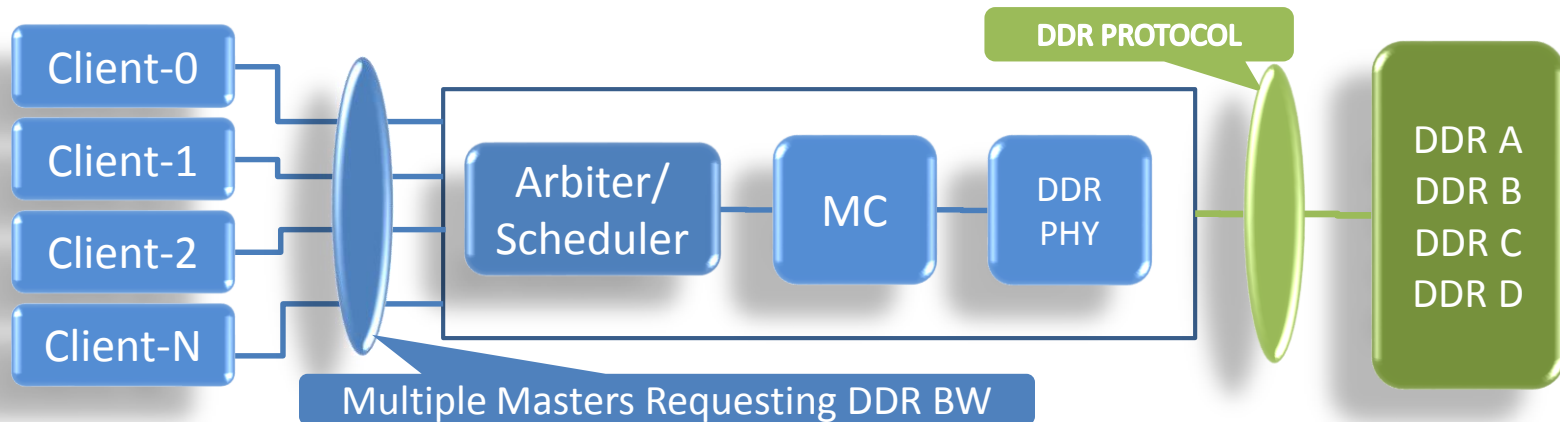
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Agenda

- System Outlook & Complexity
- Verification Scope
- RTL Performance Verification Challenges
- DV Strategies
- Return on Investment [ROI]
- Conclusions
- Q & A

System Outlook & Complexity

- Interconnect & Memory
- Frequency Bump, Increasing complexity, Phy & MC
- Performance budget – Worst Case & Beyond Budget
- DDR Bandwidth and Multiple clients
 - Concurrent cases and Traffic Distribution



Verification Scope

- Synthetic Traces
 - Architectural exploration
 - Modeling corner-case scenarios
 - Stall and starve situations
 - Sign-off best and worst performance numbers
- TRACES
 - Realistic-Traffic (platform traces)
 - Micro-traces and region of interest
 - Replay and workaround identification
- Performance effective configuration settings
- Closure Directive - PCM

RTL PV Challenges

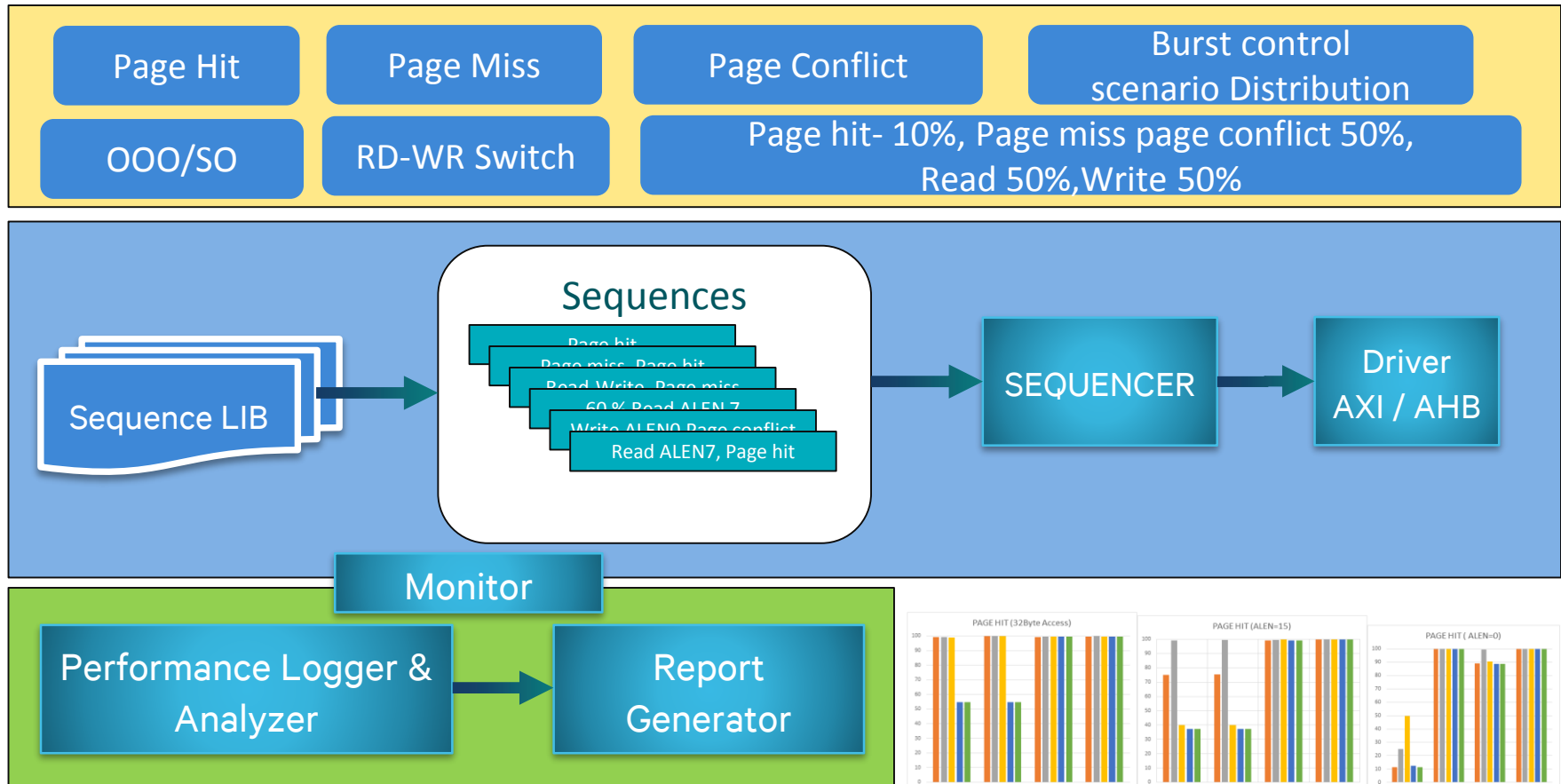
- Beating Timeline-Pressure
 - Low development cost and time.
 - Functional & Performance, Teams vs Teams
- Every clock is important
 - Logical interfaces perfectly tuned.
 - Data sensitive to time-sensitive interfaces
- Micro-Traces
 - Overshooting simulation capacity
- Performance Data space explosion
 - Automated Data mining

RTL PV Challenges

- Looking beyond sub-system
 - Enhancement & Traffic profiling for Master
 - Memory aware transaction scheduling effectiveness
- Closure Directive
 - Performance verification closure How and when??
 - Sign-off criteria across all cores.

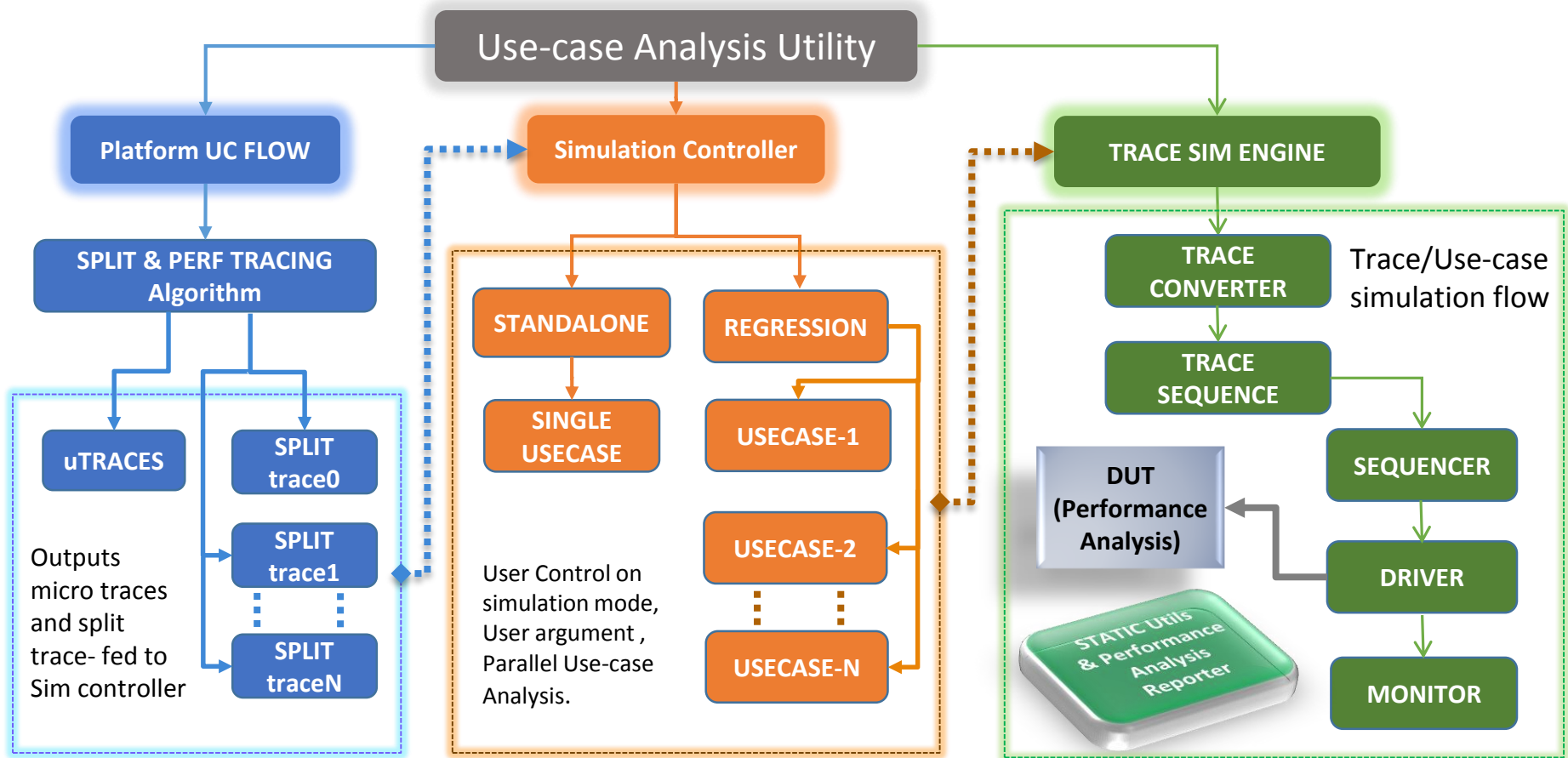
DV Strategies & RTL PV

- Automated UVM Framework



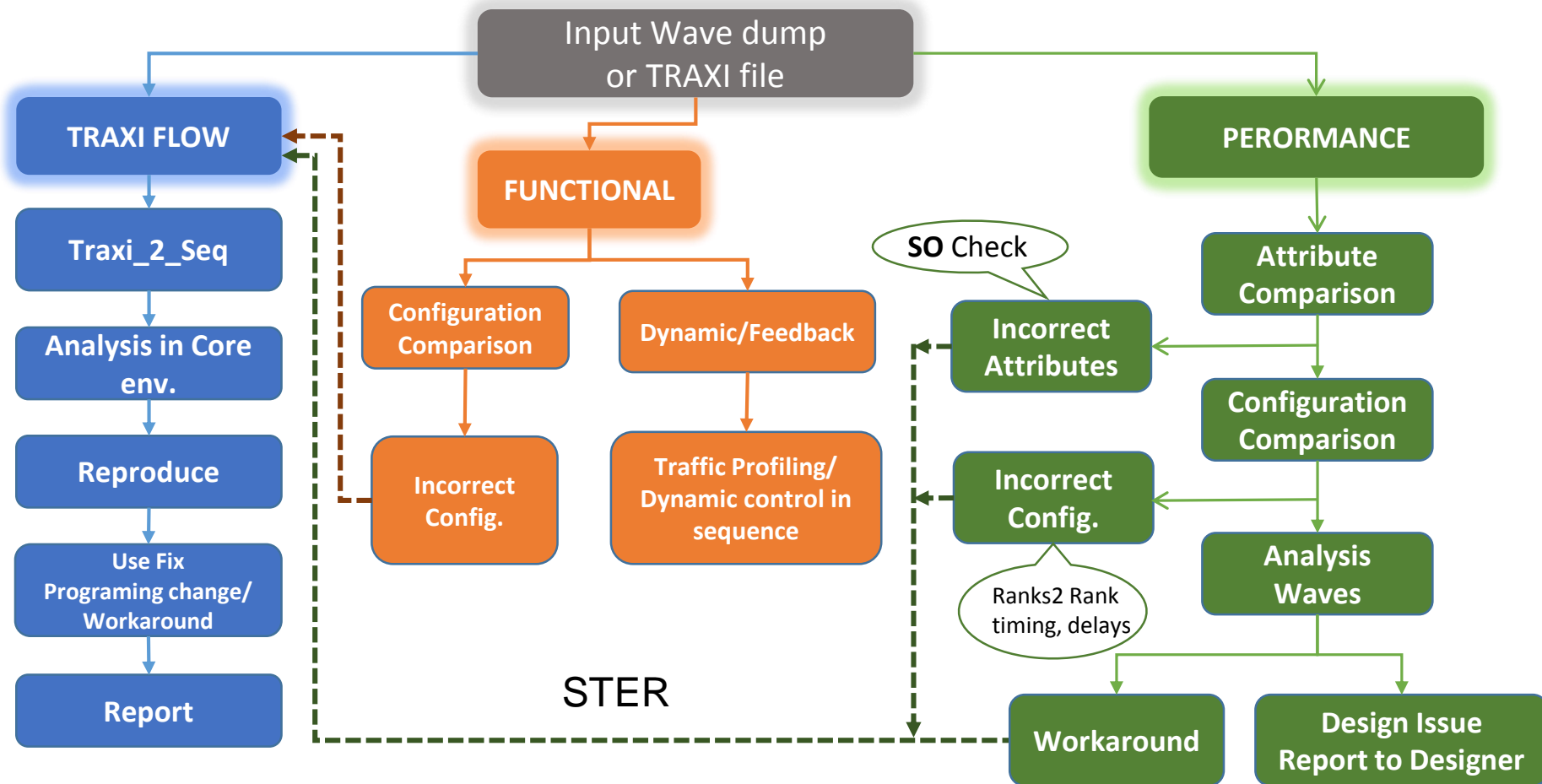
DV Strategies & RTL PV

- Automated UVM Sequence for TRACE infrastructure



DV Strategies & RTL PV

- Platform independent static Analysis infrastructure



DV Strategies & RTL PV

SIGN-OFF Criteria

- Performance Coverage Model(PCM)
 - Insight into quality and depth of traffic
 - Ensure Interesting situations
- DDRX (Theoretical limit vs sim values)
- Buffer occupancy models
 - Use case and Trend analysis
- Bus Coverage models (Re-use) OOO, OT
- Stall and starve models

DV Strategies & RTL PV

SMARTER Plugins

- Online and Offline Analysis Modes
- Micro-traces
 - Iterative and approximation algorithm
 - Similar intent and acceptable deviation
- Dynamic Power Analysis
 - Max B.W region, idle and peak power.
- Functional

ROI

- UVM Framework
 - Seamless migration Vertical and Horizontal Reuse
 - Weeks -> Days
- Regression Infrastructure
 - End-to-End Automation Quick and refined perf-data
 - Overall outlook , exposes traffic pattern limitation
- Platform independent Analysis
 - Control knobs , debug-analysis-report loop Days to hours
 - Analysis and Exploration of Traces from globally distributed teams

ROI

- PVC's
 - Traffic tuner,
 - Issue isolator and highlighter
 - Attribute-Differentiator
 - Configuration comparator
- TRACE Static Analysis – Algorithmic Approach
- Every clock is important

Sign-off & Re-use

Coverage Convergence & Sign-off

- Leverage Functional verification Infrastructure
 - Hookup scalable and modular PVCs
 - PCM
- ✓ Smart Strategies to reduce exposure to late performance bugs due to early engagement
- ✓ Deep dive into RTL exploration for future products

Conclusion

- Complex control intensive design are dreadful to crack
 - PVC's
- Automated UVM & Regression Framework
 - Weeks to Days
- Platform Independent STATIC Analysis
 - Days to Hours
- Beating Time-line pressure UTRACES
- Smart Strategies for Endless Challenges.

Q & A