# Hardware Software Co-verification in Hybrid QEMU/HDL Environment

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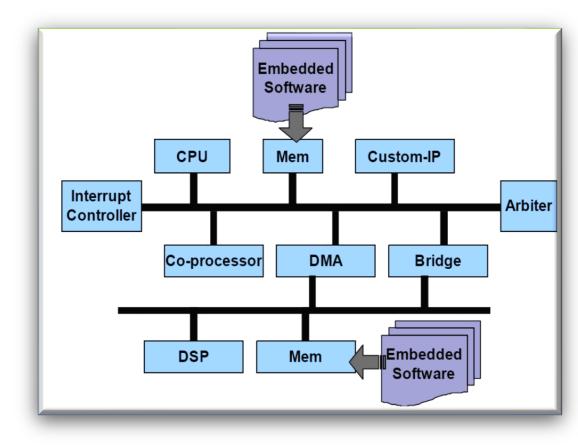






# SoC verification challenges

- Contains complex hardware and embedded software
  - both need verification
  - software on critical-path
- Heterogeneous architecture and hierarchical Networkon-Chip (NoC)
  - Corner case hardware problems
  - System level integration problems
- Standard IP reuse: CPU, DMA, MEM ... side effects:
  - Design size fast growth
  - Slow HDL simulation
- Custom IP-Cores
  - Need cycle accuracy for debugging
  - Cannot be fully verified at block level (out of SoC context)



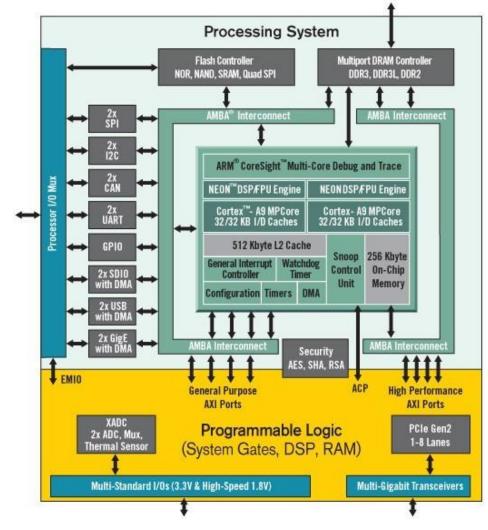




# SoC Designs in FPGA Domain

Xilinx Zynq and the like...

- Processing System
  - ARM Cortex CPU
  - Standard I/O peripherals
- Programmable Logic
  - Classic FPGA used for:
    - More peripherals
    - Glue logic & Bridge



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#### Virtual Platforms & Virtual Machines Pros & Cons

- (+) Available earlier than system-level RTL code
- (+) Fast enough for firmware/software development
- (+) Integrated with software development tool-chain
- (-) Not cycle accurate
- (-) Virtual models not available for Custom-IP

#### Virtual Machine



Versatile – many architectures:

- ARM, RISC-V, SPARC, MIPS
- x86, PowerPC, MIPS

#### **Virtual Platforms**

#### **ARM**<sup>®</sup>Fast Models

Virtual Platforms

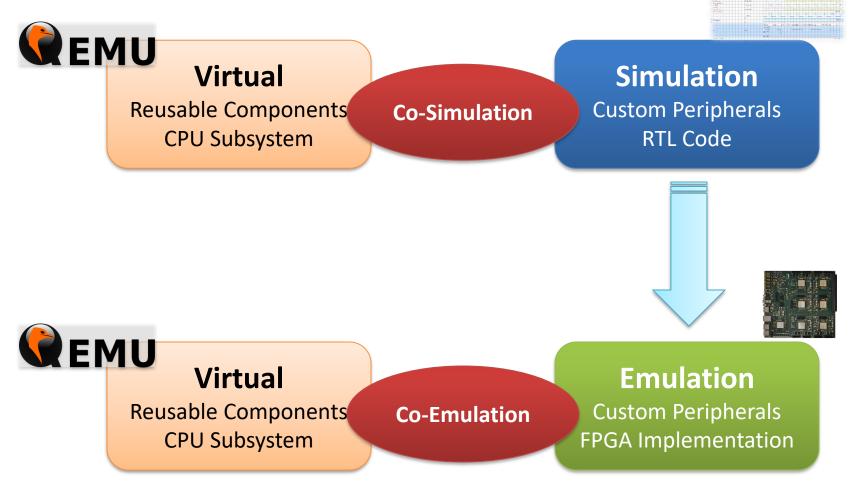








# Hybrid co-simulation and co-emulation

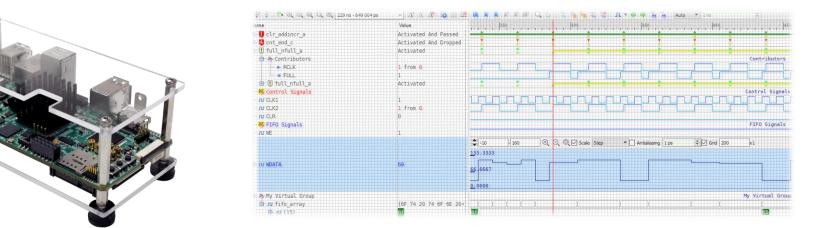


- Custom IP development
- Block-level verification
- QEMU software driven testbench

- SoC Integration & bring up
- Drivers & firmware development
- Complete SoC model for SDK
- QEMU integral part of SoC model











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**QEMU co-simulation with Riviera-PRO** 

# QEMU co-simulation platform

- Parts of the flow:
  - Riviera-PRO Advance Verification Platform
  - -Aldec AXI BFM
  - -Aldec QEMU Bridge
  - -QEMU Emulator







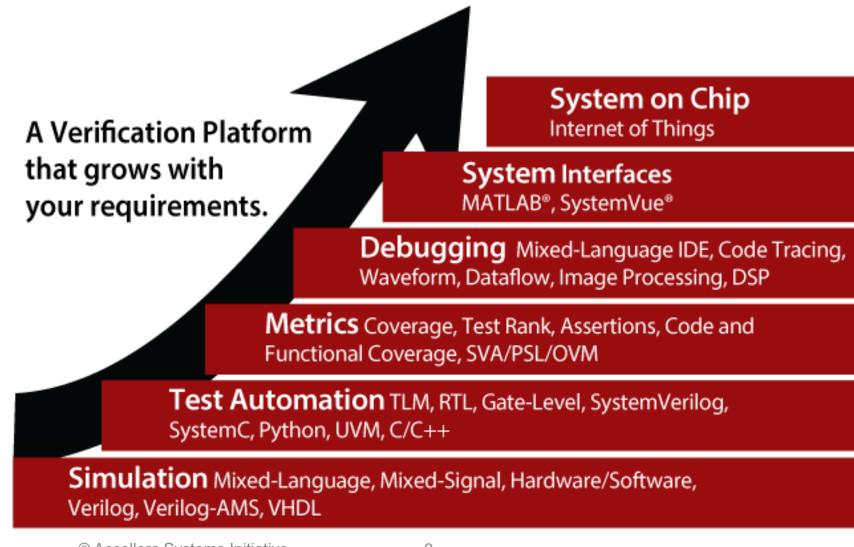
# QEMU co-simulation highlights

- Full debug capabilities of RTL IP Core in Riviera-PRO simulator:
  - Waveforms
  - Hardware Breakpoints
  - Hardware steps
  - Transaction based verification and debug
- Kernel and driver debug via GDB
  - Software Breakpoints
  - Variable probing
- Zynq Linux OS ready to use on QEMU without modifications





## **Riviera-PRO Verification Platform**





# **Riviera-PRO Highlights**

- High Performance Simulation
  - Extensive simulation optimization algorithms
  - Support for latest Verification Libraries: UVM, OSVVM, UVVM, CocoTB and more
- Advanced Debugging
  - Transaction Level simulation end debug
  - Multi-language debug environment (Verilog, VHDL, SystemVerilog, SystemC, Verilog-AMS)
  - Support for MATLAB and Simulink
  - C/C++ debug environment
  - Support for external C/C++ compilers (GCC, Visual C++)
  - UVM Toolbox, Graph and Class Viewer
  - Code tracing, Waveform, Dataflow, FSM window, Coverage, assertions, memory visualization
  - Comprehensive Assertions-Based Verification (SVA and PSL)
  - Advanced Code and Functional Coverage
  - User-defined test plan linking with coverage database
  - Plot Viewer and Image Viewer





# **QEMU** Highlights

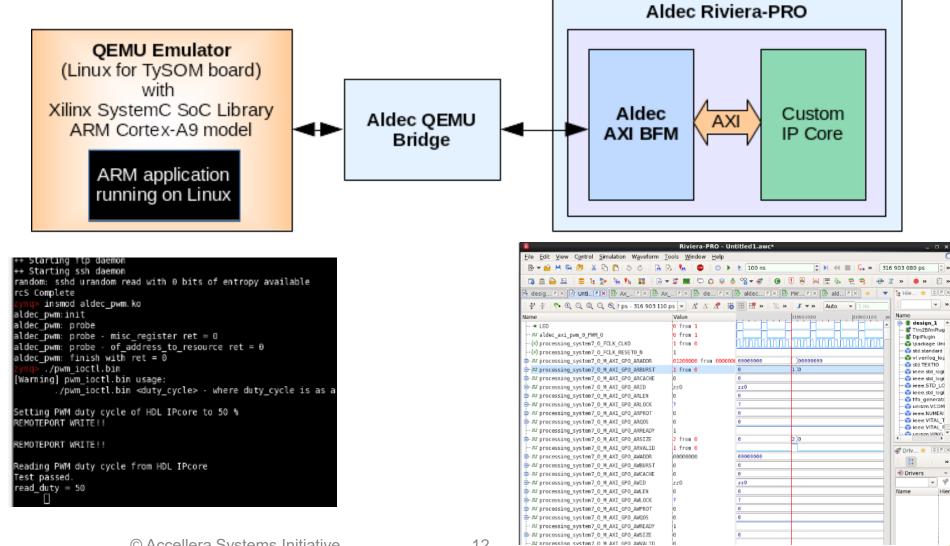
- Free and open-source
- Fast software emulator
- Supports many machines:
  - Xilinx-zynq-a9
- Supports many ARM processors:
  - ARM926
  - ARM946
  - Cortex-A8
  - Cortex-A9
  - Cortex-A15
  - Cortex-A53
  - Cortex-A57







## Connecting QEMU with Riviera-PRO





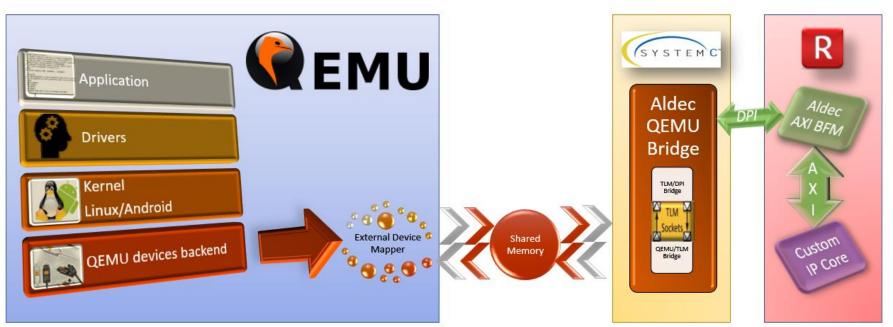
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CONFERENCE AND EXHIBITION

## Aldec QEMU Bridge



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aldec_pwm	
aldec_pw	
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	<pre>m: probe - of_address_to_resource ret = 0</pre>
	<pre>n: finish with ret = 0</pre>
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	pum_ioctl.bin usage:
	<pre>/pwm_ioctl.bin <duty_cycle> - where duty_cycle is as</duty_cycle></pre>
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Reading P	PWM duty cycle from HDL IPcore
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# AXI BFM – HDL site QEMU interface

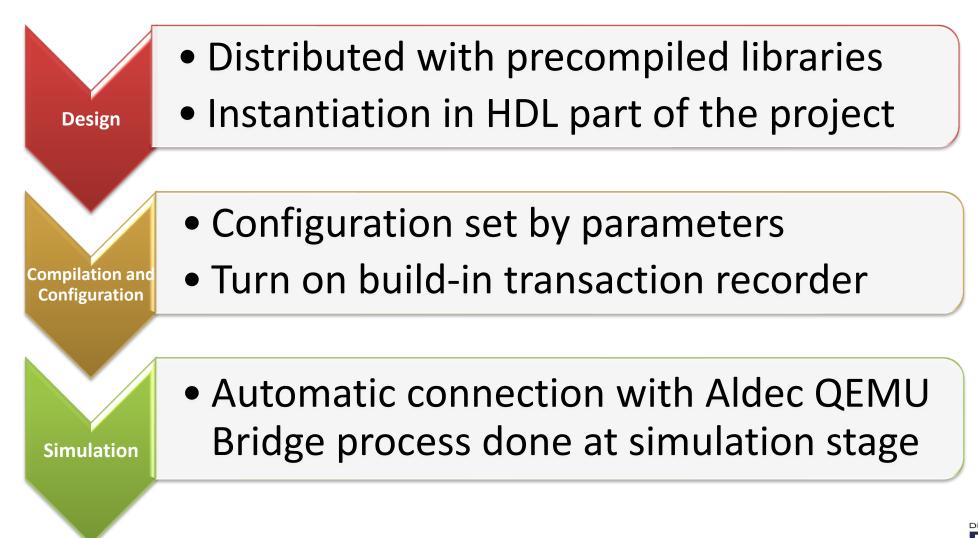
- AXI 3 Master
- AXI 3 Slave
- AXI 4 Master
- AXI 4 Slave
- AXI 4 Lite Master
- AXI 4 Lite Slave
- AXI 4 Stream Master
- AXI 4 Stream Slave

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🖨 👖 aldec_axi_bfm_qemu (RO)		/home/radekn/Aldec/Riviera-PRO-2017.06-x
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🐺 Ax_Axi3MasterBFM Name: aldec_	axi_bfm_qemu	
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🖽 Ax_Axi3SlaveBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 Ax_Axi4LiteMasterBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
😰 Ax_Axi4LiteMasterBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 Ax_Axi4LiteSlaveBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🔁 Ax_Axi4LiteSlaveBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 Ax_Axi4MasterBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🔁 Ax_Axi4MasterBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 Ax_Axi4SlaveBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
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🌇 Ax_Axi4StreamMasterBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🕼 Ax_Axi4StreamMasterBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 Ax_Axi4StreamSlaveBFM	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
😰 Ax_Axi4StreamSlaveBFMcore	Module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 TransactionRecorderAxi3	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🌇 TransactionRecorderAxi4	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
🥵 TransactionRecorderAxi4Lite	Top module	/home/radekn/Aldec/Riviera-PRO-2017.06-x
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# Aldec AXI BFM usage





#### AXI BFM instance in HDL Code

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<b>86</b>							
765	.AWVALID(processing system7 0 M AXI GP1 AWVALID),	« ***	N	lame	Design unit	Library	
766	.BID(processing system7 0 M AXI GP1 BID),			🗦 書 design_1	design_1	xil_defaultlib	
767	.BREADY(processing system7 0 M AXI GP1 BREADY),			🖶 ≢ axi_bram_ctrl_0	design 1 axi bram ctrl	0)⊧xil defaultlib	
768	.BRESP(processing system7 0 M AXI GP1 BRESP),			🕀 🛊 axi_bram_ctrl_0_bram	design_1_axi_bram_ctrl_	0) xil_defaultlib	
769	.BVALID(processing system7 0 M AXI GP1 BVALID),			🕀 ≢ axi_cdma_0	design_1_axi_cdma_0_0(	d⊢xil_defaultlib	
770	.RDATA(processing system7 0 M AXI GP1 RDATA),			🕀 ≢ axi_mem_intercon_1	design_1_axi_mem_inter	c⊧ xil_defaultlib	
771	.RID(processing system7 0 M AXI GP1 RID).			🕀 🛊 axi protocol converter 0	design 1 axi protocol co	p∲ xil defaultlib	
772	.RLAST(processing system7 0 M AXI GP1 RLAST),			🕀 ≢ master 0	Ax Axi3MasterBFM	aldec axi bfm qemu	
773	.RREADY(processing system7 0 M AXI GP1 RREADY),			🕀 🛊 master_1	Ax_Axi3MasterBFM	aldec_axi_bfm_qemu	
774	.RRESP(processing system7 0 M AXI GP1 RRESP),			⊕- ≢ slave_0	Ax_Axi3SlaveBFM	aldec_axi_bfm_qemu	
775	.RVALID(processing system7 0 M AXI GP1 RVALID),			🗘 @INITIAL#829_0@		xil_defaultlib	
76	.WDATA(processing system7 0 M AXI GP1 WDATA),			🗘 @INITIAL#841_1@		xil_defaultlib	
777	.WID(processing system7 0 M AXI GP1 WID),			🗄 📲 gibi	glbl	xil_defaultlib	
778	.WLAST(processing system7 0 M AXI GP1 WLAST),			🔤 📲 TIm2BfmPlugin	TIm2BfmPlugin	aldec_axi_bfm_qemu	
779	.WREADY(processing system7 0 M AXI GP1 WREADY),			🔤 📲 DpiPlugin	DpiPlugin	aldec_axi_bfm_qemu	
780	.WSTRB(processing system7 0 M AXI GP1 WSTRB),			🛶 🎲 \package UnitScopePackage_1\	UnitScopePackage_1	aldec_axi_bfm_qemu	
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785	DATA BUS WIDTH(64),			🗝 🌍 ie Language: VHDL	NUMERIC_STD	ieee	
786	.ADDRESS WIDTH(32),			a Design Unit: standard ram_ctrl_funcs	axi_bram_ctrl_funcs	axi_bram_ctrl_v4_0_10	)
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88 🖻	slave 0 <sup>-</sup> (			🛶 🌍 unisim.VCOMPONENTS	VCOMPONENTS	unisim	
789	.ACLK(processing system7 0 FCLK CLK0),			🗝 🌍 ieee.VITAL_Timing	VITAL_Timing	ieee	
90	.ARESETn(processing system7 0 FCLK RESET0 N),			🗝 🌍 ieee.VITAL_Primitives	VITAL_Primitives	ieee	
791	.ARADDR(axi mem intercon 1 M01 AXI ARADDR),		11	🗝 🌍 unisim.VPKG	VPKG	unisim	
792	.ARBURST(axi mem intercon 1 M01 AXI ARBURST),			🗝 🌍 ieee.STD_LOGIC_UNSIGNED	STD_LOGIC_UNSIGNED	ieee	
793	.ARCACHE(axi mem intercon 1 M01 AXI ARCACHE),			ieee std. Ionic. misc	istd logic misc	ieee	
794	.ARID({1'b0,1'b0,1'b0,1'b0,axi_mem_intercon_1_M01_AXI_ARID}),			Hierarchy Datasets Classes			
795	.ARLEN({4'b0,axi_mem_intercon_1_M01_AXI_ARLEN}),						
796	.ARLOCK(axi_mem_intercon_1_M01_AXI_ARLOCK),		л	• Objects			
797	.ARPROT(axi_mem_intercon_1_M01_AXI_ARPROT),						
798	.ARREADY(axi_mem_intercon_1_M01_AXI_ARREADY),		-	۹L		-	-
799	.ARSIZE(axi_mem_intercon_1_M01_AXI_ARSIZE),		-	lame			Тур
300	.ARVALID(axi_mem_intercon_1_M01_AXI_ARVALID),	•		ACLK	1		wire
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				Objects Drivers/Readers			



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#### AXI BFM instance in HDL Code

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683	11	.S AXI HPO WID({1'b0,1'b0,1'b0,1'b0,axi mem intercon 1 M01 AXI WID})		🖨 書 design_1	design_1	xil_defaultlib		
684	11	.S AXI HPO WLAST(axi mem intercon 1 M01 AXI WLAST),		🖶 🖶 axi_bram_ctrl_0	design_1_axi_bram_ctrl_0	)⊧ xil_defaultlib		
685	11	.S AXI HPO WREADY(axi mem intercon 1 M01 AXI WREADY),		🖶 🖶 axi_bram_ctrl_0_bram	design_1_axi_bram_ctrl_0	)⊧ xil_defaultlib		
686	11	.S AXI HPO WRISSUECAPI EN(1'b0),		🕀 書 axi cdma 0	design 1 axi cdma 0 0(d	I xil defaultlib		
687	11	.S AXI HPO WSTRB(axi mem intercon 1 M01 AXI WSTRB),		🕀 🔹 axi mem intercon 1	design 1 axi mem interd	⇒xil defaultlib		
688	-11	.S AXI HPO WVALID(axi mem intercon 1 MO1 AXI WVALID));		🖶 🔹 axi protocol converter 0	design 1 axi protocol co	I xil defaultlib		
689	111			🕀 🔹 master 0	Ax Axi3MasterBFM	aldec axi bfm gemu	1	
690		//assign processing system7 0 M AXI GP0 WID = 12'b0;	_	🖶 婁 master 1	Ax Axi3MasterBFM	aldec axi bfm gemu	1	
		Ax Axi3MasterBFM #(		🕀 🖶 slave 0	Ax Axi3SlaveBFM	aldec axi bfm gemu	1	
692	Ĩ.	.DATA BUS WIDTH(32),		- 🙃 @INITIAL#829 0@	-	xil defaultlib		
693		.ADDRESS WIDTH(32),				xil defaultlib		
694	L	.ID WIDTH(12))			glbl	xil defaultlib		
695		naster 0 (		🛛 📲 TIm2BfmPlugin	TIm2BfmPlugin	aldec axi bfm gemu		
696	Ĩ "	.ACLK(processing system7 0 FCLK CLK0),		📲 🚽 DpiPlugin	DpiPlugin	aldec axi bfm gemu		
697		ARESETN(processing_system7_0_FCLK_RESET0 N),		Apackage UnitScopePackage 1\	UnitScopePackage 1	aldec axi bfm gemu		
698		.ARADDR(processing_system7 0 M AXI GP0 ARADDR),		std.standard	standard	std		
699		.ARBURST(processing_system/ 0 M AXI GPO ARBURST),		vl.verilog_logic	verilog logic	vl		
700		.ARCACHE(processing system7 0 M AXI GPO ARCACHE),		std.TEXTIO	TEXTIO	std		
701		.ARID(processing system7 0 M AXI GP0 ARID),		ieee.std logic 1164	std logic 1164	ieee		
702		.ARLEN(processing_system7_0_M_AXI_GPO_ARLEN),		ieee.NUMERIC STD	NUMERIC STD	ieee		
703		.ARLOCK(processing_system/_0_M_AXI_GPO_ARLOK),		axi bram ctrl v4 0 10.axi bram ctrl funcs	axi bram ctrl funcs	axi bram ctrl v4 0	10	
704		.ARPROT(processing_system7 0 M AXI GP0 ARPROT),		ieee.std logic arith	std logic arith	ieee		
705					VCOMPONENTS	unisim		
705		.ARREADY(processing_system7_0_M_AXI_GP0_ARREADY),		ieee.VITAL Timing	VITAL Timing	leee		
		.ARSIZE(processing_system7_0_M_AXI_GP0_ARSIZE),		ieee.VITAL Primitives	VITAL Primitives	ieee		
707		.ARVALID(processing_system7_0_M_AXI_GP0_ARVALID),		unisim.VPKG	VPKG	unisim		
708		.AWADDR(processing_system7_0_M_AXI_GP0_AWADDR),		ieee.STD LOGIC UNSIGNED	STD LOGIC UNSIGNED	ieee		
709		.AWBURST(processing_system7_0_M_AXI_GP0_AWBURST),			std logic misc	ieee		
710		.AWCACHE(processing_system7_0_M_AXI_GP0_AWCACHE),		Hierarchy Datasets Classes	.stri inter trist			
711		.AWID(processing_system7_0_M_AXI_GP0_AWID),		Hierarchy Datasets Classes				
712		.AWLEN(processing_system7_0_M_AXI_GP0_AWLEN),		Provide the second seco				★ €₹
713		.AWLOCK(processing_system7_0_M_AXI_GP0_AWLOCK),		R- colecto				
714		.AWPROT(processing_system7_0_M_AXI_GP0_AWPROT),					▼   ♥ (.*)	Attributes
715		.AWREADY(processing_system7_0_M_AXI_GP0_AWREADY),	-	Name	Va	10	Type	
716		.AWSIZE(processing_system7_0_M_AXI_GP0_AWSIZE),						-
717		.AWVALID(processing_system7_0_M_AXI_GP0_AWVALID),		TI axi_bram_ctrl_0_BRAM_PORTA_ADDR		data	[12:0]wire	
718		.BID(processing_system7_0_M_AXI_GP0_BID),		····ЛГ axi_bram_ctrl_0_BRAM_PORTA_CLK		data	wire	
719		BREADY(processing_system7_0_M_AXI_GP0_BREADY),		🖶 ூரு axi_bram_ctrl_0_BRAM_PORTA_DIN	No	data	[31:0]wire	





DESIGN AND VE

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#### Riviera-PRO QEMU environment

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# KEDNEL SLR cimulation initializ	ation done _ time: 0.0 [c]						start_qe	mu.sh; bash		×	
# KERNEL: SLP simulation initializ # KERNEL: Kernel process initializ # the time for the time of time of time of the time of the time of time of time of time of the time of ti	ation done.				No soundcards fou						-
# Allocation: Simulator allocated # VPI: ALDEC AXI BFM version 1.7.1		22609 kernel=6627 sdT=0)			RAMDISK: gzip image EXT4-fs (ram0): cou	ldn't mount as ext3 due to feat	ture incompatib	oilities			
# KERNEL: ASDB file was created in		iviera-PR0-2017.06-x64/exa	mples/tools/qemu/		EXT4-fs (ram0): war	ming: mounting unchecked fs, ru avice ram0): ext4_update_dynamic	unning e2fsck :	s recommended			
zynq_demo/pl_logic/dataset.asdb					cause of new featur	e flag, running e2fsck is recom	mmended	-			
# VSIM: 176 object(s) traced.					EXT4-fs (ram0): mou	nted filesystem without journal ext4 filesystem) on device 1:0.	1. Opts: (null)				
# VSIM: 0 object(s) traced. # WAVEFORM: 8 object(s) inserted t	o virtual array 'm avi rdata[0	.71.			devtmpfs: mounted						
# WAVEFORM: 8 object(s) inserted t				8	Freeing unused kerr Starting rcS	nel memory: 264K (c06e6000 - c07	728000)				
# WAVEFORM: 8 object(s) inserted t	o virtual array 'm_axi_rdata[10	5:23]'.			++ Mounting filesys	stem					
<pre># WAVEFORM: 8 object(s) inserted t</pre>					mount: mounting /de	ev/mmcblkOp1 on /mnt failed: No ev/mmcblkO on /mnt failed: No su	such file or o	lirectory			
<pre># WAVEFORM: 4 object(s) inserted t # VSIM: 0 object(s) traced.</pre>	o virtual record 'Virtual Reco	rd 1'.			++ Setting up mdev			cector g			
# KERNEL: Block Memory Generator m	odule				++ Starting telnet ++ Starting http da	daemon					
design_1.axi_bram_ctrl_0_bram.inst	.native_mem_mapped_module.blk_m	nem_gen_v8_3_5_inst is usi	ng a behavioral model f	or	++ Starting ftp dae	emon					
simulation which will not precisel	y model memory collision behavi	ior.			++ Starting ssh dae	emon om read with 0 bits of entropy a	available				
				-	rcS Complete						
					zynq> ./dma_test.bi	in <b>-</b>					
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Console Messages											



#### Hardware and Software co-sim

57       #define         58       //#define         69       //#define         61       int main         62       {         63       int and         64       void         65       off_         66       void         67       int and         68       void         69       off_         70       int and         71       int and         72       void         73       unsi         74       off_         75       unsi         76       unsi         77       unsi         78       unsi         79       if (         80       int and         81       if (         82       unsi         84       }         90       /*=         91       57E         93       -	<pre>DDR_MAP_SIZE 0x10000000 DDR_MAP_MASK (DDR_MAP_SIZE - 1) me BUFFER_BYTESIZE 1024 n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; t_dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t_dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t_dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int RegetMask; igned int RegetMask; igneMask; igned int RegetMask;</pre>	<pre>&gt;&gt; X</pre>	er_compile.do T X Untitle Q Q Q Q I 1388 248 568 Hierarchy /design	dl.awc* € X Dp 435 ps ▼ Δ* Δ Δ 1/axi_cdma_0 1/axi_cdma	>         ↑         Auto         1           1 <th>253         ATTRIBUI           254         ATTRIBUI           255         ATTRIBUI           256         ATTRIBUI           257         ATTRIBUI           258         ATTRIBUI           259         ATTRIBUI           259         ATTRIBUI           260         ATTRIBUI           261         ATTRIBUI           262         ATTRIBUI           263         ATTRIBUI           264         ATTRIBUI           265         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           267         ATTRIBUI           268         BEGIN           269         U0 : ax:           270         GENERI           271         C_S.           272         C_S.</th> <th>TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF AXIL LITE ADDR WIDTH =&gt;</th> <th><pre>m_axi_awvali m_axi_awaddr m_axi_awlen: m_axi_awsize m_axi_awsize m_axi_awprot m_axi_awprot m_axi_awready m_axi_wready m_axi_wready m_axi_wready m_axi_wstrb: m_axi_wstrb: m_axi_wlast; m_axi_bvalid</pre></th>	253         ATTRIBUI           254         ATTRIBUI           255         ATTRIBUI           256         ATTRIBUI           257         ATTRIBUI           258         ATTRIBUI           259         ATTRIBUI           259         ATTRIBUI           260         ATTRIBUI           261         ATTRIBUI           262         ATTRIBUI           263         ATTRIBUI           264         ATTRIBUI           265         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           267         ATTRIBUI           268         BEGIN           269         U0 : ax:           270         GENERI           271         C_S.           272         C_S.	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF AXIL LITE ADDR WIDTH =>	<pre>m_axi_awvali m_axi_awaddr m_axi_awlen: m_axi_awsize m_axi_awsize m_axi_awprot m_axi_awprot m_axi_awready m_axi_wready m_axi_wready m_axi_wready m_axi_wstrb: m_axi_wstrb: m_axi_wlast; m_axi_bvalid</pre>
55     #define       57     #define       57     #define       58     //#define       60     int main       62     {       63     int       64     void       66     off_       67     int       70     off_       71     int       72     void       66     off_       71     int       72     void       73     off_       74     void       75     unsi       76     unsi       77     unsi       81<     if (       82     83       84     -       85     unsi       86     unsi       87     unsi       90     if (       92     -       93     -	DDR_MAP_SIZE 0x100000000 DDR_MAP_MASK (DDR_MAP_SIZE - 1) ne BUFFER_BYTESIZE 1024 n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int TimeOut =5; igned int RestMask; igned int RestMask; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &BUFFER_BYTESIZE); (BUFFER_BYTESIZE+1]   BUFFER_BYTESIZE>1024){	// Name - ● (9) - ● (8) - ● (7) - ● (6) - ● (7) - ● (6) - ● (7) - ● (6) - ● (7) - ● (7) - ● (6) - ● (7) - ● ● (7) - ● (7)	Q       Q       Q       1388 248 568         Hierarchy       /design         /design       /design         /dual       /design	435 ps ▼	Image: Non-State	255         ATTRIBUT           256         ATTRIBUT           257         ATTRIBUT           258         ATTRIBUT           259         ATTRIBUT           260         ATTRIBUT           261         ATTRIBUT           262         ATTRIBUT           263         ATTRIBUT           264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           266         ATTRIBUT           266         ATTRIBUT           268         BEGIN           269         U0 : ax:           270         GENERNI           271         C_S.           272         C_S.	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF T_ X_INFO OF T_ X_INTERFACE_INFO OF T_ X_INFO OF	<pre>m_axi_awlen: m_axi_awsize m_axi_awburs m_axi_awprot m_axi_awcach m_axi_wready m_axi_wready m_axi_wradid m_axi_wdata: m_axi_wlast: m_axi_bvalid m_axi_bvalid</pre>
56       #define         57       #define         58       //#define         59       //#define         60       int main         61       int main         62       {         63       int         64       void         65       off         66       int         67       int         68       void         69       off         71       int         72       void         73       off         74       void         75       unsi         76       unsi         77       if (         80       if (         82       83         84       -         88       unsi         88       unsi         90       if (         92       -         93       -	DDR_MAP_SIZE 0x10000000 DDR_MAP_MASK (DDR_MAP_SIZE - 1) ne BUFFER_BYTESIZE 1024 n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdm = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResvEMask; igned int ResvEMask; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &BUFFER_BYTESIZE); (BUFFER_BYTESIZEA=1]   BUFFER_BYTESIZE>1024){	Name         -       ●       ●       ●         -       ●       ●       ●       ●         -       ●       ●       ●       ●       ●         -       ●       <	Hierarchy /design /design /design /design /design /design /design /design /design /design /design /design /design p /design p /design out /design	1/axi_cdma_0 1/	III         >         %         III         Auto         III            1360	256         ATTRIBUI           257         ATTRIBUI           258         ATTRIBUI           259         ATTRIBUI           250         ATTRIBUI           250         ATTRIBUI           260         ATTRIBUI           261         ATTRIBUI           262         ATTRIBUI           263         ATTRIBUI           264         ATTRIBUI           265         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           267         ATTRIBUI           268         BEGIN           269         U0 : ax:           270         E           271         C S.           272         C S.	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF T	<pre>m_axi_awsize m_axi_awburs m_axi_awprot m_axi_awcach m_axi_wready m_axi_wvalid m_axi_wdata: m_axi_wdata: m_axi_wlast: m_axi_brady m_axi_bvalid</pre>
57       #define         58       //#define         69       //#define         61       int main         62       {         63       int and         64       void         65       off_         66       void         67       int and         68       void         69       off_         70       int and         71       int and         72       void         73       unsi         74       off_         75       unsi         76       unsi         77       unsi         78       unsi         79       if (         80       int and         81       if (         82       unsi         84       }         90       /*=         91       57E         93       -	DDR_MAP_MASK (DDR_MAP_SIZE - 1) ne BUFFER_BYTESIZE 1024 n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResvtMask; igned int ResvtMask; igned int ResvtMask; igned int RUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "Md", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE+1]    BUFFER_BYTESIZE>1024){		/design /design /design /design /design /design /design /design /design /design t /design dy /design id /design p /design p	1/axi_cdma 0 1/axi_cdma 0	, µзей,	258         ATTRIBUT           259         ATTRIBUT           260         ATTRIBUT           261         ATTRIBUT           262         ATTRIBUT           263         ATTRIBUT           264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           267         ATTRIBUT           268         BEGIN           269         U0 : ax:           270         E           271         C           272         C	TE X INTERFACE INFO OF TE X_INTERFACE_INFO OF I_cdma IC MAP (	<pre>m_axi_awprot m_axi_awcach m_axi_wready m_axi_wvalid m_axi_wdata: m_axi_wdstb: m_axi_wlast: m_axi_bready m_axi_bvalid</pre>
58       //#defin         60       int main         62       {         63       int         64       void         65       off_         66       off_         67       int         68       void         69       off_         71       int         72       void         73       off_         74       unsi         75       unsi         76       unsi         77       if (         81<	<pre>ne BUFFER_BYTESIZE 1024 n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int RegvAlue; igned int RegvAlue; igned int RegvEnsure; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE+1024){</pre>		/design /design /design /design /design /design /design /design /design /design t /design dy /design id /design p /design p	1/axi_cdma 0 1/axi_cdma 0		259         ATTRIBUT           260         ATTRIBUT           261         ATTRIBUT           262         ATTRIBUT           263         ATTRIBUT           264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           267         ATTRIBUT           268         BEGIN           269         UC ax;           270         GENERI           271         C 5.           272         C 5.	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF I_cdma	<pre>m_axi_awcach m_axi_wready m_axi_wvalid m_axi_wdata: m_axi_wstrb: m_axi_wlast: m_axi_bready m_axi_bvalid</pre>
59       //#defin         60       int main         61       int main         62       [         63       int main         64       void         65       off_         66       int main         67       int main         68       void         69       off_         70       int main         72       void         73       off_         74       unsi         75       unsi         76       unsi         77       unsi         78       unsi         79       if (         81       if (         84       -         86       unsi         90       int         91       57E         93       -	<pre>n(int argc, char* argv[]) memfd; d *mapped_base, *mapped_dev_base; _t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int ResetMask; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE*1024){</pre>	<pre>(7) (6) (6) (7) (7) (7) (7) (7) (7) (7) (7) (7) (7</pre>	/design_ /design_ /design_ /design_ /design_ /design_ /design_ t /design_ t /design_ id /design_ id /design_ jp /design_ _out /design_	1/axi_cdma_0		260         ATTRIBUI           261         ATTRIBUI           262         ATTRIBUI           263         ATTRIBUI           264         ATTRIBUI           265         ATTRIBUI           266         ATTRIBUI           266         ATTRIBUI           267         ATTRIBUI           268         BEGIN           269         U0 : ax:           270         E           271         C S.           272         C S.	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF i_cdma IC MAP (	<pre>m_axi_wready m_axi_wvalid m_axi_wdata: m_axi_wstrb: m_axi_wlast: m_axi_bready m_axi_bvalid</pre>
61     int main       62     □       63             64     void       65     off       66     void       67     int:       68     void       69     off       71     int:       72     void       73     off       74     void       75     unsi       76     unsi       77     unsi       78     unsi       81     □       82	<pre>memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int ResetMask; igned int ResetMask; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE+1]   BUFFER_BYTESIZE&gt;1024){</pre>		/design_ /design_ /design_ /design_ /design_ /design_ bt /design_ dy /design_ id /design_ p /design_ _out /design_	1/axi_cdma_0		262         ATTRIBUT           263         ATTRIBUT           264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           267         ATTRIBUT           268         ■ BEGIN           269         U0 : ax:           270         ■ GENERI           271         C_S           272         C_S	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF i_ccdma IC MAP (	m_axi_wdata: m_axi_wstrb: m_axi_wlast: m_axi_bready m_axi_bvalid
62     □       63     int:       64     void       65     off_       66     off_       67     int:       70     off_       71     int:       72     void       73     off_       74     off_       75     unsi       76     unsi       77     unsi       78     unsi       79     if (       80     ist       81     if (       82     ist       84     }       86     unsi       88     unsi       90     /*=       91     57E       92     -	<pre>memfd; d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int ResetMask; igned int ResetMask; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE+1]   BUFFER_BYTESIZE&gt;1024){</pre>	<pre></pre>	/design_ /design_ /design_ /design_ /design_ /design_ t /design_ id /design_ id /design_ out /design_	1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0 1/axi_dma_0		263         ATTRIBUT           264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           267         ATTRIBUT           268         BEGIN           269         U0: ax:           270         GENERN           271         C_S           272         C_S	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF i_cdma IC MAP (	<pre>m_axi_wstrb: m_axi_wlast: m_axi_bready m_axi_bvalid</pre>
63 int 64 void 66 off_ 66 void 67 int 68 void 69 off_ 71 int 72 void 73 off_ 74 unsi 76 unsi 77 unsi 78 unsi 81 ⊟ if ( 82 83 84 - } 85 84 - } 86 unsi 88 unsi 88 unsi 88 unsi 89 int 90 ⊟ '*== 91 STE 93	<pre>d *mapped_base, *mapped_dev_base; t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d *mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int RegValue; igned int BUFFER_BYTESIZE = 28; (argc = 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE+1]    BUFFER_BYTESIZE&gt;1024){</pre>		/design_ /design_ /design_ /design_ /design_ t /design_ t /design_ id /design_ p /design_ _out /design_	1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0		264         ATTRIBUT           265         ATTRIBUT           266         ATTRIBUT           267         ATTRIBUT           268         BEGIN           269         U0 : ax:           270         GENERI           271         C_S           272         C_S	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF i_cdma IC MAP (	m_axi_wlast m_axi_bready m_axi_bvalid
65     off_       66     67       67     int       68     void       69     off_       70     off_       71     int       72     void       73     off_       74     void       75     unsi       76     unsi       77     unsi       81     if (       83     85       84     -       85     unsi       86     unsi       88     unsi       90     /*==       91     STE       92     -	<pre>_t dev_base_bram = BRAM_BASE_ADDRESS; memfd_1; d "mapped_base_1, *mapped_dev_base_1; t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int ReyFALue; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv11), "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE*1024){</pre>		/design_ /design_ /design_ bt//design_ bt//design_ dy//design_ id//design_ p//design_ out//design_	1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0		266         ATTRIBUT           267         ATTRIBUT           268         ■ BEGIN           269         00 : ax:           270         ■ GENER           271         C_S           272         C_S	TE X_INTERFACE_INFO OF TE X_INTERFACE_INFO OF i_cdma IC MAP (	m_axi_bvalid
66        67     int       68     void       69     off       70     int       71     int       72     void       73     off       74     off       75     unsi       76     unsi       77     unsi       78     unsi       79     if (       81<	<pre>memfd_1; d *mapped_base_1, *mapped_dev_base_1; _t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int RegValue; igned int RegValue; igned int RegValue; igned int RUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE*1]   BUFFER_BYTESIZE&gt;1024){</pre>		/design_ /design_ bb /design_ t /design_ dy /design_ id /design_ p /design_ out /design_	1/axi_cdma_0         1/axi_cdma_0         1/axi_cdma_0         1/axi_cdma_0         F         1/axi_cdma_0         1/axi_cdma_0         1/axi_cdma_0         1/axi_cdma_0		267         ATTRIBUT           268         ■ BEGIN           269         U0 : ax:           270         ■ GENERJ           271         C_S           272         C_S	TE X_INTERFACE_INFO OF i_cdma IC MAP (	
67 int: 68 void 69 off_ 70 void 72 void 73 off_ 74 unsi 75 unsi 77 unsi 80 if ( 81 □ if ( 82 83 84 - } 85 86 unsi 88 unsi 88 unsi 88 unsi 88 unsi 88 unsi 89 j int 90 j /t= 91 STE 92	<pre>d *mapped_base_1, *mapped_dev_base_1; _t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE*1]/ BUFFER_BYTESIZE&gt;1024){</pre>	+ • (1) + • (0) + • • • axi_wstrt + • • • axi_wstrt + • • • axi_breac + • • • • • • • • • • • • • • • • • • •	/design_ /design_ t /design_ dy /design_ id /design_ p /design_ _out /design_	1/axi_cdma_0       1/axi_cdma_0       1/axi_cdma_0       F       1/axi_cdma_0       1/axi_cdma_0       1/axi_cdma_0	)(0	268 BEGIN 269 U0 : ax: 270 ⊡ GENERJ 271 C_S 272 C_S	i_cdma IC MAP (	m_axi_bresp
68     void       69     off_       71     int.       72     void       73     off_       74     off_       75     unsi       76     unsi       77     unsi       78     unsi       79     if (       80     if (       82     83       84     -       86     unsi       88     unsi       89     int       90     jf (       91     STE       92     -	<pre>d *mapped_base_1, *mapped_dev_base_1; _t dev_base_cdma = CDMA_BASE_ADDRESS; memfd_2; d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int BUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE*1]/ BUFFER_BYTESIZE&gt;1024){</pre>		/design_ b /design_ t /design dy /design_ id /design_ p /design_ out /design_	1/axi_cdma_0 1/axi_cdma_0 F 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0	)(e	270	IC MAP (	
70        71     int,       72     void       73     off       74        75     unsi       76     unsi       77     unsi       78     unsi       79     if (       80        81        82        83        84        86     unsi       88     unsi       88     unsi       90        91     STE       92	<pre>memfd_2; d *mapped_base_2, *mapped_dev_base_2; t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int ResetMask; igned int RUFFER_BYTESIZE = 28; (argc == 2); sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE*1    BUFFER_BYTESIZE&gt;1024){</pre>	⊕ • m_axi_wstrt     − • m_axi_wlast     − • m_axi_breac     ↦ m_axi_breac     ⊕ • m_axi_breac     ⊕ • m_axi_totat     ⊕ • m_axi_rdat     ⊕ ⊕ m_axi_rdat     ⊕ ⊕ m_axi_rd	b /design_ t /design_ dy /design_ id /design_ p /design_ _out /design_	1/axi_cdma_0 F 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0	),6	271 C_S 272 C_S		
71     int       72     void       73     void       74     off_       75     unsi       76     unsi       77     unsi       78     unsi       79     if (       80     if (       82     83       84     }       86     unsi       87     unsi       88     unsi       90     /*=       91     57E       92	<pre>d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int RegvAlue; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE*1    BUFFER_BYTESIZE&gt;1024){</pre>	- = m_axi_wlast - = m_axi_breac - = m_axi_breac - = m_axi_breac - = cdma_tvect_ X = = m_axi_rdat - = Cma_tvect_ - = Cma_tvect_ - = m_axi_rdat	t /design_ dy /design_ id /design_ p /design_ _out /design_	1/axi_cdma_0 1/axi_cdma_0 1/axi_cdma_0		272 C_S		• 6
72     void       73     off_       74     off_       75     unsi       76     unsi       77     unsi       78     unsi       78     unsi       81     if (       83     84       84     -       86     unsi       87     unsi       88     unsi       90     int       91     STE       92     -	<pre>d *mapped_base_2, *mapped_dev_base_2; _t dev_base_ddr = DDR_BASE_ADDRESS; igned int TimeOut =5; igned int ResetMask; igned int RegvAlue; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE*1    BUFFER_BYTESIZE&gt;1024){</pre>	<pre>m_axi_bvali m_m_axi_bresp m_axi_bresp m_axi_bresp m_axi_rdata m_m_axi_rdata m_m_virtual Rec m_m_axi_rdata</pre>	id /design_ p /design_ _out /design	1/axi_cdma_0			AXI LITE DATA WIDTH =>	
74 unsi 75 unsi 77 unsi 78 unsi 79 if ( 80 81 □ if ( 82 83 84 - } 85 86 unsi 87 unsi 88 unsi 88 unsi 88 unsi 90 □ /*= 91 STE 93	<pre>igned int TimeOut =5; igned int ResetMask; igned int RegValue; igned int RufFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", GBUFFER_BYTESIZE); (BUFFER_BYTESIZE*1    BUFFER_BYTESIZE&gt;1024){</pre>		p /design_ _out /design_				XI_LITE_IS_ASYNC => 0,	
75         unsi           76         unsi           77         unsi           78         unsi           79         if (           80         if (           81         if (           82         a           84         -           86         unsi           87         unsi           88         unsi           90         int           91         STE           92	<pre>igned int ResetMask; igned int RegValue; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE&lt;1    BUFFER_BYTESIZE&gt;1024){</pre>	<ul> <li>cdma_tvect_</li> <li>m_axi_rdata</li> <li>m_Virtual Rec</li> <li>m_m_axi_rd</li> </ul>	_out /design_				_AXI_ADDR_WIDTH => 32,	
76 unsi 77 unsi 78 unsi 79 if( 80 81 □ if( 81 □ if( 83 84 - } 85 86 unsi 87 unsi 88 unsi 88 unsi 90 □ /*== 91 STE 93	<pre>igned int ResetMask; igned int RegValue; igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE&lt;1    BUFFER_BYTESIZE&gt;1024){</pre>	×  ■ ■ m_axi_rdata P I Virtual Rec ■ I m_m_axi_rd		1/axi_cdma_0			_AXI_DATA_WIDTH => 32, AXI MAX BURST LEN => 1	
78     unsi       79     if (       80     if (       81     if (       82     83       84     -       85     unsi       86     unsi       87     unsi       88     unsi       90     ift       91     STE       92     -	<pre>igned int BUFFER_BYTESIZE = 28; (argc == 2) sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE+1    BUFFER_BYTESIZE&gt;1024){</pre>	E I Virtual Rec ⊕ ■ m_axi_rd		1/axi_cdma_0 000000	0000	277 C_IM	NCLUDE_DRE => 0,	
79 if ( 80 81  ☐ if ( 82 83 84 - } 85 85 86 unsi 87 unsi 88 unsi 88 unsi 90  ☐ /*= 91 \$7E 93	<pre>(argc == 2) sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE-1    BUFFER_BYTESIZE&gt;1024){</pre>	🔲 🕀 🖽 m_axi_rd		1/axi_cdma_0 000000			SE_DATAMOVER_LITE => 0,	
80   81 □ if ( 82   83   84 - } 85   86   unsi 87   unsi 88   int 90 □ /*== 91   STE 93	<pre>sscanf(argv[1], "%d", &amp;BUFFER_BYTESIZE); (BUFFER_BYTESIZE&lt;1    BUFFER_BYTESIZE&gt;1024){</pre>			{0 0 0			EAD_ADDR_PIPE_DEPTH => RITE ADDR PIPE DEPTH =>	
82 83 84 - } 85 unsi 87 unsi 88 unsi 89 int 90 E /*== 91 STE 92 93		🔲 🖽 🖽 maxird		0			NCLUDE_SF => 0,	.,
83 84 - } 85 86 unsi 87 unsi 88 unsi 89 int 90 ⊟ /*== 91 STE 92 93 - ===		E ⊞ m axi rd		θ	2 6 10 14 19 22 26 0		NCLUDE_SG => 0,	
84     -       85     unsi       86     unsi       87     unsi       89     int       90<	<pre>printf("[WARNING] Passed number of bytes are wrong. Supported val BUFFER BYTESIZE=28;</pre>	⊡-⊞ m axi rd		θ	Ver Ver Ver Ver Ver Ver		_AXI_SG_ADDR_WIDTH => AXI_SG_DATA WIDTH => AXI_SG_DATA_WIDTH => AXI_SG_D	
85 unsi 86 unsi 87 unsi 88 unsi 89 int 90 ₽ /*== 91 STE 92 93	BUFFER_BITESIZE=20;	- Default cursor	1 372 ms				LYTMR RESOLUTION => 250	
87         unsi           88         unsi           89         int           90<			1571115				AMILY => "zynq"	
88         unsi           89         int           90         —           91         STE           92         —           93         —	<pre>igned char SrcArray[1024 ]; igned char DestArray[1024 ];</pre>			start	rt_qemu.sh; bash	×		
89         int           90         =         /*==           91         STE           92         93         ===	igned int Index;		yng>./dma_test.bin				i aclk => m axi aclk,	
91 STE 92 93	result=0;	Ē	i] Mapping PL logic BRAM memory.				i_lite_aclk => s_axi_l	
92 93			/dev/mem opened. BRAM memory mapped to user	space.			<pre>i_lite_aresetn =&gt; s_ax introut =&gt; cdma intro</pre>	
93	EP 1 : Initialize the source buffer bytes with a pattern and clea location	.e) []	writing data 28 to BRAM. []] BRAM transfer finished. Memory	unmanned			i lite awready => s a	
94 for			I] Mapping AXI CDMA to user space	anapped:			i_lite_awvalid => s_ax	xi_lite_awva
	<pre>(Index = 0; Index &lt; BUFFER_BYTESIZE; Index++)</pre>	<pre>!/examples/tool:</pre>	/dev/mem opened. reset CDMA.				i_lite_awaddr => s_ax	
95 E {	<pre>SrcArray[Index] = Index;</pre>		enabling interrupt. checking for the Bus Idle.				<pre>i_lite_wready =&gt; s_axx i lite wvalid =&gt; s axx</pre>	
97	DestArray[Index] = 0;		switch mode to simple				i tite wyatiu => 5 ax.	i titte wvati
98 - }			set source addres to BRAM set destination address to	: 81000000. HP SLAVE = 80010000			S 0 ISO-8859-1	▼ Unix INS R
	D. 2 Mar the langel energy leasting starting form 0.20000000 to		wait for DMA transfer stat	IS.				
100 STEP 101	P 2 : Map the kernel memory location starting from 0x20000000 to	Tr	ransfer Completed I] DMA transfer finished and unma	ped from user space.				
102 prin	<pre>ntf("[i] Mapping PL logic BRAM memory.\n");</pre>		<ol> <li>Map kernel memory to user spac /dev/mem opened.</li> </ol>					
103 memf	<pre>fd_1 = open("/dev/mem", 0_RDWR   0_SYNC);</pre>		/dev/mem opened. Memory mapped at address 0	:a6e33000.				
104 <b>if</b> ( 105 ⊟ {	(memfd_1 == -1)	The second se	he data pattern:					
106	<pre>printf("Can't open /dev/mem.\n");</pre>	; using a behavi 0	0123456789101112131415161718192021	22324252627				
107		TH	he data read from HDL:					
108 - }	exit(0);		0123456789101112131415161718192021 DATA Transfer is Successful, 28	22324252627				
109 prin	<pre>exit(0); ntf("\t/dev/mem opened. \n");</pre>							



## **Built-in Transaction Recorder**

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axi slv bfm core.wait on(phase, count); «	Name	Design unit	Library	
ndtask	📋 書 design_1	design_1	xil_defaultlib	
//////////////////////////////////////	🖶 🖶 axi_bram_ctrl_0	design_1_axi_bram_ctrl_0	xil_defaultlib	
endif	🖶 🖶 axi_bram_ctrl_0_bram	design_1_axi_bram_ctrl_0	xil_defaultlib	
	🖶 🖶 axi_cdma_0	design_1_axi_cdma_0_0(d	xil_defaultlib	
	🖶 🖶 axi_mem_intercon_1	design_1_axi_mem_interc⊧	xil_defaultlib	
fdef ALDEC USE TRANSACTIONS	🖶 🖶 axi_protocol_converter_0	design_1_axi_protocol_co⊭	xil_defaultlib	
	🖶 ≢ master_0	Ax_Axi3MasterBFM	aldec_axi_bfm_qemu	
TransactionRecorderAxi3 #(	🕀 ≢ master_1	Ax Axi3MasterBFM	aldec_axi_bfm_qemu	
.DATA BUS WIDTH(DATA BUS WIDTH),	🗇 ≢ slave_0	Ax Axi3SlaveBFM	aldec axi bfm qemu	
.ADDRESS WIDTH(ADDRESS WIDTH),	- 📽 axi slv bfm core	Ax Axi3SlaveBFMcore	aldec axi bfm qemu	
.ID WIDTH(ID WIDTH),	🕀 婁 TransRecorder	TransactionRecorderAxi3	aldec axi bfm gemu	
.INSTANCE(\$sformatf("%m")))	🔤 🔂 @INITIAL#ini@		aldec axi bfm gemu	
TransRecorder (	🗘 @INITIAL#829 0@		xil defaultlib	
.ACLK(ACLK),	@INITIAL#841 1@		xil defaultlib	
.ARESETn (ARESETn),	🖶 🖶 glbl	glbl	xil defaultlib	
.AWID(AWID),		TIm2BfmPlugin	aldec axi bfm gemu	
AWADDR (AWADDR),	🚽 🐨 🐨 DpiPlugin	DpiPlugin	aldec axi bfm qemu	
.AWLEN(AWLEN),	\package UnitScopePackage 1\	UnitScopePackage 1	aldec axi bfm gemu	
. AWSIZE (AWSIZE),	std.standard	standard	std	
.AWBURST (AWBURST),	vI.verilog logic	verilog logic	vl	
.AWLOCK (AWLOCK),	std.TEXTIO		std	
. AWCACHE (AWCACHE),	ieee.std logic 1164	std logic 1164	ieee	
. AWPROT (AWPROT),	ieee.NUMERIC STD	NUMERIC STD	leee	
.AWVALID(AWVALID),	axi_bram_ctrl_v4_0_10.axi_bram_ctrl_funcs		axi bram ctrl v4 0 10	
. AWREADY (AWREADY),	ieee.std logic arith	std_logic_arith	leee	
.WID(WID),	unisim.VCOMPONENTS	VCOMPONENTS	unisim	
.WDATA(WDATA),	ieee.VITAL Timing	VITAL Timing	leee	
.WSTRB(WSTRB),	ieee VITAI Primitives	VITAI Primitives	ieee	
.WLAST(WLAST),	Hierarchy Datasets Classes			
.WVALID(WVALID),				
WREADY (WREADY),	🎦 Objects			ج 🗢 🛧
.BID(BID).				👻 🌳 (.*) Attributes
BRESP(BRESP),				• • • • Attributes
.BVALID(BVALID),	Name	Valu	е Тур	e
BREADY (BREADY).	ACLK	1	wire	2
.ARID(ARID),	ARESETN	1	wire	
	AWID	z?0	[ID	WIDTH-1:0]wire
• ANADON ( ANADON ) ,		:	: -	· - :

#### Transaction based debug

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										have	1240	hana
me ∍ m axi awsize	Hierarchy All /design 1/axi cdma 0	A	0	1330	1338	1340	1342		1344	1346	1348	1350
m_axi_awsize	/design_1/axi_cdma_0	0	0									
m_uxi_uwburst m_axi_awprot		0	0									
m_axi_awcache	/design 1/axi cdma 0	3	3									
▶ m axi wready	/design_1/axi_cdma_0	1				•			•		•	
🛥 m axi wvalid	/design 1/axi cdma 0	1										
🛥 m axi wdata	/design 1/axi cdma 0	OFOEODOC	03020100	-	07060504	080A0908	ØFØEØDØC		13121110	17161514	1B1A1918	0000000
a m_axi_wstrb	/design_1/axi_cdma_0	F	F									0
🛥 m_axi_wlast	/design_1/axi_cdma_0	0										
m_axi_bready	/design_1/axi_cdma_0	1										
▶ m_axi_bvalid	/design_1/axi_cdma_0	0										
▶ m_axi_bresp	/design_1/axi_cdma_0	0	0									
cdma_tvect_out		0000000	00000000									
▶ m_axi_rdata	/design_1/axi_cdma_0			07060504	080A0908	(0F0E0D0C	13121116		17161514	181A1918	000000	
B Virtual Record 1		{16 17 18 19}	{0 1 2 3}	(4 5 6 7)	(8 9 10 11)	(12 13 14 15)	({16 17 1	B 19}	{20 21 22 23}	{24 25 26 27}	(000)	
			🗧 🗸 Count	(2) 🗸 Relations 🗸	Auto height							
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Sender WDATA		0706050403020100						50403020100		0f0e0d0c0b0a0908		relations o.
Sender WSTRB		ff					ff			ff		
Sender WLAST		0	1				0			0		
Sender WVALID Sender WREADY		1					1			1		
Signal		Value					Value			Value		
relations in( 0	)	vacue						ns in( 0 )		relations in( 0 )		
relations out( @								ns out( 0 )		relations out( 0 )		
									Sender name : design_1			
			2						Sender WID : zZ0	-		
									Sender WDATA : 07060 Sender WSTRB : ff	50403020100		
			Count	(1) V Relations V	Auto beight				Sender WLAST : 0			
			V Count		Rato height				Sender WVALID : 1			
R_Stream	/design_1/master_0/Træ							R_Stream	Sender WREADY : 1 Signal : Value			
									Stream: sim:/design_1/s	slave_0/TransRecorder/W_Strea	m	
									Substream: 1 Begin time: 1342ms			
									End time: 1344ms			
			1						1			
									1			
									Value			
									relations in( 0 ) relations out( 0 )			
									relations out( 0 )			
			🗧 🗸 Count	(1) 🗸 Relations 🖌	Auto height							
AR Stream	/design_1/master_0/Træ							AR Stream				
-											🖃 design 1.master θ	
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											7e200004	
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Default cursor 1	342 650 us	:					1 342	550 us			2	1
			▶ ◀ 133502	29333013ps - 1351110	0666987ps							•••



NCE AND EXHIBITION

#### **Transaction** logs

me	Hierarchy All 🌲	Value	200	(1) (2) (3) (4)	(5) (6) (7) (8) (9) (10) (11) (12) (13)	(14) (15) (16) (17) (18) (19)	20) (21) (22) (23) (1)	(2) (3) (4) (5) (6)	(1) (2) (3) (4) (5) (6)	(7) (8) (9) (10) (11) (12)	(13) (14) (15) (16) (17) (18)	(19) (20) (21) (22) (23) (24) (25)	) (26) (1)
			🗧 🗸 Co	unt (1) 🖌 Rel	ations 🖌 Auto height								
W Stream	/design 1/master 1/Træ							W	Stream				
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								lue	- Value				Va
							rela	ations in( 0 )	relations in( $\theta$ )				rel
							rela	ations out( θ…	relations out( 0 )				rel
			Co	unt 🗌 Relatio	ns 🗸 Auto height								
W_Stream	/design_1/master_0/Træ							W_	Stream				
Sender name		design_1.master_0	¢.	🗆 design_1.m	aster_0								
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Sender WDATA Sender WSTRB		00007000 f		00007000 f									
Sender WLAST		1		1									
Sender WVALID		1		1									
Sender WREADY		1		1									
Signal		Value	_	Value									
					si	m:/design_1/maste	er_0/TransRecord	er/W_Stream			×		
		-	<u>F</u> ile <u>E</u> dit								<b>Z</b>		
			Begin Time		•	- 😤 (.*) 🕓	D 🕅 🔁						
			Begin Time	End Time	Sender name Sender WID		Sender WSTRB	Sender WLAST	Sender WVALID	Sender WREADY	Signal		
			198ms	200ms	design_1.master_0 000	0000004	f	1	1	1	Value		
			284ms	286ms	design_1.master_0 000	00007000	f	1	1	1	Value		
			926ms 972ms	928ms 974ms	design_1.master_0 000 design 1.master 0 000	00000004 00000004	f f	1	1	1	Value Value		
			1018ms	1020ms	design_1.master_0_000	00000004	f	1	1	1	Value		
			1064ms	1066ms	design 1.master 0 000	00000004	f	1	1	1	Value		
			1110ms	1112ms	design_1.master_0 000	00000004	f	1	1	1	Value		
			1176ms	1178ms	design_1.master_0 000	00007000	f	1	1	1	Value		
			1242ms	1244ms	design_1.master_0 000	81000000	f	1	1	1	Value		
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		=				0000010		-	-	-	Vulue		
		L	T Snows se	elected transac	ations in waveform								
Default cursor	284 ms + 11				284 ms + 11								



<u>File</u> Edit Waveform



# Summary

- SoC FPGA Verification Platform
- Processor modeling based on QEMU emulator (instead of simplified BFM model)
- Hardware and Software debugging
- Fast RTL IP Core Verification and bugs fixing
- Driver and Firmware Verification
- Built-in Transaction Recorder
- Support for many platforms and processors
- Support for different Linux versions
  - Yocto project





## **QEMU co-emulation with HES-DVM**

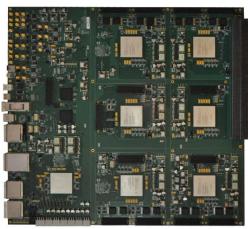


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# **Emulation Pros & Cons**

- (+) Fast 10+ MHz speed
- (+) Cycle Accurate hardware model
- (+) Advanced Hardware Debugging
- (+) Enables testing with real devices/live data
- (-) Emulation available later than RTL Simulation
- (-) Usually limited emulation resources



**HES** Hardware Emulation Solutions



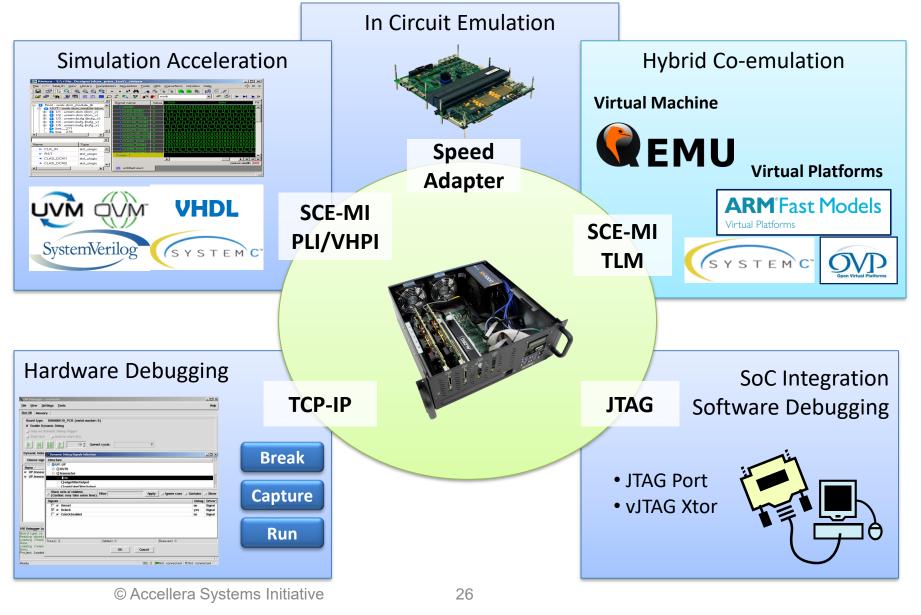




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# HES-DVM<sup>™</sup> Versatile Emulation Platform



accellera

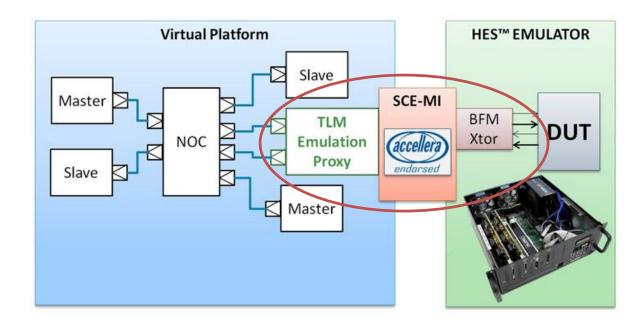
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# **Connecting Virtual Platforms**

#### SoC Bus Transactors (BFM with SCE-MI)

- AMBA Advanced Microcontroller Bus Architecture
  - AXI Master & Slave
  - AHB Master & Slave
  - APB Master & Slave
- OCP Open Core Protocol
  - Master & Slave



#### Virtual Platform Plug & Play

- HES PCIe host driver (Linux/Windows)
- SystemC/TLM Proxy for each bus transactor
- SCE-MI Accellera Standard Co-Emulation Modeling Interface





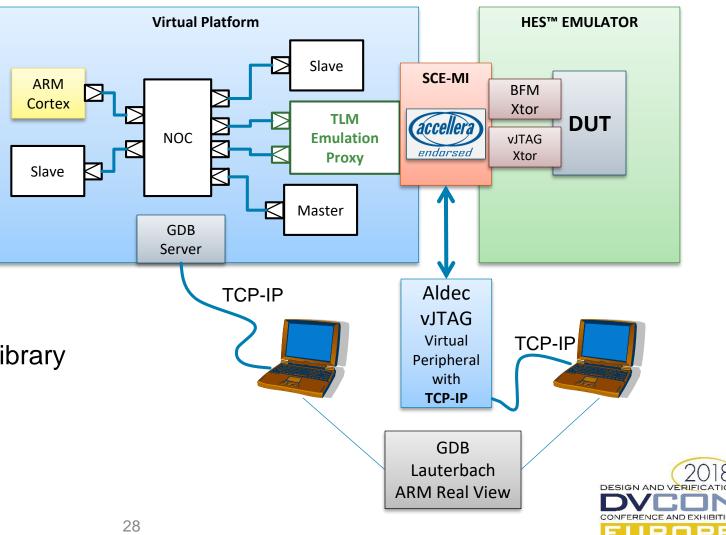
# Software debugging



- In Virtual Platform
  - VP provides interface

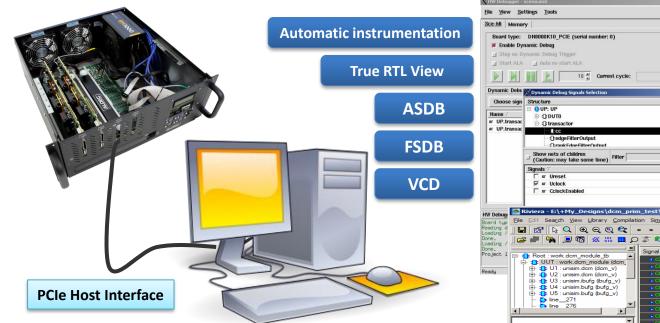
#### In HES Emulator

- Aldec provides solution:
  - vJTAG Transactor
  - vJTAG Virtual Peripheral library with TCP-IP





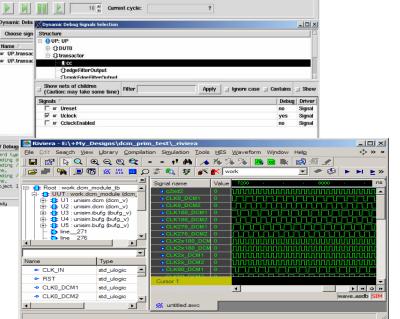
# Hardware debugging



- Debug probes 100% visibility
- Breakpoints and Triggers
- Clock control
- True RTL debugging
- Memory visibility



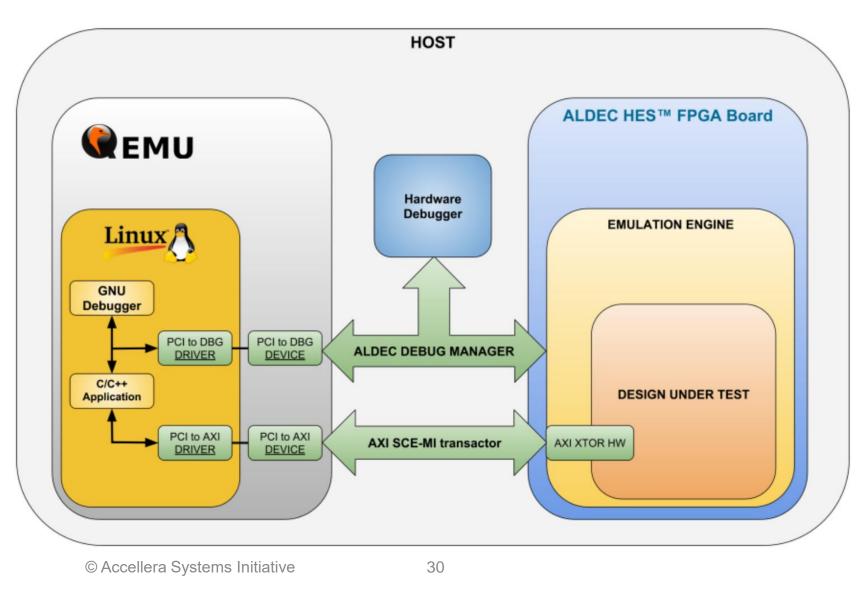




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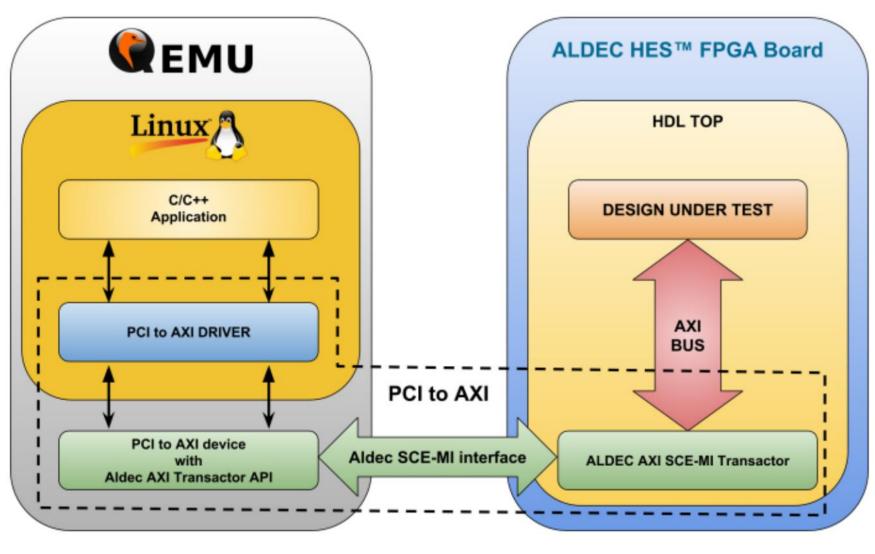
## **QEMU Co-Emulation**







## QEMU PCI to AXI bridge







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# **QEMU Co-Emulation Highlights**

- Synchronized Hardware/Software Debug
  - Force Break stop hardware clocks on software breakpoint
  - Software debugger integration (GDB), custom commands
- AMBA AXI interface support
  - Aldec AXI Master transactor VIP
- PCI to AXI Bridge
- QEMU virtual machine architectures with PCI device tree (ARM, x86 and others)
- Integrated with Linux Guest OS in QEMU
- Automated design compilation in HES-DVM platform



#### QEMU Co-Emulation Live Demo

QEMU	_ 🗆 🗙 krzysieks@k17:~/home/QEMU-ix86/qemu_sudoku_v1_0/emu/run
View	View Search Terminal Help
idoku Solver	t₊ Pl +0) 14:02 🌣 ks@k17 run]\$ hesls
<pre>     delta d</pre>	Image: Support in the set of the se
[New Thread 0x7fffe0ff6700 (LWP 1679)] [New Thread 0x7fffdbfff700 (LWP 1680)]	
[New Thread 0x7fffdb7fe700 (LWP 1682)]	krzysieks@k17:~/home/QEMU-ix86/qemu_sudoku_v1_0/emu
[New Thread 0x7fffdaffd700 (LWP 1683)] [Thread 0x7fffdaffd700 (LWP 1683) exited]	File Edit View Search Terminal Help
[Thread 0x7fffdb7fe700 (LWP 1682) exited]	<pre>qemu-system-x86_64: info: [ALDEC XTOR INF0] clock mode changed to 2</pre>
[New Thread 0x7fffdb7fe700 (LWP 1687)] [Thread 0x7fffdb7fe700 (LWP 1687) exited]	<dbg> RUN</dbg>
	<dbg> STOP</dbg>
Thread 1 "sudoku_solver" hit Breakpoint 1, MainWindow::on_btnSolve_clicked (this=0x7fffffffda10) at/ma dow.con:90	
dow.cpp:90 (gdb)	<dbg> DISCONNECT</dbg>
📗 [ [VNC config] 🛛 🛛 📓 krzysieks@k17:~/hom 🛛 📓 krzysieks@k17:~/hom 🛛 📅 [HW Debugger] 👘 🕄 [R	viera-PRO - /home/    🙀 QEMU



## Questions



