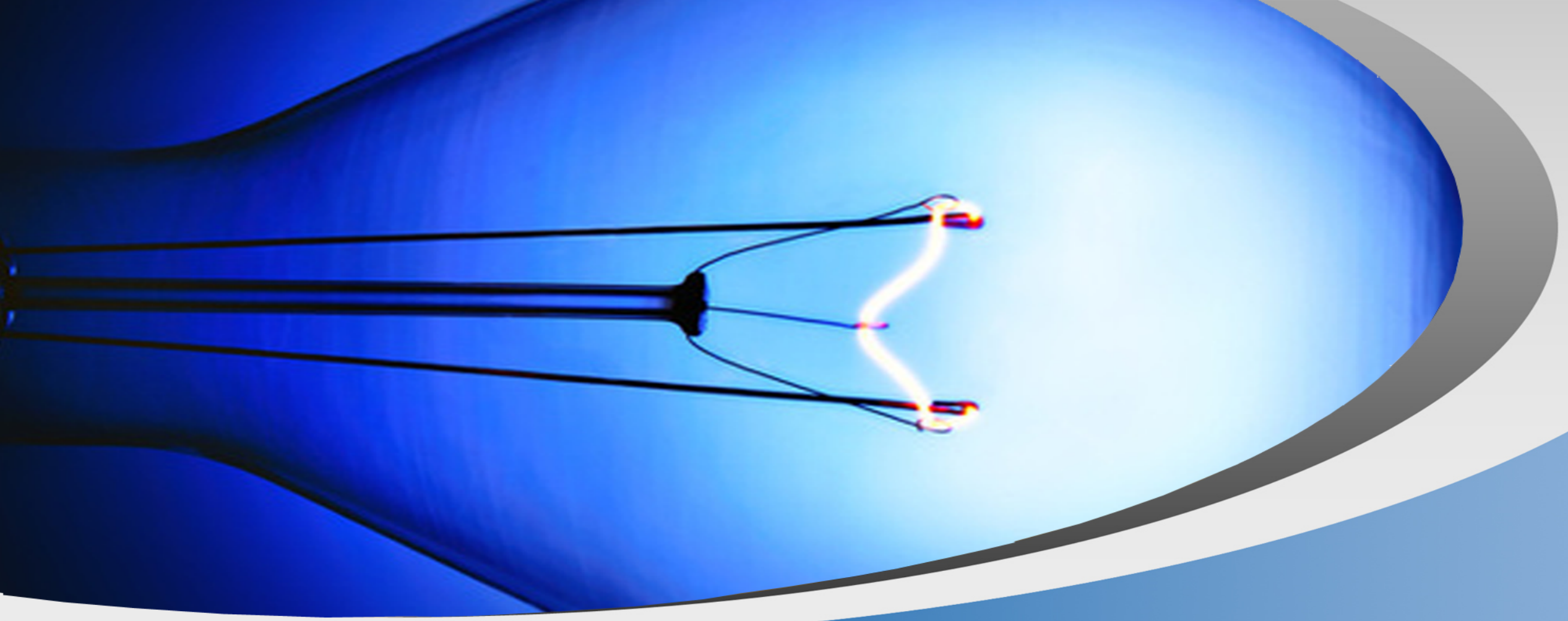

Accellera Overview

July 2024

Lu Dai | Accellera Chair

accellera

SYSTEMS INITIATIVE

Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global Electronic Design Automation and IP standards that improve design and verification productivity for today's advanced integrated circuits and embedded systems. In addition, we strive to promote the widespread adoption of these standards.

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Broad Industry Support

Corporate Members

AMD, arm, cadence, Ericsson, Ford, intel, NXP, Qualcomm, Siemens, ST, Synopsys

Start-Up and University

Sciences Sorbonne Université, Kärnten University of Applied Sciences, MachineWare, 合见工软 UNIVISTA

Associate Members

Advantest, Agnisys, Aldec, AMIQ, Analog Devices, Apple, Arteris IP, ausdia, Blue Pearl Software, Bosch Invented for life, Breker, Coseda Technologies, Doulos, Fraunhofer IIS, Huawei, Infineon, Marvell, Microchip, Microsoft, NVIDIA, Renesas, S2C EDA Solutions, scientific analog, Vayavya Labs Pvt. Ltd., Verific, verilab, Western Digital

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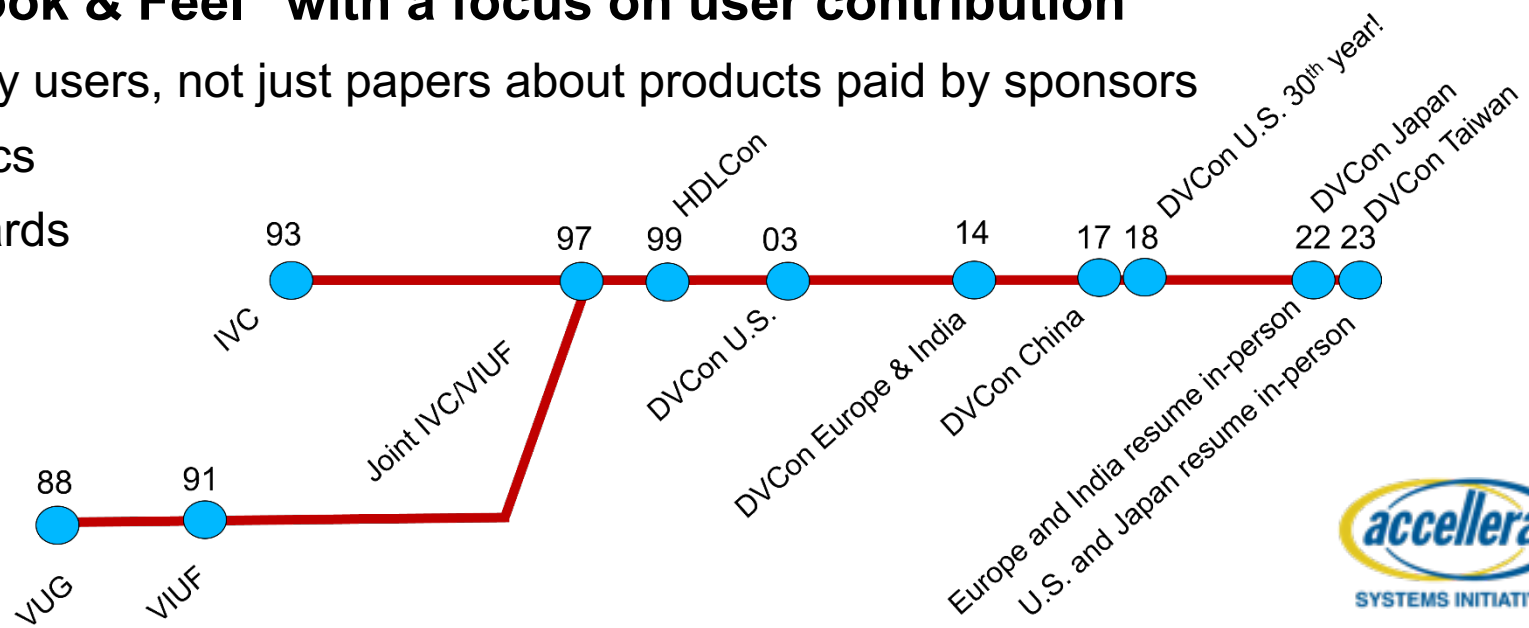
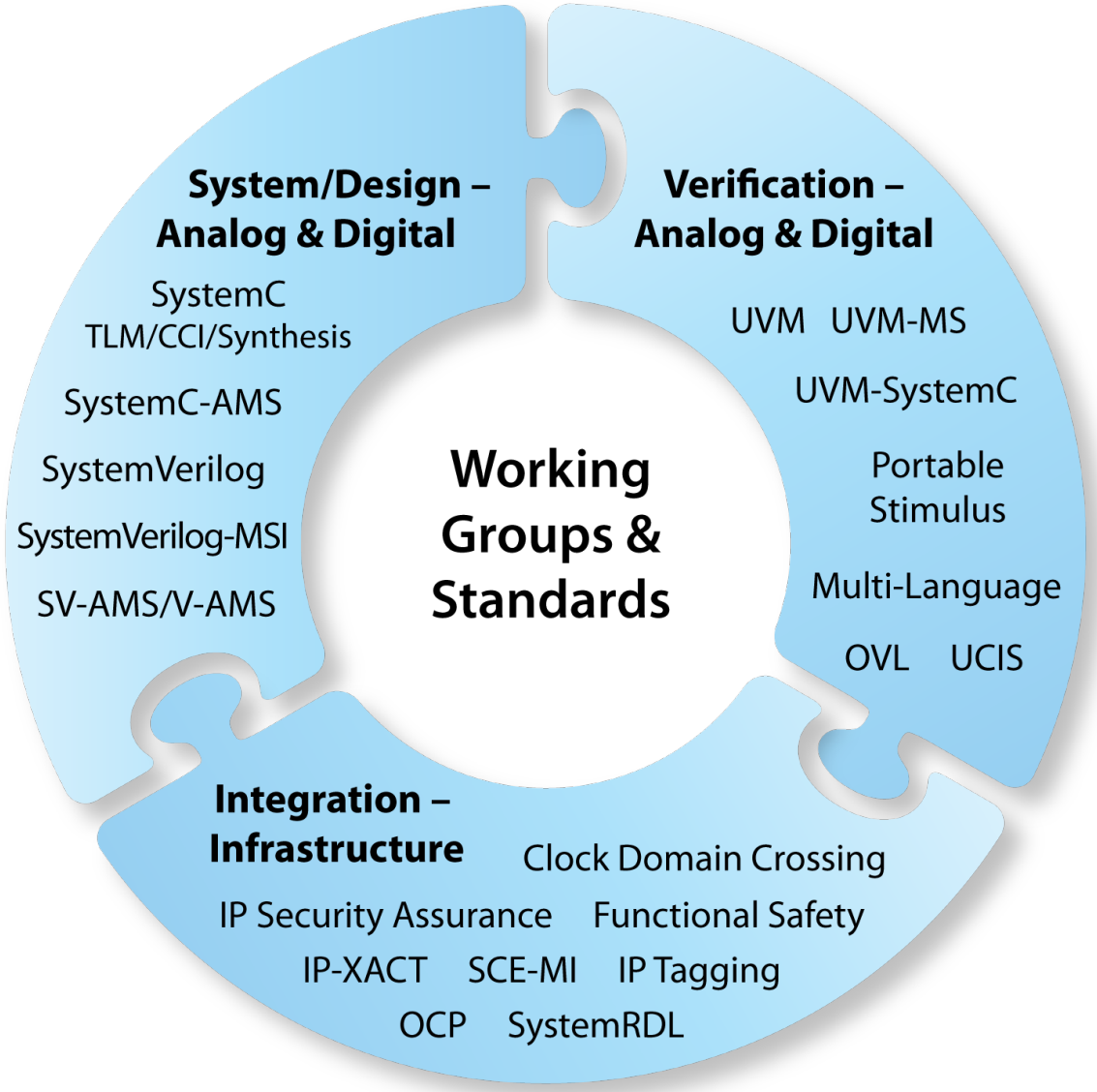
Accellera and DVCon

- **Accellera has been successfully sponsoring Design & Verification Conference & Exhibition in the US for over 35 years**
  - Original events had different names and were tied to VHDL International and Open Verilog International
  - Eventually VHDL and Verilog-focused groups merged into a single conference and became DVCon in 2003
- **Global expansion started in 2014**
  - DVCon Europe, DVCon India, DVCon China, DVCon Japan, and DVCon Taiwan
- **Every DVCon has a similar "Look & Feel" with a focus on user contribution**
  - Papers written by and presented by users, not just papers about products paid by sponsors
  - Panel sessions on current hot topics
  - Tutorials related to relevant standards



The Accellera Ecosystem



Helping you bring all the pieces together

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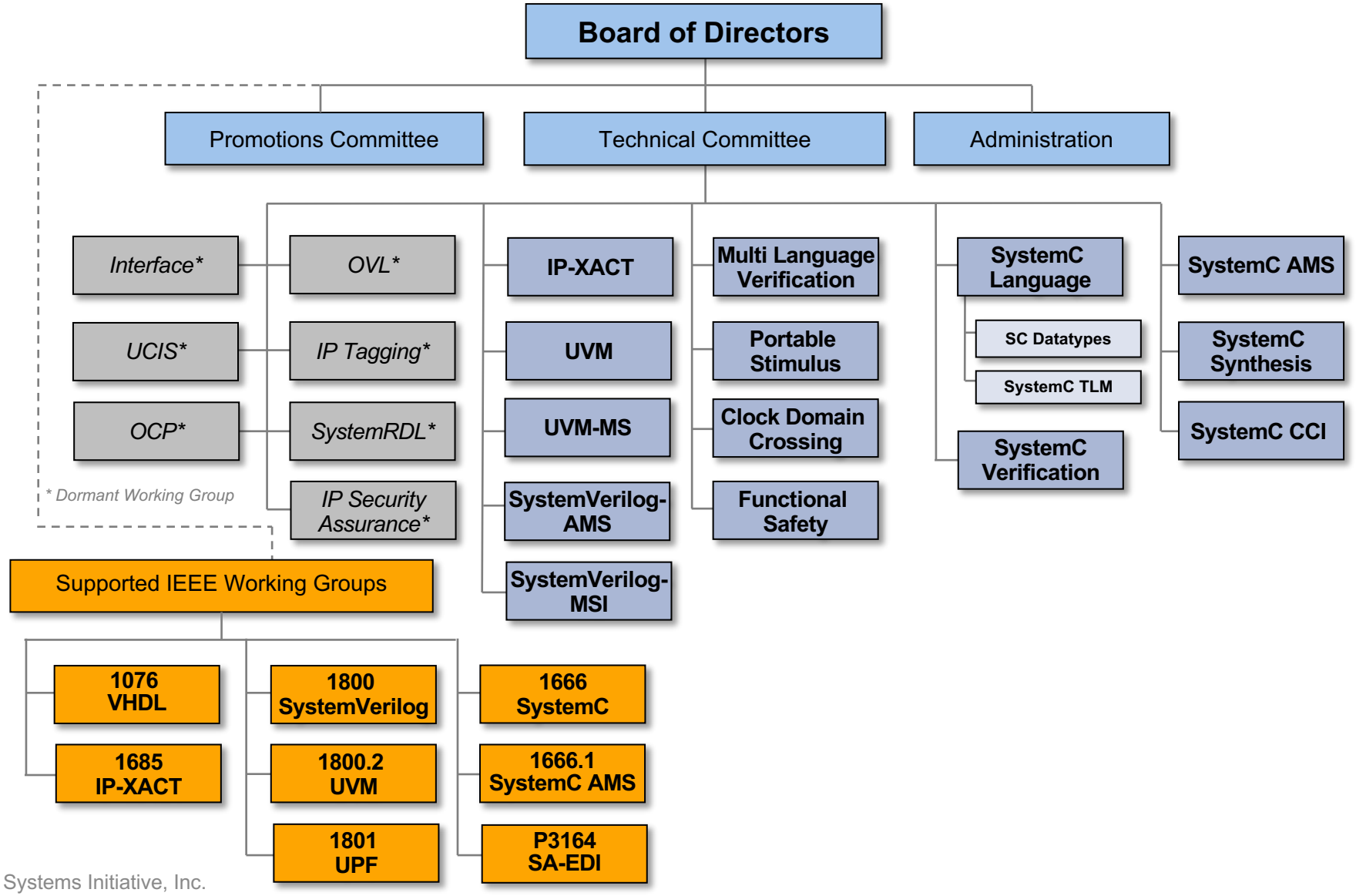
Accellera Systems Initiative



Accellera Standards and Activities

Current Standards and Supplemental material

Standards

- Intellectual Property (IP) Tagging 1.0
- IP-XACT - Update of IEEE P1685 and Vendor Extensions
- Multi-Language (ongoing)
- Open Verification Library (OVL) 2.8.1
- Portable Stimulus 2.1
- Security Annotation for Electronic Design Integration 1.0
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- SystemVerilog-AMS & SystemVerilog-MSI (ongoing)
- SystemRDL 2.0
- SystemC Analog Mixed-Signal (AMS) 2.3
- SystemC Configuration, Control & Inspection (CCI) 1.0
- SystemC Core Language 2.3.3 (includes TLM 2.0)
- SystemC Synthesis 1.4.7
- Unified Coverage Interoperability Standard (UCIS) 1.0
- Universal Verification Methodology 2020-1.1
- Verilog-AMS 2023

Supplemental material

- IP-XACT Users Guide
- SystemC AMS Users Guide and Application Examples
- SystemC CCI 1.0 Proof-of-Concept Kit
- SystemC Reference Implementation and Regression Test Suite 3.0
- SystemC Core Language and Examples
- SystemC Verification Library (SCV) 2.0.1
- UVM 2020.3.0 Reference Implementation
- UVM-SystemC Library 1.0-beta4

Whitepapers

- IP Security Assurance
- Functional Safety

IEEE Standards Access at No Charge

- **Accellera relationship with the IEEE-SA**
- **Accellera will release 10 standards for 10 years under an extended IEEE Get program**
- **More than 187,000 downloads to date!**

IEEE GET EDA Standards

Download IEEE Standards
http://ieeexplore.ieee.org/Xplore/home.jsp
- or find links to specific standards at -
www.accellera.org/downloads/ieee

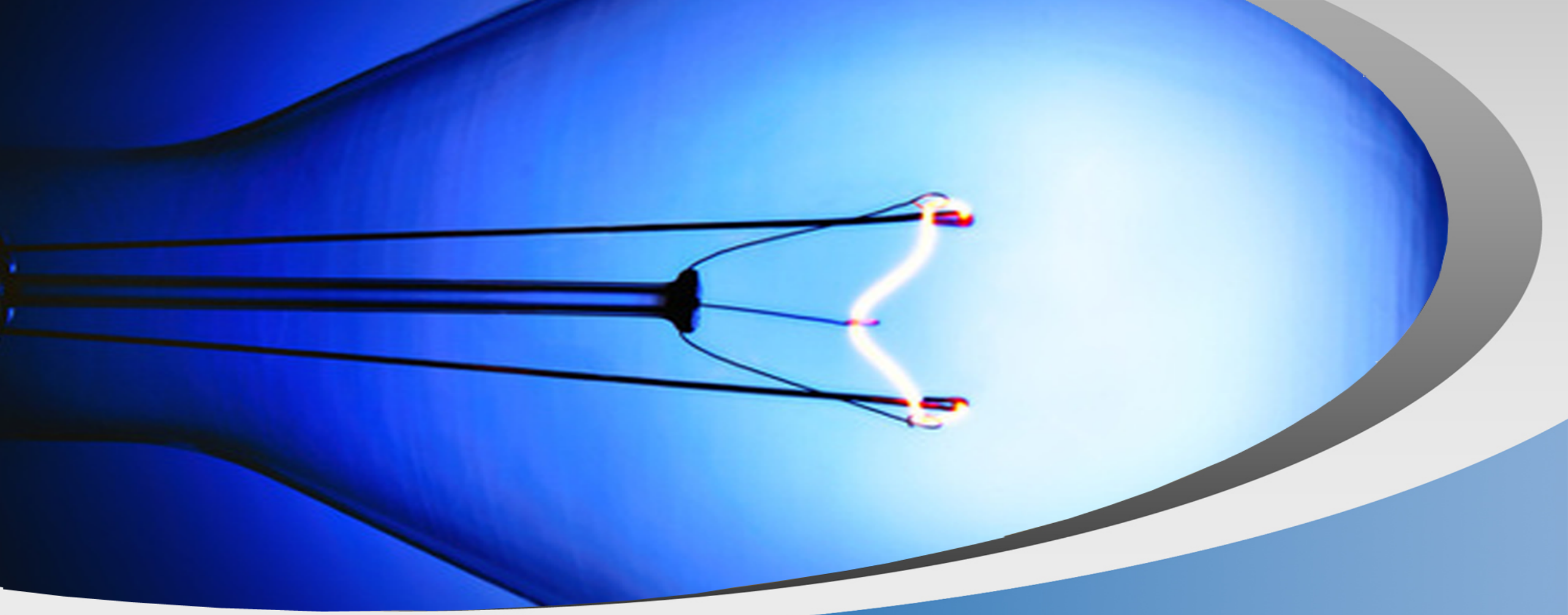
Recent Accellera News

- **Federated Simulation Standard Working Group Formed –** June 2024
- **Verilog-AMS 2023 Standard –** March 4, 2024
- **IEEE 1800™-2023 Availability in GET Program –** March 4, 2024
- **Distinguished Service Award - Shalom Bresticker –** February 26, 2024
- **SystemC 3.0.0 Fully Compatible with IEEE 1666™-2023 –** February 5, 2024
- **SystemVerilog Mixed-Signal Interface (MSI) Working Group –** February 7, 2024

Looking Forward

- **Portable Stimulus Working Group**
  - Portable Stimulus Standard 3.0 in public review through July 5
- **Clock Domain Crossing Working Group**
  - Team on fast track to develop standard
- **SystemC Synthesis Working Group Restarted**
  - New Chair - Frederic Doucet, Qualcomm
- **Functional Safety Working Group**
  - LRM to be released later this year
- **SystemVerilog Mixed-Signal Interface (MSI) Working Group**
  - Recently approved as formal working group
  - Planning to release standard this year

Accellera Global Sponsors
Thank you!



Accellera Technical Committee Update

August 2024

Martin Barnasconi | Accellera Technical Committee Chair

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Technical Committee Update

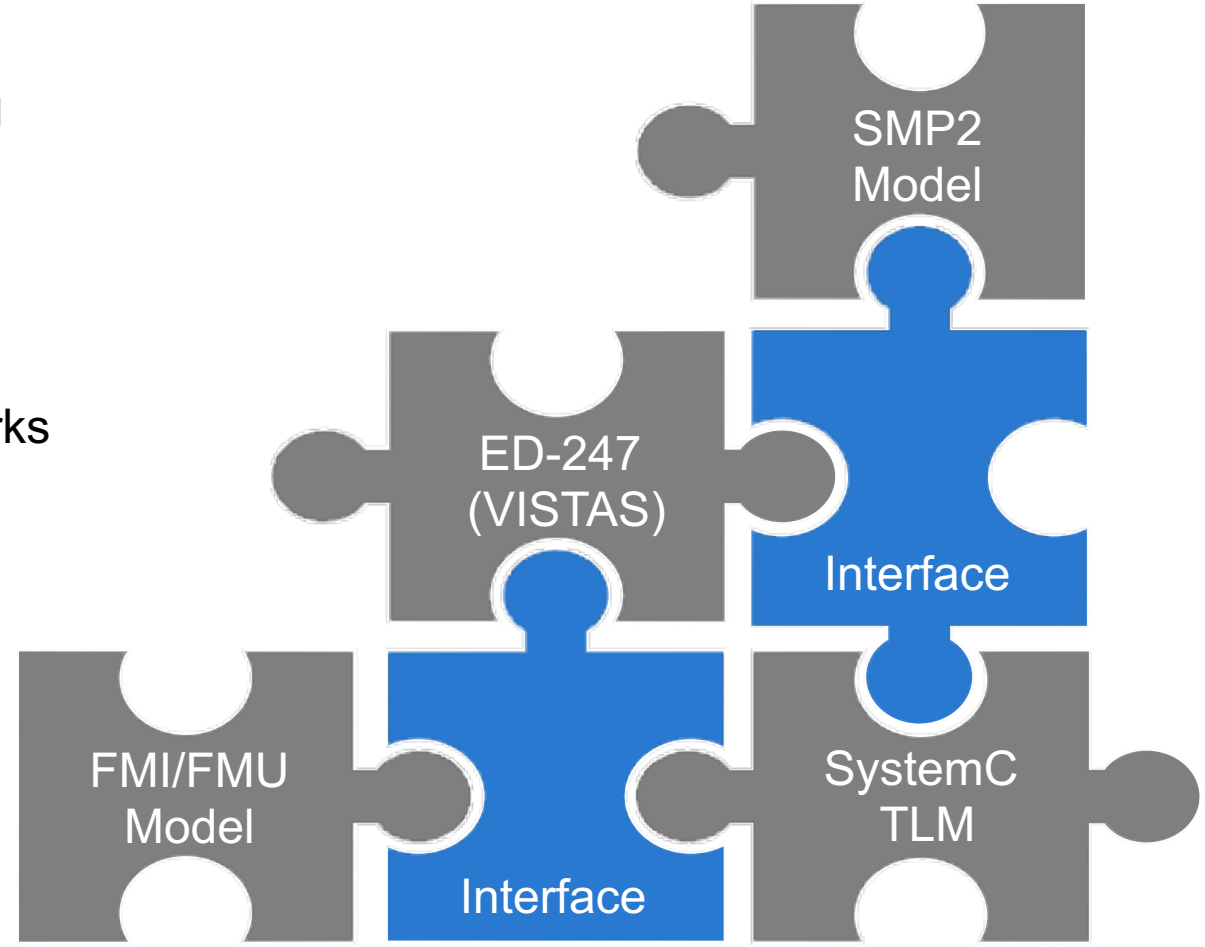
- **Federated Simulation Standard (FSS)**
- **Universal Verification Methodology (UVM)**
- **Universal Verification Methodology for Mixed-Signal (UVM-MS)**
- **SystemC standards and eco-system**

Federated Simulation Standard (FSS)

- **Accellera FSS Working Group formation approved in July, meeting series start in September**
- **Charter**
  - Cross-industry alignment and collaboration to improve the interoperability of product and environment simulation using existing and new open standards
- **Scope and objectives**
  - Develop a standard (meta-model and API) and open infrastructure to enable interoperability of established modeling and simulation standards, technologies and tools as part of a distributed, orchestrated and federated simulation ecosystem
- **Main Deliverables**
  - Standard definition (Language Reference Manual)
  - Supplemental material enabling standard deployment (e.g. reference implementation, examples, etc.)
- **In addition to the Working Group standardization, an industry-open User Group is formed**
  - Enabling open innovation and co-development with other organizations and consortia

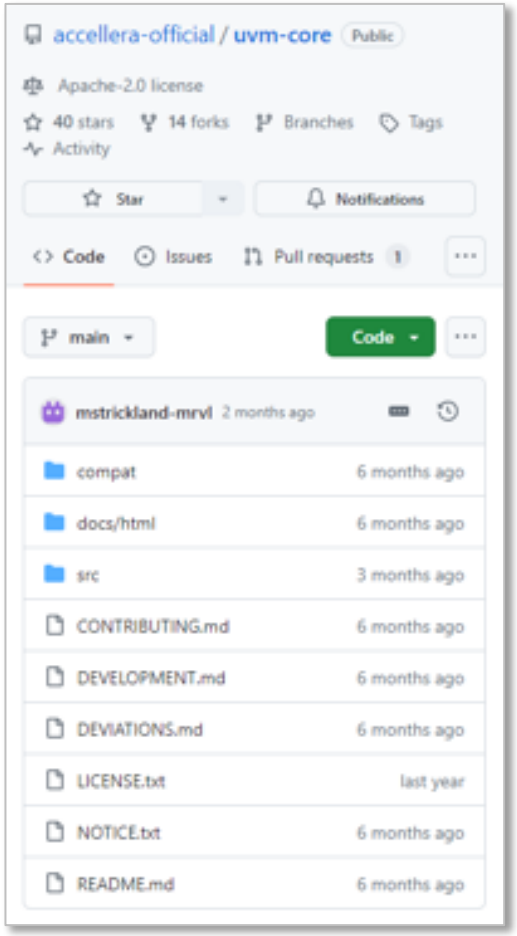
FSS: Cross-industry collaboration enabling interoperability of simulation frameworks

- **Approach: Leveraging and connecting existing standards and industry formats**
  - Not re-invent wheels
- **Introduce standardized interfaces**
  - Enabling interoperability between simulation frameworks
- **Targeting a scalable simulation and modeling ecosystem**
  - Support models and simulation domains used at different levels of the ‘OSI stack’
  - Ecosystem of simulators, models, and other components that together form Systems-of-Systems



Universal Verification Methodology (UVM)

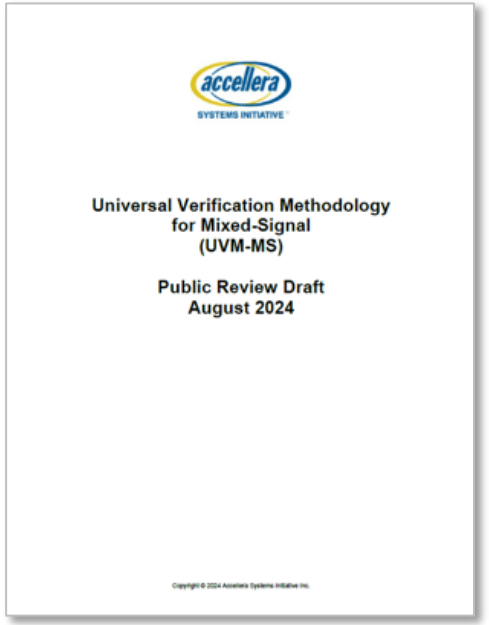
- **UVM 2020-3.0 Reference Implementation released at DVCon US 2024 earlier this year**
  - UVM SystemVerilog library matching the requirements of IEEE 1800.2-2020
  - Enhancements: RTL signal polling and callback mechanism for killed processes
  - Address compatibility issues and resolve bug fixes
- **Library and release also available at Public GitHub Repository**
- **Ongoing developments**
  - Development of an extension mechanism to support UVM Mixed Signal (UVM-MS)
  - Reviewing an enhancement proposal for the heartbeat feature



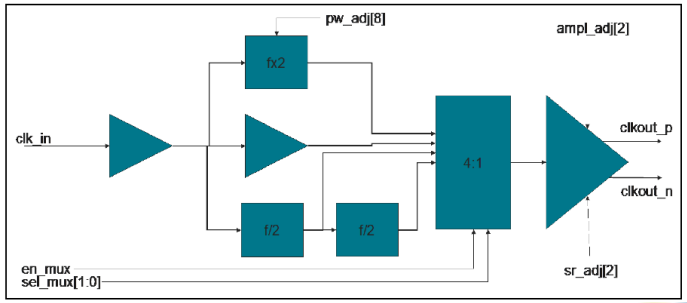
UVM at GitHub

UVM Mixed Signal (UVM-MS)

- **Accellera released the UVM-MS Draft Standard in August 2024**
  - Unified analog/mixed-signal verification methodology based on UVM (IEEE Std 1800.2)
  - Improves analog/mixed-signal (AMS) and digital/mixed-signal (DMS) verification of integrated circuits and systems
  - Public review open through September 9, 2024
- **UVM-MS test case**
  - Example: Frequency Adapter
  - Demonstrates how to migrate from UVM to UVM-MS
- **Draft standard and test case are available for download at Accellera**
  https://accellera.org/downloads/drafts-review



UVM-MS Draft Standard



Frequency Adapter Example

SystemC standards and eco-system

- **SystemC 3.0.0 reference implementation released in March 2024**
  - Fully compliant with latest SystemC standard IEEE Std 1666-2023
  - Available via Accellera public repository on GitHub
  - Latest development available in the `develop` branch

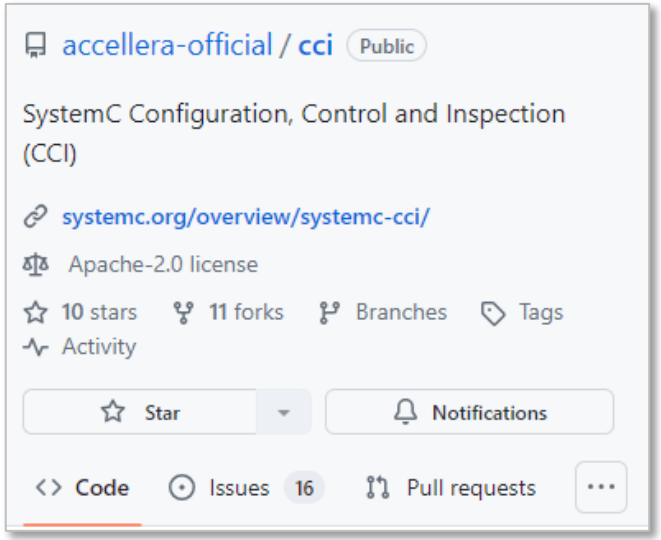
- **SystemC Synthesis Working Group restarted**
  - New leadership: Chair Frederic Doucet (Qualcomm), Vice-chair Rauf Salimi Khaligh (Apple)
  - WG plans and developments presented at SystemC Fika in May
  - **Call for Participation**: https://vimeo.com/929513471

Synthesis Working Group Call for Participation

SystemC standards and eco-system

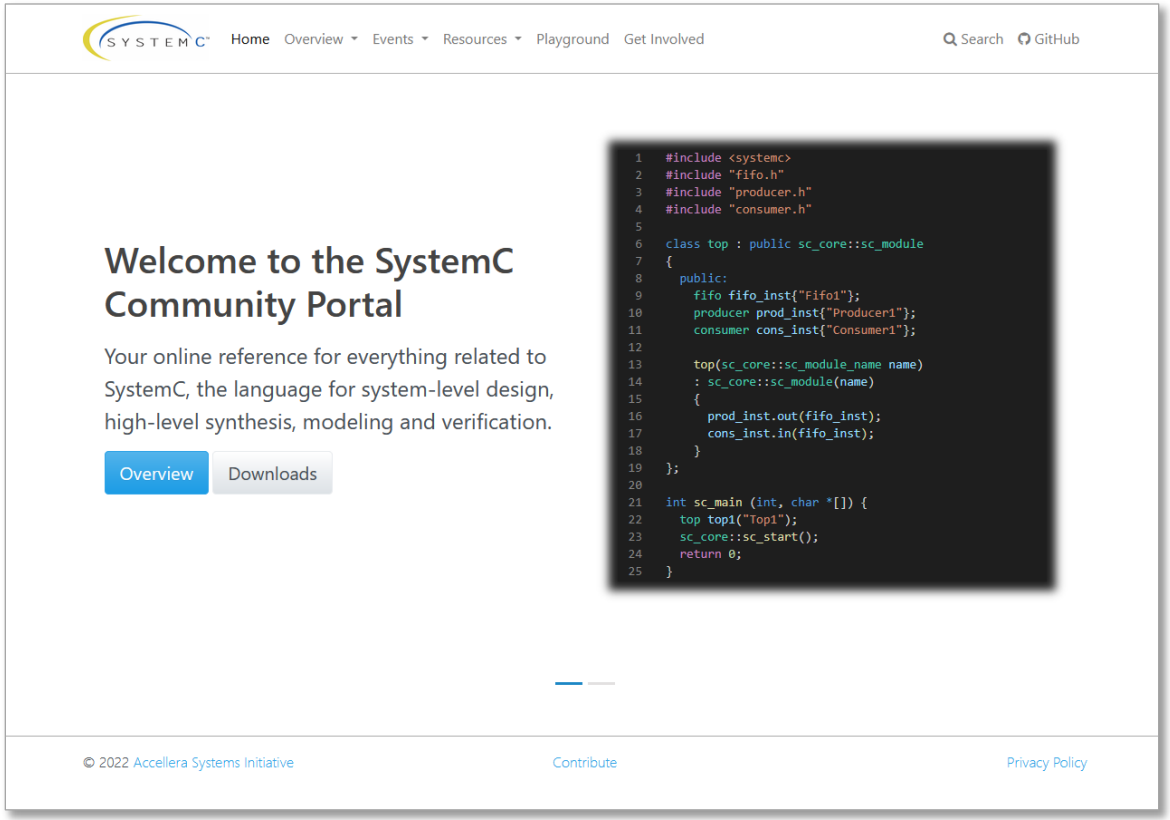
- **SystemC Verification Working Group released UVM-SystemC Library 1.0-beta6**
  - Reference Implementation of UVM in SystemC
  - Compatible with SystemC 3.0.0
  - Public Review open till September 6, 2024

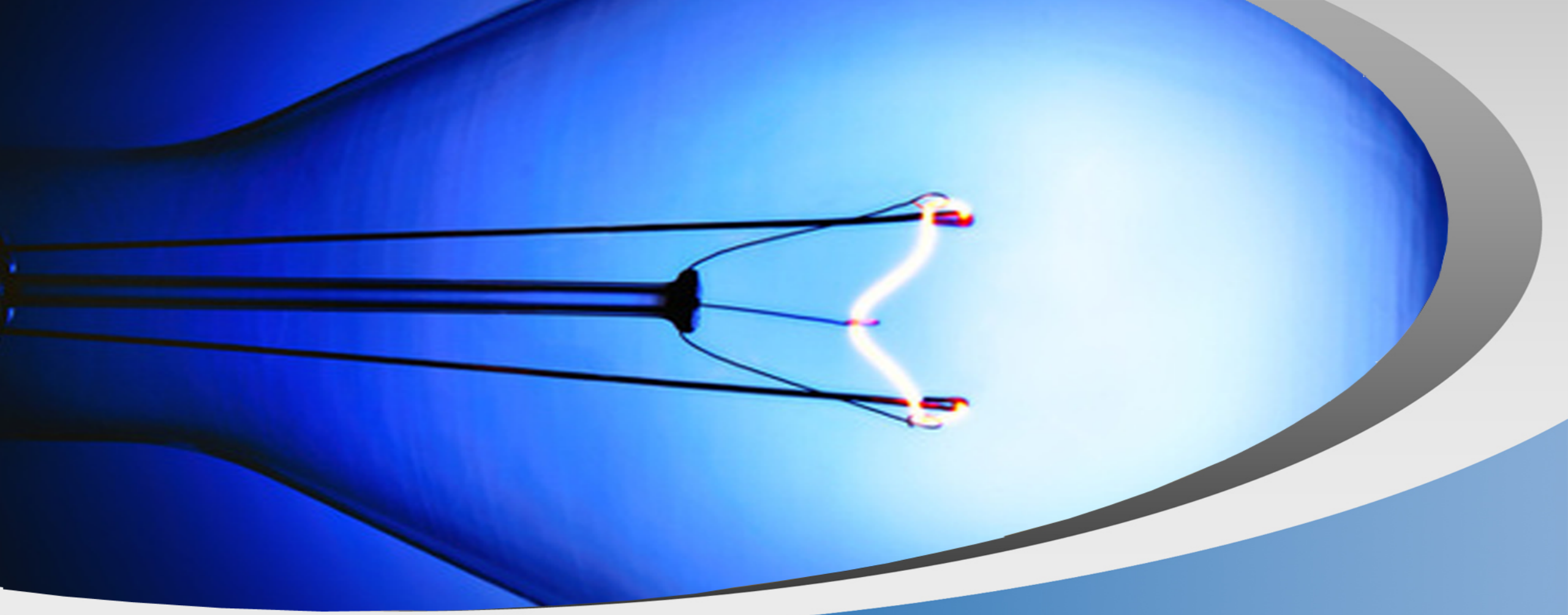
- **SystemC Configuration Control Inspection (CCI) developments**
  - Available via Accellera public repository on GitHub
  - Improved build and release flow using CMake
  - Compatible with SystemC 3.0.0
  - Standardization of memory inspection API ongoing



SystemC standards and eco-system

- **Visit SystemC.org for the latest news and developments**
- **Latest updates**
  - All presentations of SystemC Evolution Day and Fikas are available for download
  - Libraries and Projects page
- **Next Event: SystemC Evolution Day 2024**
  - Full day F2F event, 17 October 2024, Munich, Germany
- **Feel free to contribute to systemc.org**
  - Submit your pull request to github.com/accellera-official/systemc.org





THANK YOU!

More info: accellera.org and systemc.org

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