Fault Effect Propagation using Verilog-A for Analog Test Coverage

Aishwarya Prabhakaran
Ahmed Sokar
Jaafar Mejri
Agenda

1. Analog Fault Simulation
2. Modeling Methodology overview
3. Test Circuits and results
4. Future Work and Conclusion
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Motivation

› Several field returns (metal shorts, opens), which were not detected by the ATE test program

› Optimize test time and cost for circuits by evaluating the test program in regard of over-testing and under-testing

› Formally report and proof test coverage to customers

› Compliance to IEEE standard (working group IEEE p2427)

Example: Field return
Side Benefits

› In the functional safety domain, inject the defects in the fault catalog and check whether the safety mechanisms are excited
› Qualify the Design For Test (DFT) circuitry with defect coverage metric
› Testbenches qualification in mixed-signal verification
First Preliminary Flow Proposal

- **DUT**
- **Test-benches**
- **Defect Extraction**
- **Defect List**
- **Smart Simulation Engines**
- **Detected Faults Statistics**

Adaptations at each step.
Fault models

Schematic

- Transistor
  - Stuck-at-on
  - Stuck-at-off
- Resistance
  - Short
  - Open
- Cap
  - Short
  - Open
- User Defined Faults
- Parametric defects

Layout

- Parasitic based fault extraction

Potential short circuit

Potential open circuit
Why is there no analog test coverage?

› A high side switch contains around 100k Transistors was examined in Infineon

› According to IEEE standard draft, open and short circuits are mandatory to simulate

› After excluding some complex blocks, all the digital part, and some metal layers and vias, total number of possible defects was over 50k.

› One simulation takes ~8 hours

„50,000 defects → years of simulations and high licenses cost”
Simulation speed up

› Parallel Defect Simulation
› Fault Collapsing
› Random Sampling of the defects to estimate the coverage with certain confidence.
› Fault Sensitivity Analysis (FSA)
› Define levels of detectability
  – Undetected, detected, and undetectable defects
  – Find worst corner for Process Voltage Temperature variation
› Start with the defects that have more likelihood and stop after a sufficient coverage is reached
› Simulating defects in abstract-level surrounding[Model the surrounding blocks where a defect is injected]
Using Models in AFS context

Definitions:

› Block under Test
  ▪ Source block into which faults are injected

› Defect effect propagation path
  ▪ From the source block to the observation point

› Blocks on the propagation path
  ▪ Abstract models capable of propagating fault effect

Can the abstract models propagate the fault effect?
Overview of the Methodology

Augment a shell to the model that covers the fault effects

\[ \text{Accuracy (in \%)} = \frac{\text{Measure}_{\text{Transistor model}} - \text{Measure}_{\text{Abstract model}}}{\text{Measure}_{\text{Transistor model}}} \times 100 \]

\[ \text{Speedup Factor} = \frac{\text{Simulation Time}_{\text{Transistor model}}}{\text{Simulation Time}_{\text{Abstract mode}}} \times 100 \]
Overview of the Methodology

- Fault injection on the source block
  - To identify the fault effects to propagate
- Target block Model abstraction
  - Model augmented with fault effects
- Fault simulation
  - With source block and abstract models to speed up the simulation
Fault Injection

› Fault model

› Fault injection flow

› Fault extraction from the transistor level
  - Large number of faults

› Possible faults extracted from the layout

› Batch mode simulation in Regression environment
Fault list generation and reduction

- Bandgap Reference
- Voltage to current conversion
- Current controlled Oscillator

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Parallel simulation</td>
<td>40</td>
</tr>
<tr>
<td>Number of faults simulated</td>
<td>375</td>
</tr>
<tr>
<td>Fault type</td>
<td>Short</td>
</tr>
<tr>
<td>Fault resistance</td>
<td>10 Ω</td>
</tr>
</tbody>
</table>

- Percentage of faults that lead to performance deviation: 18%
- Percentage of faults that has no effect on the performance: 82%
Model abstraction in steps

› One target block at a time to model

- Level 1
  - Source
  - Target
  - Fault effect propagation with shell appended VA model

- Level 2
  - Source
  - Target

- Level n
  - Source
  - Target
  - Observation point
Exclude some blocks

- Do all the target blocks require shell to include fault effects?
  - Target circuit selection
- Some circuits propagate faults without any shell
  - Analog switch
Model abstraction

Fault Simulation

Record Faulty response

Generate Fault List

VDD

Out

In1

In2

Fault Injection

VDD

Out

In1

In2

Measurement setup

M1 = Maximum(Out)

M2 = Minimum(Out)

Script

Regression tool

Script

VDD

T

In

Out

Source

Circuit to Model

Script

Circuit to Model

Script

VDD

T

In

Out

Measurement setup

M1 = Maximum(Out)

Mn = Frequency(Out)
Mapping with Look-Up Tables

Measurements are done on the continuous signals
• Need for interpolation (in the case of slight variation in the input value)
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Experiment Result

› Experiment setup

![Diagram of the experiment setup]

› Parameters chosen for measurements

<table>
<thead>
<tr>
<th>Input Parameters</th>
<th>Output Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>Frequency</td>
</tr>
<tr>
<td>Temperature</td>
<td>Duty cycle</td>
</tr>
<tr>
<td>Input reference current</td>
<td>Phase</td>
</tr>
<tr>
<td>Load resistance</td>
<td>Rise time</td>
</tr>
<tr>
<td></td>
<td>Fall time</td>
</tr>
<tr>
<td></td>
<td>Average output voltage</td>
</tr>
</tbody>
</table>

› Oscillator model with Look-Up Tables

![Diagram of the oscillator model with Look-Up Tables]
Model parameters distribution vs defects

- The distribution of Oscillator input current and its frequency for faults injected in Bandgap Reference Circuit
Equivalence Checking

Transistor Model Test bench
Out_param_1
Out_param_2
... 
Out_param_n

Abstract Model Test bench
Out_param_1
Out_param_2
... 
Out_param_n

Secondary Test bench
measure(out_param_1, out_param_1)
measure(out_param_2, out_param_2)
... 
measure(out_param_n, out_param_n)

Regression Tool
Experiment Result

- **Oscillator input current**

- **Oscillator Frequency**

- **Oscillator Dutycycle**

- **Oscillator Phase**

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Interpolation accuracy for the input reference current sweep with step size 1uA
Experiment Result

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transient simulation time</td>
<td>3 us</td>
</tr>
<tr>
<td>Time step</td>
<td>100 ps</td>
</tr>
<tr>
<td>Number of Parallel simulation</td>
<td>40</td>
</tr>
<tr>
<td>Number of faults simulated</td>
<td>375</td>
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<td>Fault type</td>
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Simulation time: Transistor model vs Abstract model

- Speedup = 4.608

Storage: Oscillator's Schematic vs its Model with LUTs
The voltage-to-current takes two inputs from Bandgap Reference circuit and outputs a current that controls the Oscillator.
Using the Abstract Models for fault injection

- To speed up the process of generating abstract models (target blocks)

![Diagram of abstract models for fault injection](image-url)
Modified Flow and its Result

Flow to generate Fault model of a circuit

Experimental results

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Faults simulated</td>
<td>100</td>
</tr>
<tr>
<td>Simulation time</td>
<td>50 us</td>
</tr>
<tr>
<td>Time step</td>
<td>100 ps</td>
</tr>
<tr>
<td>Number of parallel runs</td>
<td>40</td>
</tr>
<tr>
<td>Speed up</td>
<td>10x</td>
</tr>
</tbody>
</table>

Storage of CSV files
Fault Simulation – Full chain

Blocks on the target path

Experiment Setup

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Transient simulation time</td>
<td>5 us</td>
</tr>
<tr>
<td>Time step</td>
<td>100 ps</td>
</tr>
<tr>
<td>Number of Parallel simulation</td>
<td>40</td>
</tr>
<tr>
<td>Number of faults simulated</td>
<td>375</td>
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<td>Fault type</td>
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![Bar chart showing simulation time comparison between Transistor model and Abstract model with a speedup of 10.39x]
Fault Simulation – Experiment Result

**Fault detection results**

- Percentage of faults that are detectable: 36%
- Percentage of faults whose effect deviate by 10% from the fault-free case: 13%
- Percentage of faults that produce the same effect as the fault-free case: 51%

**Parameter** | **Value**
--- | ---
Transient simulation time | 20 us
Time step | 100 ps
Number of Parallel simulation | 40
Number of faults simulated | 375
Fault type | Short
Fault resistance | 10 Ω

**Distribution of the average current measured at the load**

- Full simulation time – 35 mins (app)

- 36% - faults dropped
- 64% - Different test pattern must be chosen to detect these faults

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Conclusion and Future Work

› AFS at the system level

› Abstract models to speed up AFS

› Fault effect propagation with shell appended behavior models
  - Performance metrics mapped to faulty inputs using LUT
  - Multi-dimensional mapping
  - Applicable to Closed-loop systems

Performance results
  - A simple, multi-dimensional, LUT mapping with interpolation
  - Speedup of about 10 times
  - Accuracy close to 100%
  - Storage size in few KBs

Future Work
  › Propagation path tracing using Sensitivity analysis
  › Fault collapsing using clustering algorithms
  › Automation of Model abstraction and Fault simulation at the System level
References


Part of your life. Part of tomorrow.
Closed loop system

Modeling the transient response as a time series
- Inefficient

Performance modeling

$I_{\text{ref}}$ affects the performance of the Op-Amp
Closed loop system - Experiment Result

Equivalence checking

[Graph showing experimental results]
Closed loop system - Experiment Result

Op-Amp output voltage with faults injected in Bandgap Reference circuit

Storage space of Op-Amp
Schematic vs Model