Fast and Furious
Quick Innovation from Idea to Real Prototype

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accellera SYSTEMS INITIATIVE

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Agenda

- Motivation
- Methodology
- Results and Conclusions

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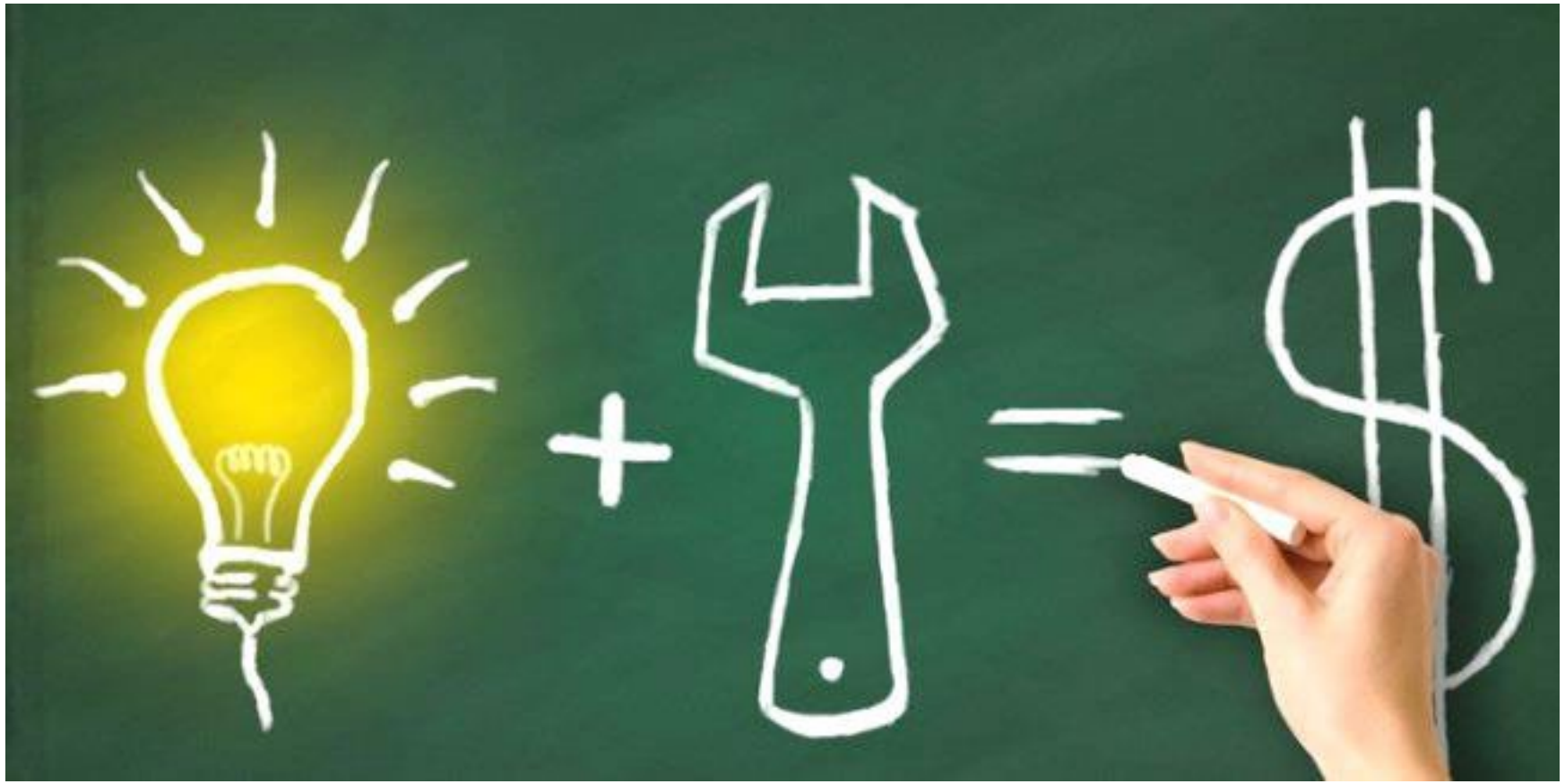
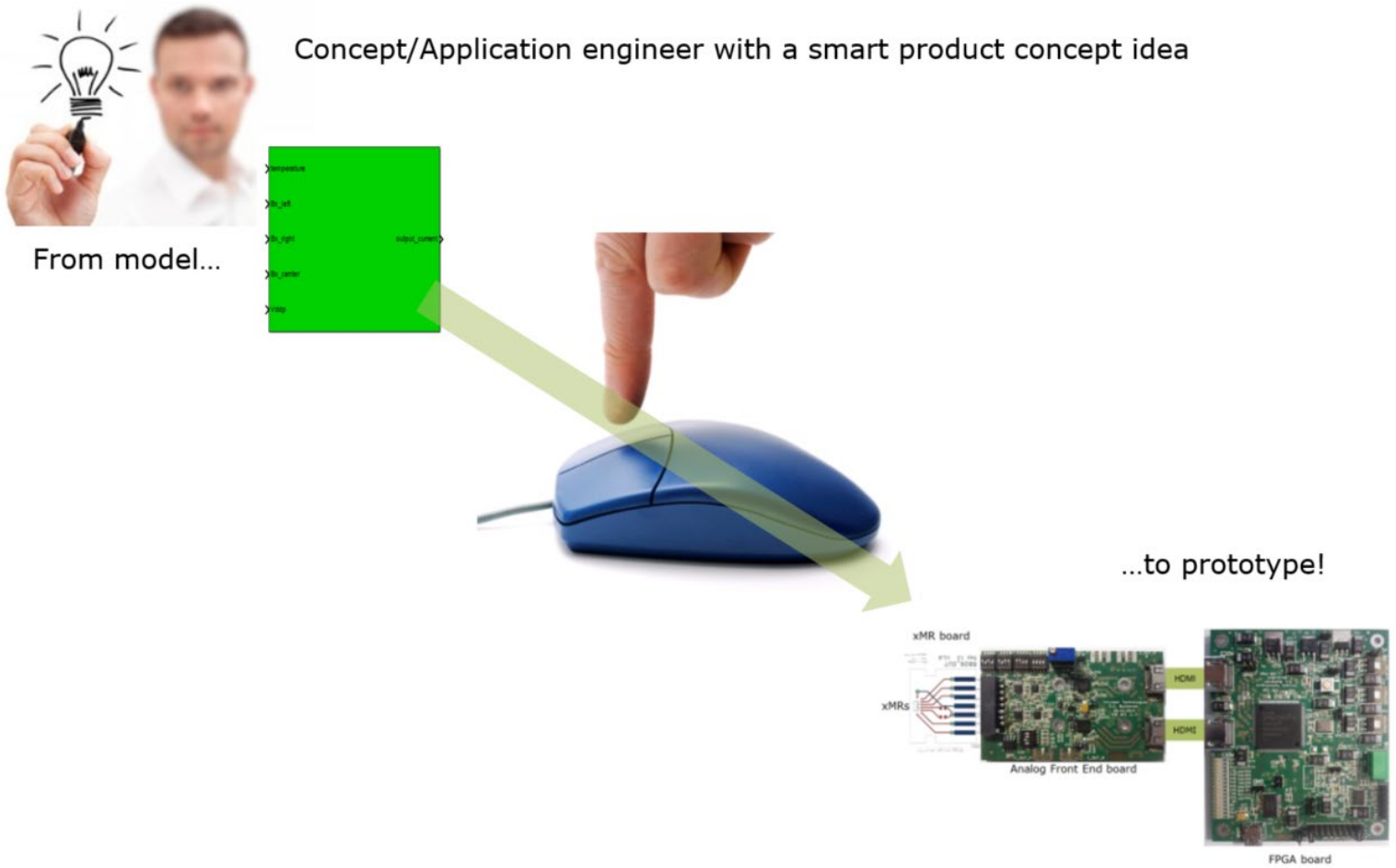
Selling an idea with a prototype



A possible approach…

…Our vision!


Concept/Application engineer with a smart product concept idea
From model…
…to prototype!
xMR board
xMRs
HDMI
HDMI
Analog Front End board
FPGA board

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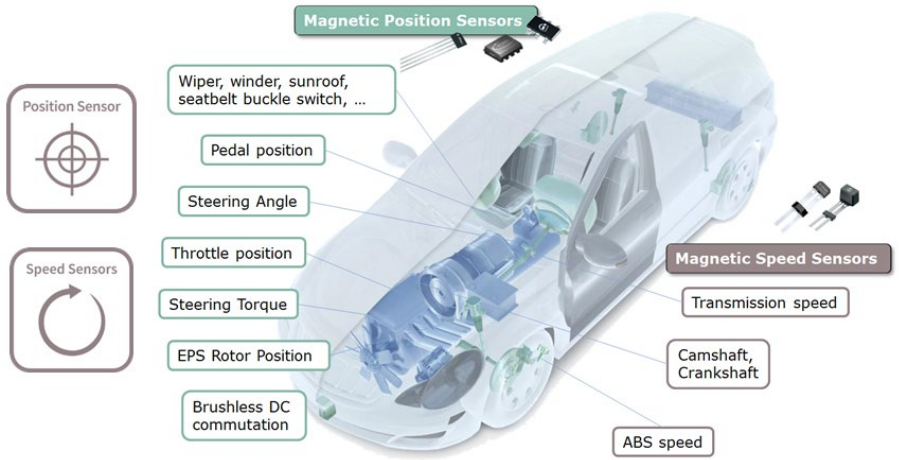
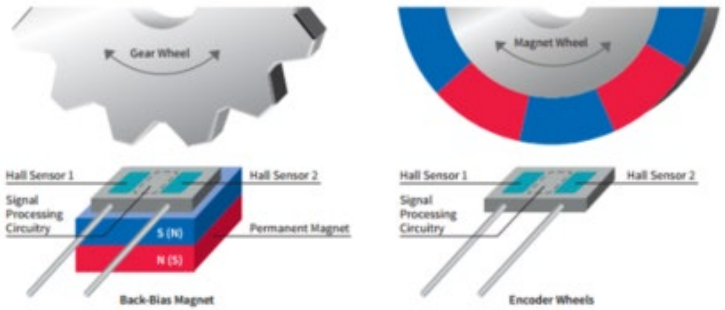
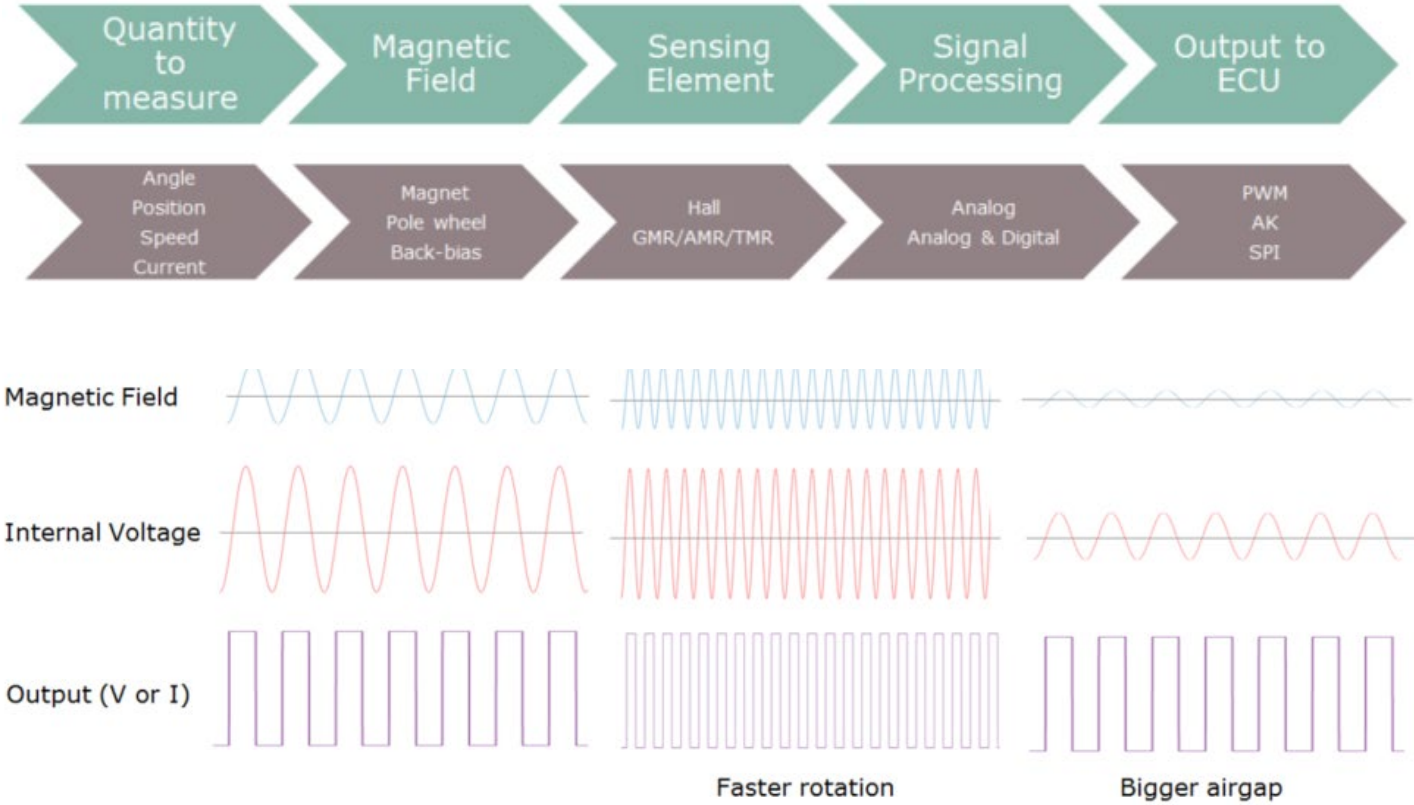
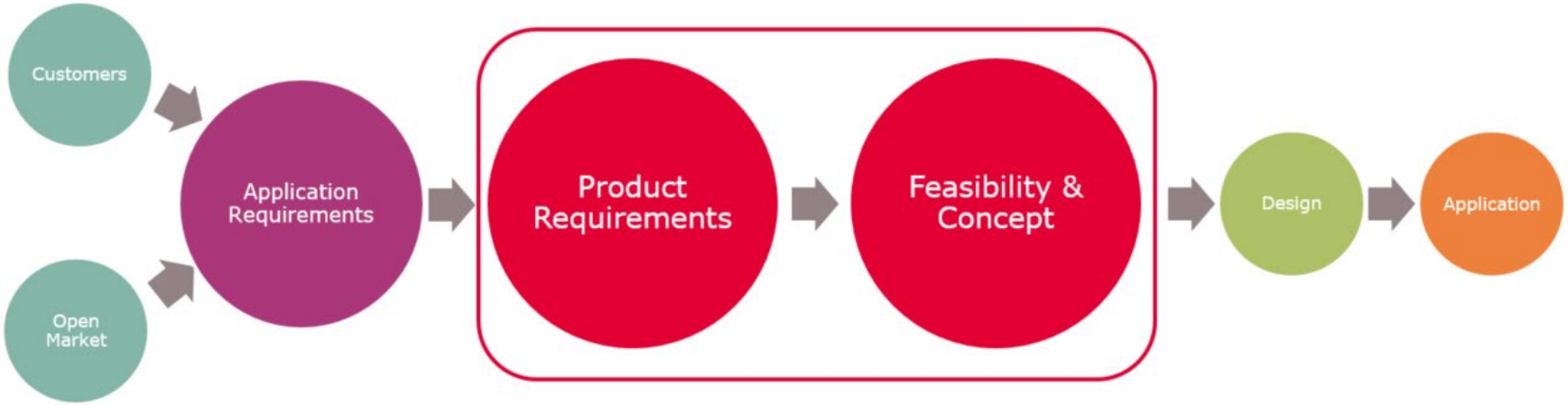
Magnetic sensors for automotive applications

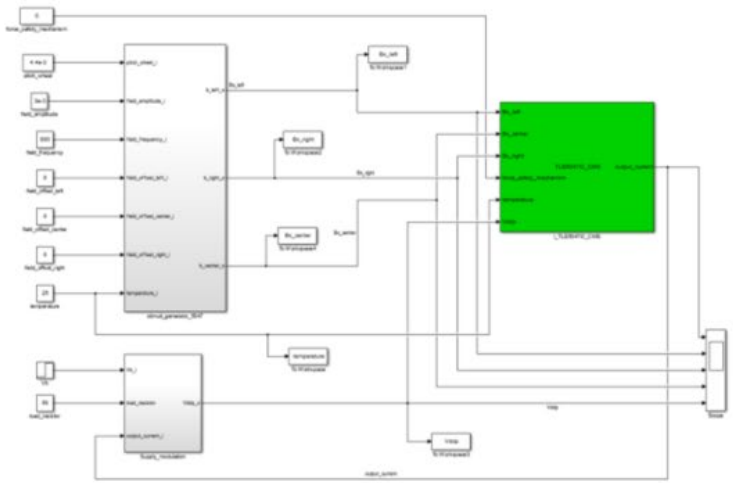


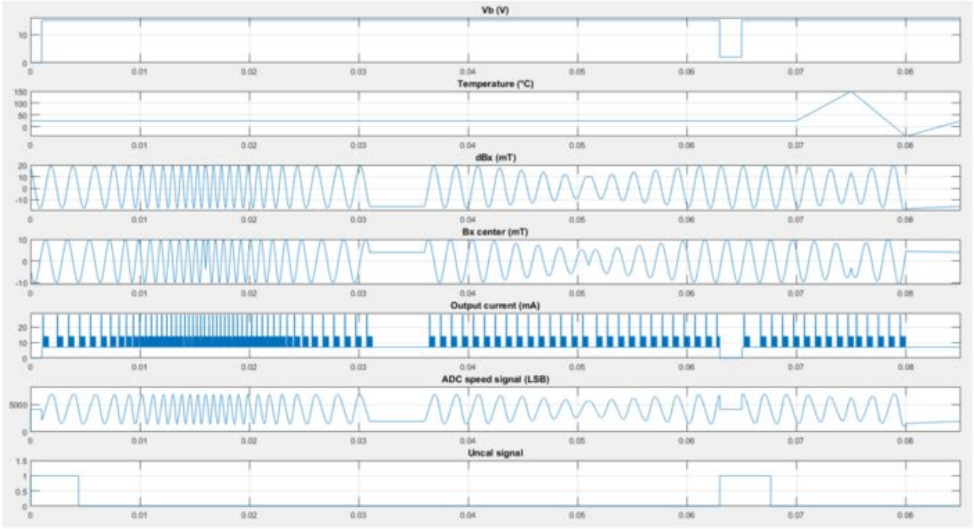




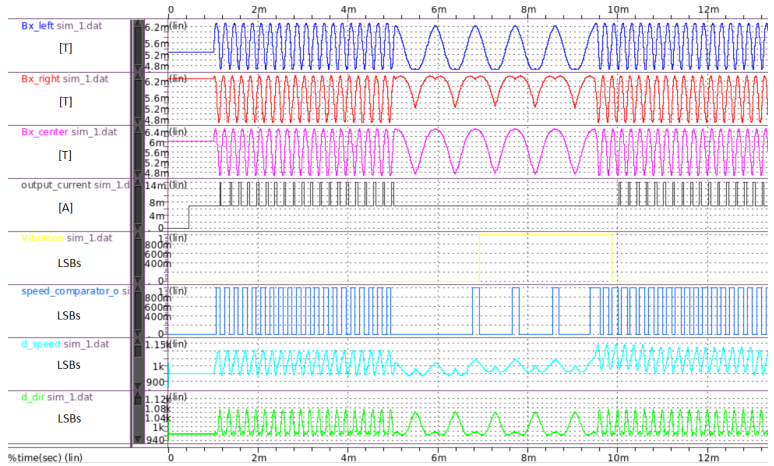
Virtual prototyping for concept definition

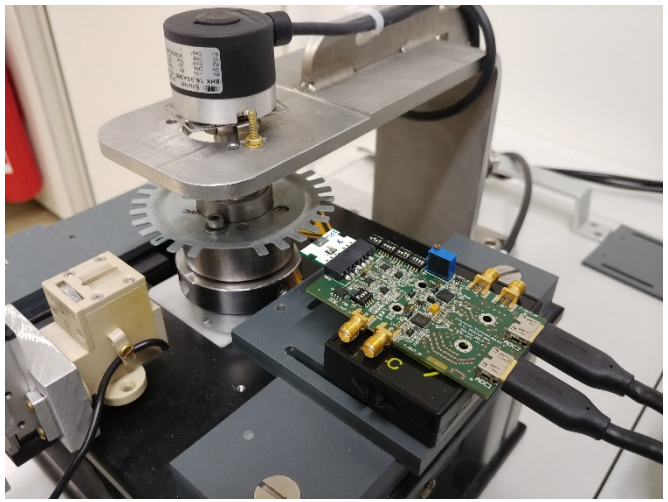




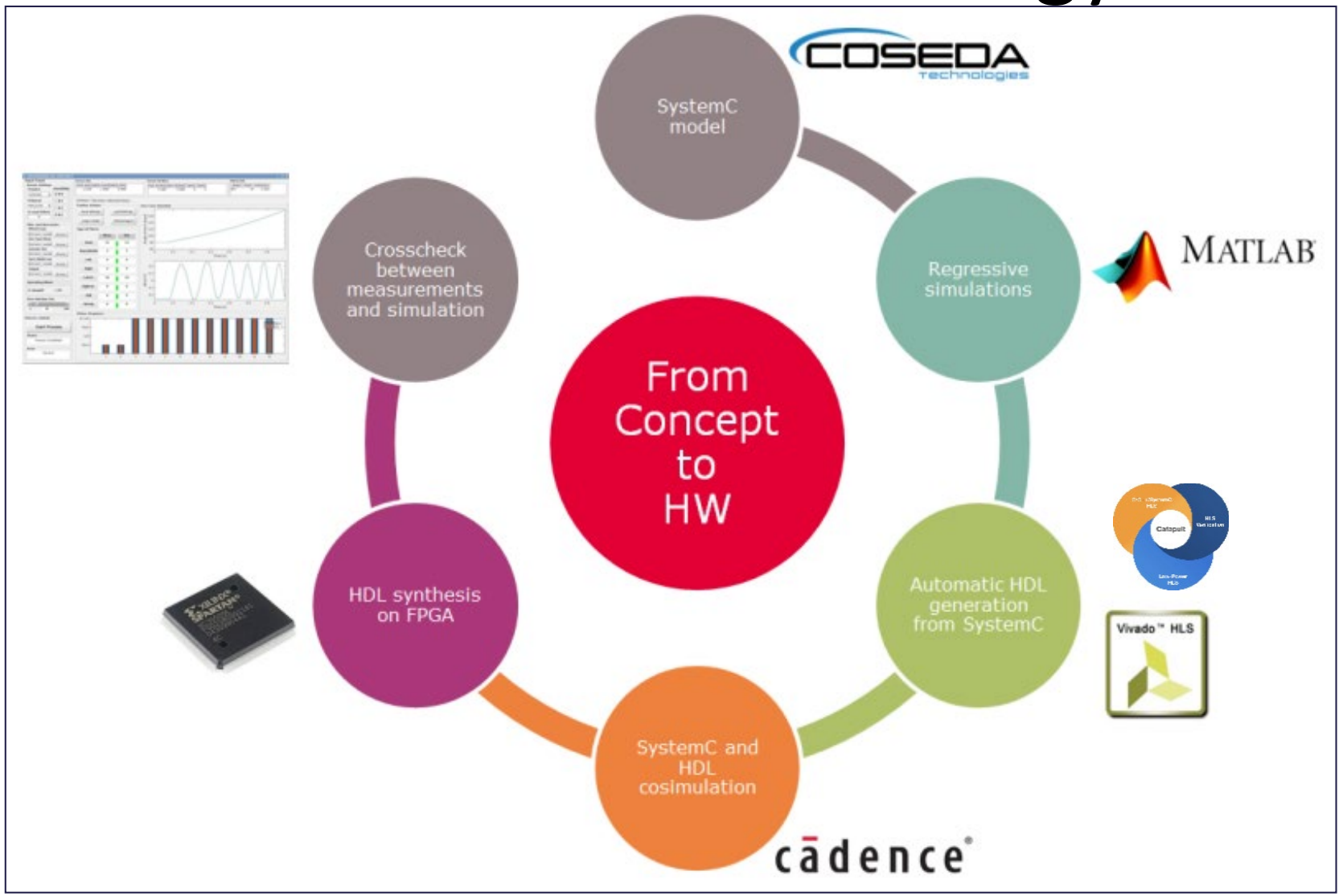


From simulation to real HW

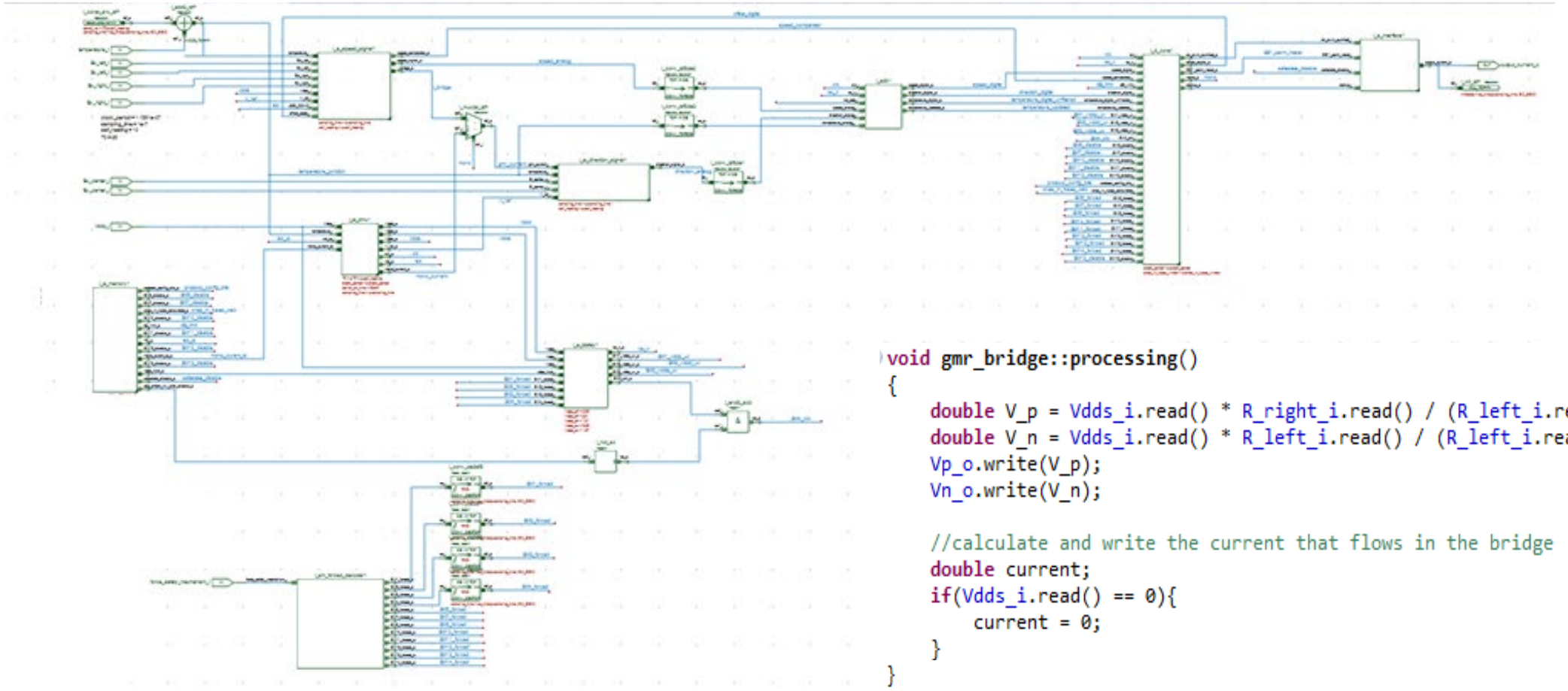




Fast & Furious: the methodology in a nutshell



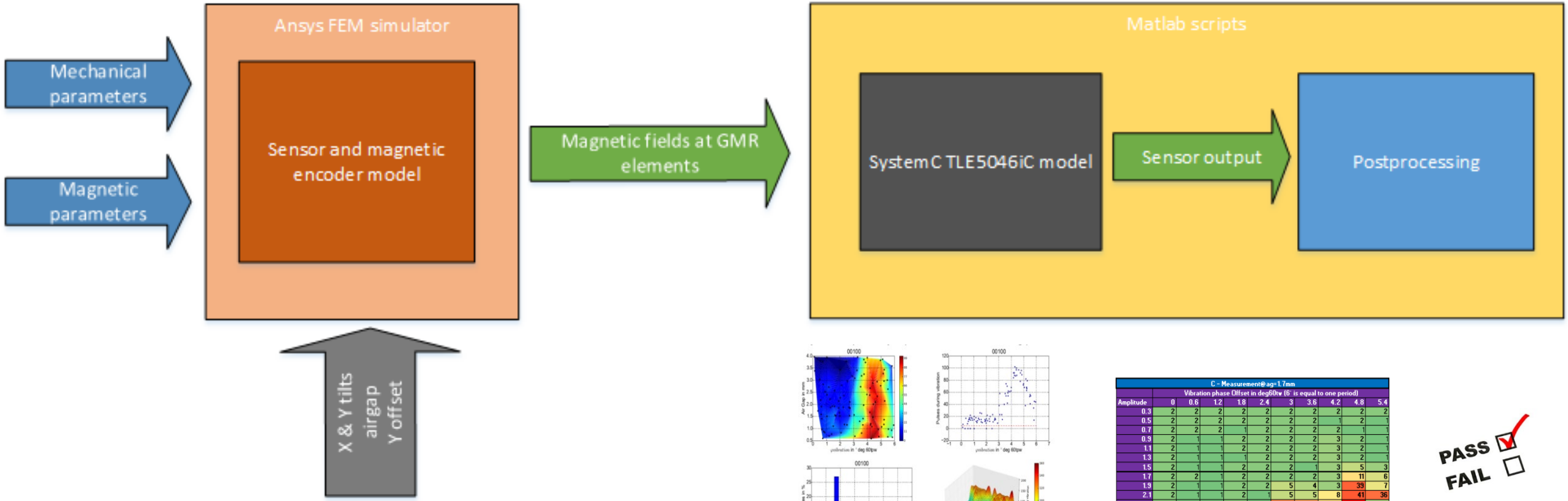
SystemC Modeling



```
void gmr_bridge::processing()
{
    double V_p = Vdds_i.read() * R_right_i.read() / (R_left_i.read() + R_right_i.read());
    double V_n = Vdds_i.read() * R_left_i.read() / (R_left_i.read() + R_right_i.read());
    Vp_o.write(V_p);
    Vn_o.write(V_n);

    //calculate and write the current that flows in the bridge
    double current;
    if(Vdds_i.read() == 0){
        current = 0;
    }
}
```

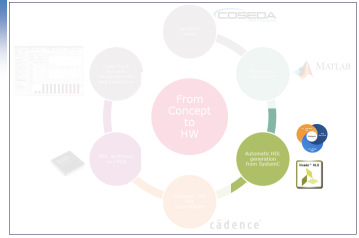
Regressive simulations



C - Measurement@ag=1.7mm									
	Vibration phase Offset in deg@tw (6° is equal to one period)								
Amplitude	0	0.6	1.2	1.8	2.4	3	3.6	4.2	4.8	5.4
0.3	2	2	2	2	2	2	2	2	2	2
0.5	2	2	2	2	2	2	2	1	2	1
0.7	2	2	2	1	2	2	2	1	1	1
0.9	2	1	1	2	2	2	2	3	2	1
1.1	2	1	1	2	2	2	2	3	2	1
1.3	2	1	1	1	2	2	2	3	2	1
1.5	2	1	1	2	2	2	1	3	5	3
1.7	2	2	1	2	2	2	2	3	11	6
1.9	2	1	1	2	2	5	4	3	39	7
2.1	2	1	1	2	1	5	5	8	41	36
2.3	2	1	1	2	1	29	24	11	60	4
2.5	2	1	1	2	1	23	9	49	58	3
2.7	2	1	1	2	1	5	13	57	61	2
2.9	1	1	1	2	1	7	57	59	61	2
3.1	2	1	1	2	1	8	61	61	57	2

PASS ☑
FAIL ☐

From SystemC to HDL in a few clicks

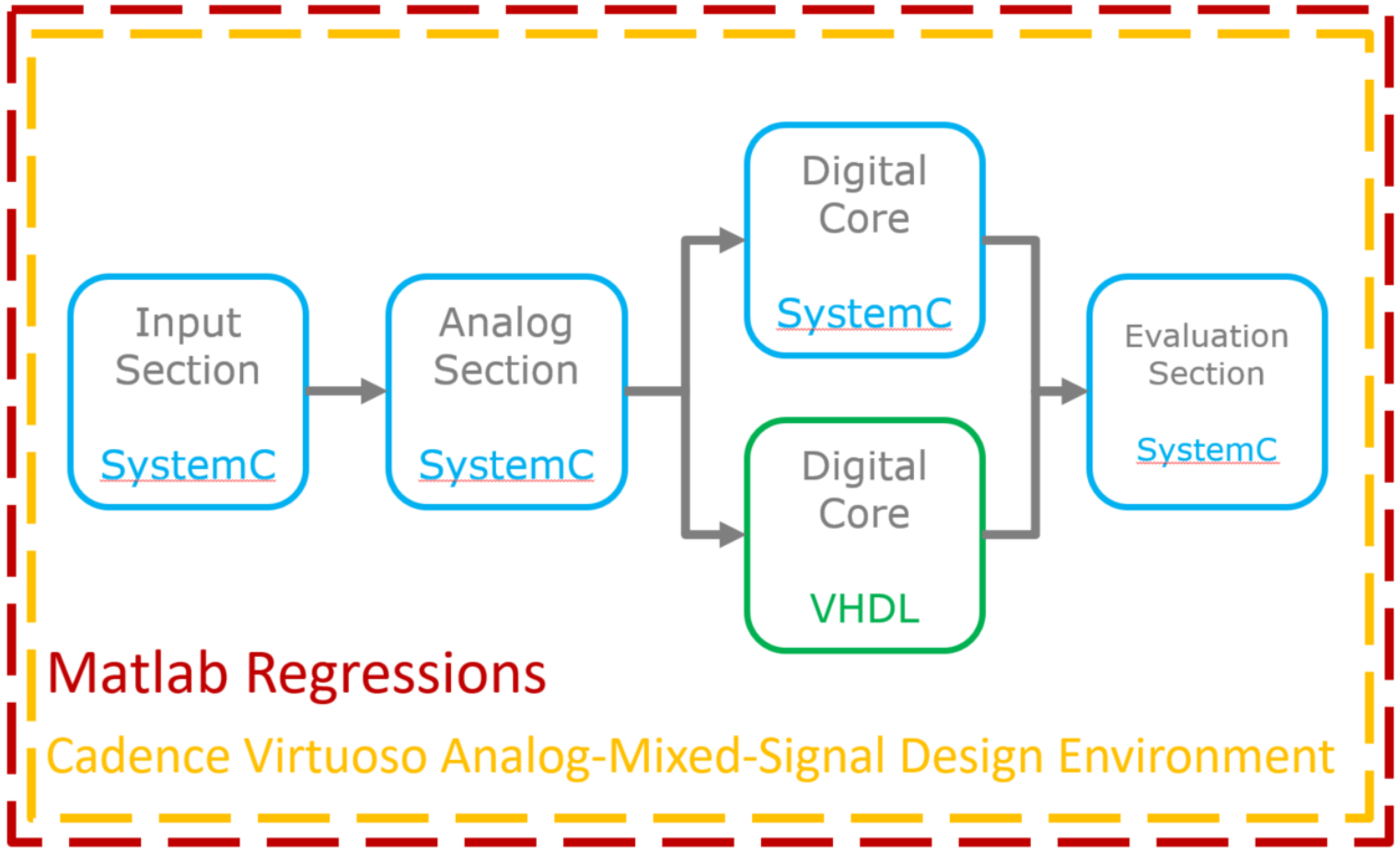


- SystemC „clean“ netlist from COSIDE®
- Conversion of each SystemC module
- Conversion of top-level
- High level synthesis
  - Vivado HLS
  - Mentor Catapult

VIDEO SHOWING THE AUTOMATIC CONVERSION PROCESS

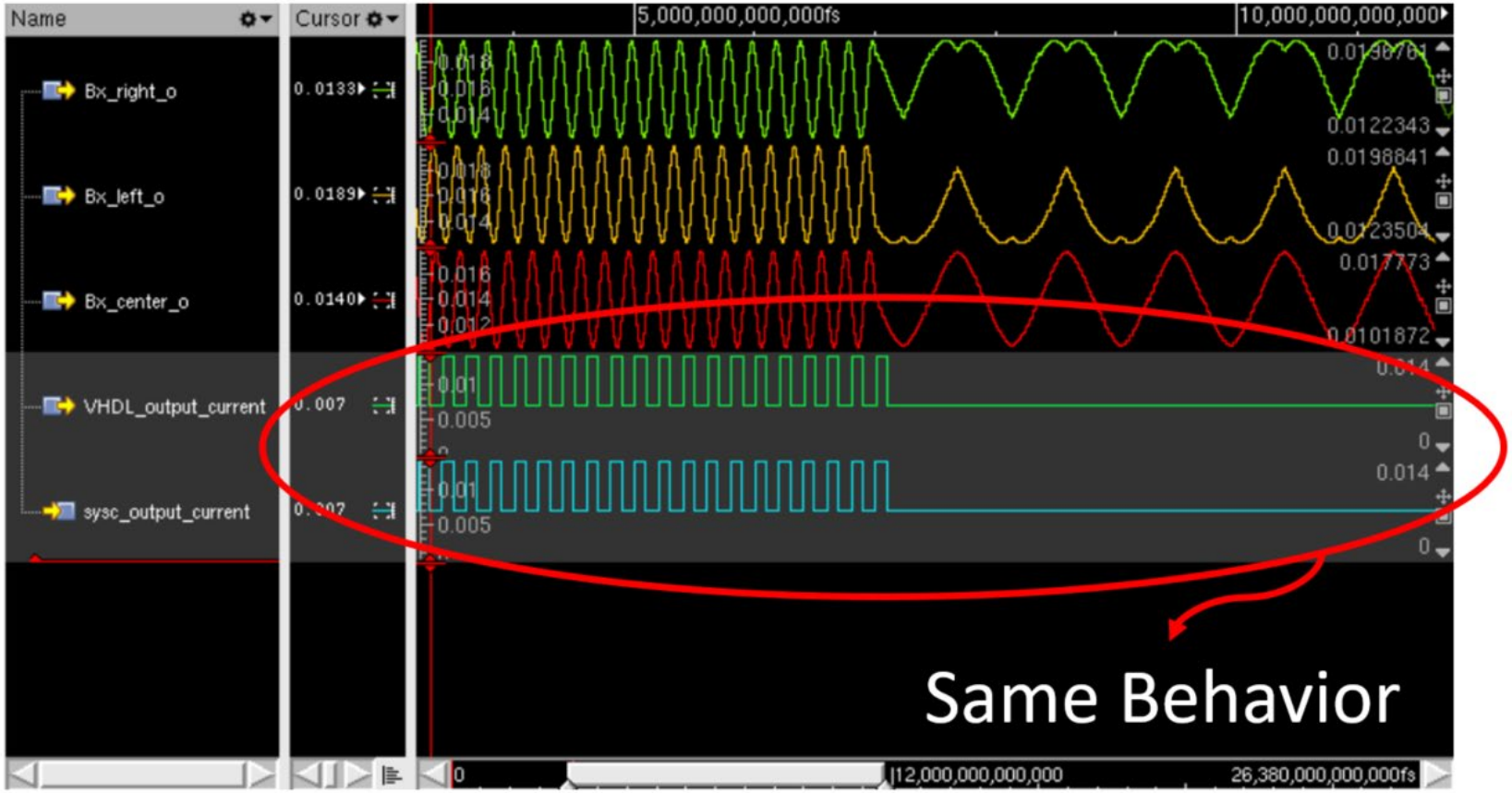
I CANNOT PUT IT INTO THE SLIDES BECAUSE OTHERWISE THE FILE GETS TOO BIG AND CANNOT UPLOAD IT. FOR THE CONFERENCE I WILL BRING THE PPTX ON A USB STICK

SystemC & VHDL cosimulation (1/2)

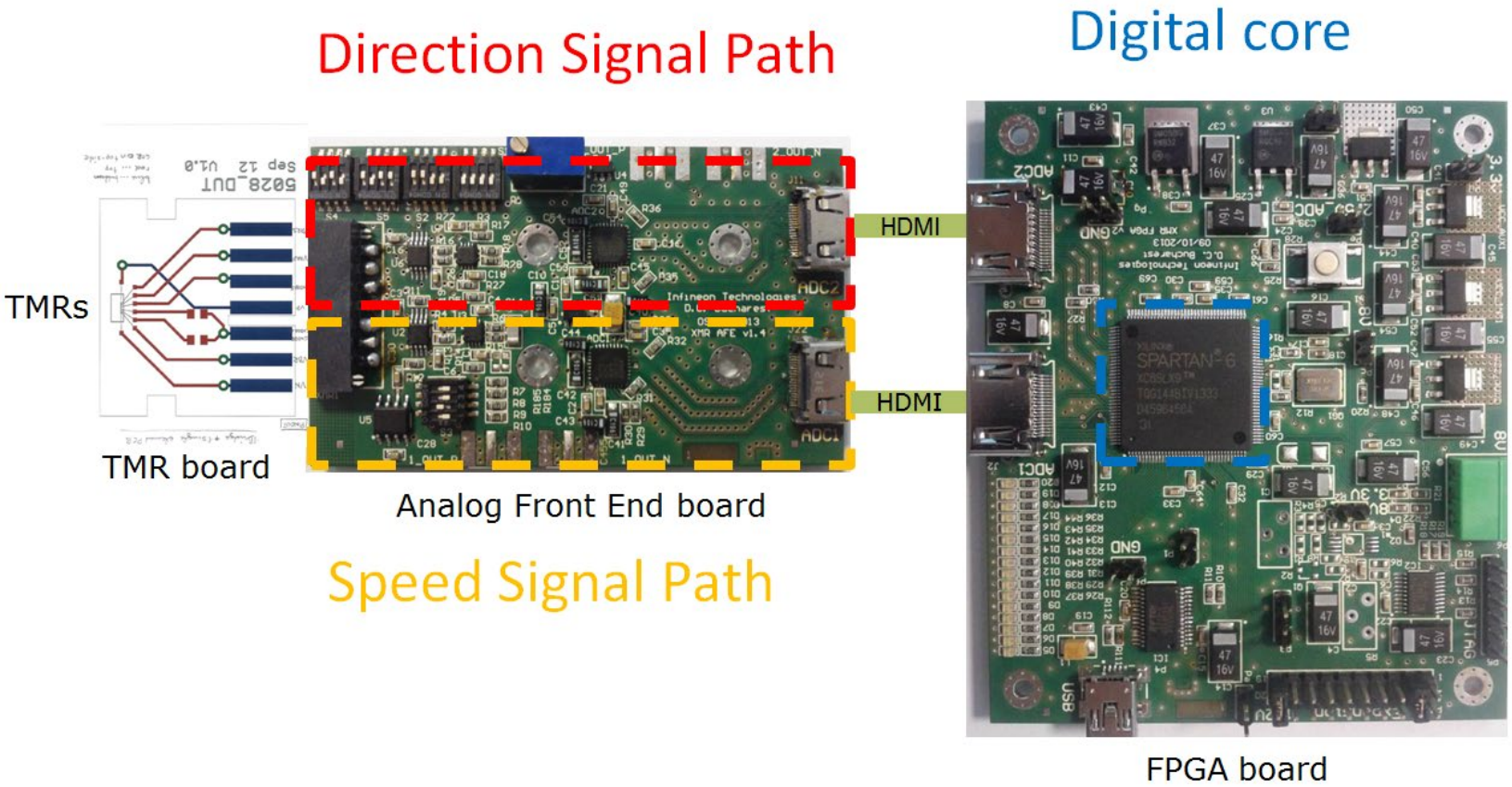


*Note: Mentor Catapult would also allow cosimulation in an integrated environment

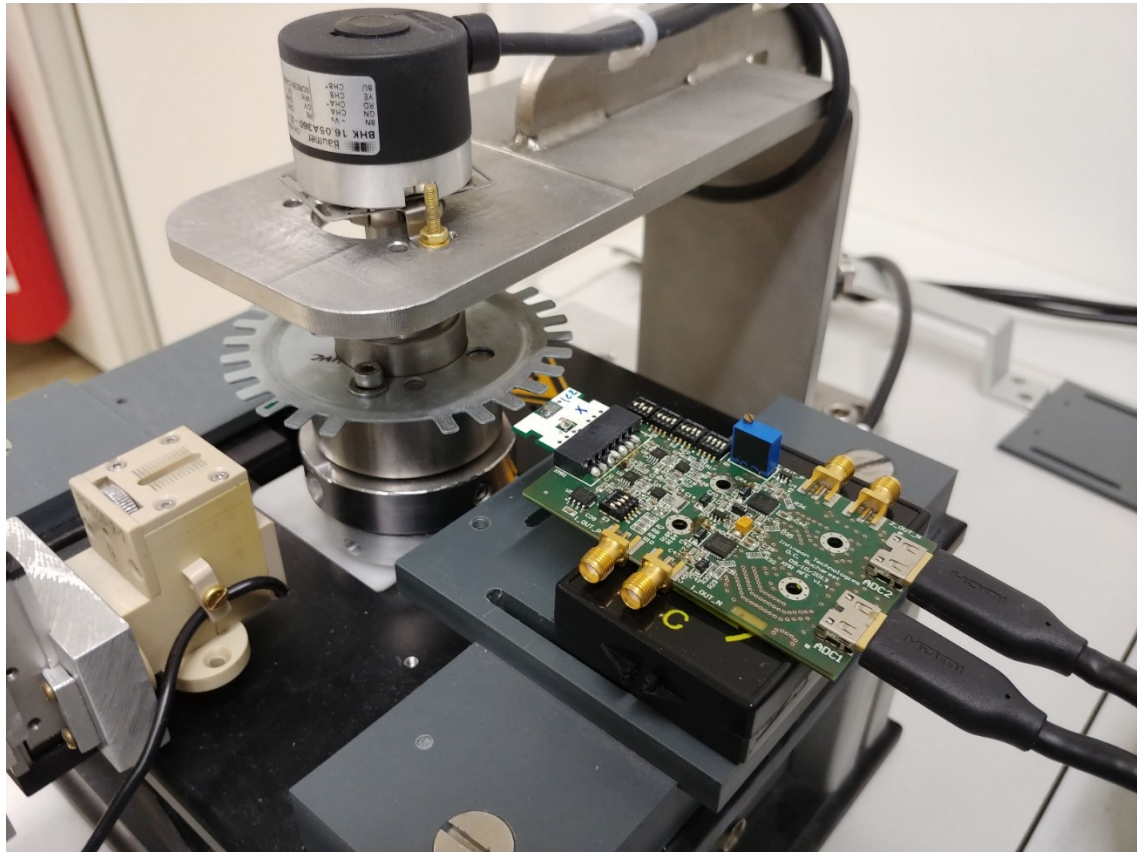
SystemC & VHDL cosimulation (2/2)

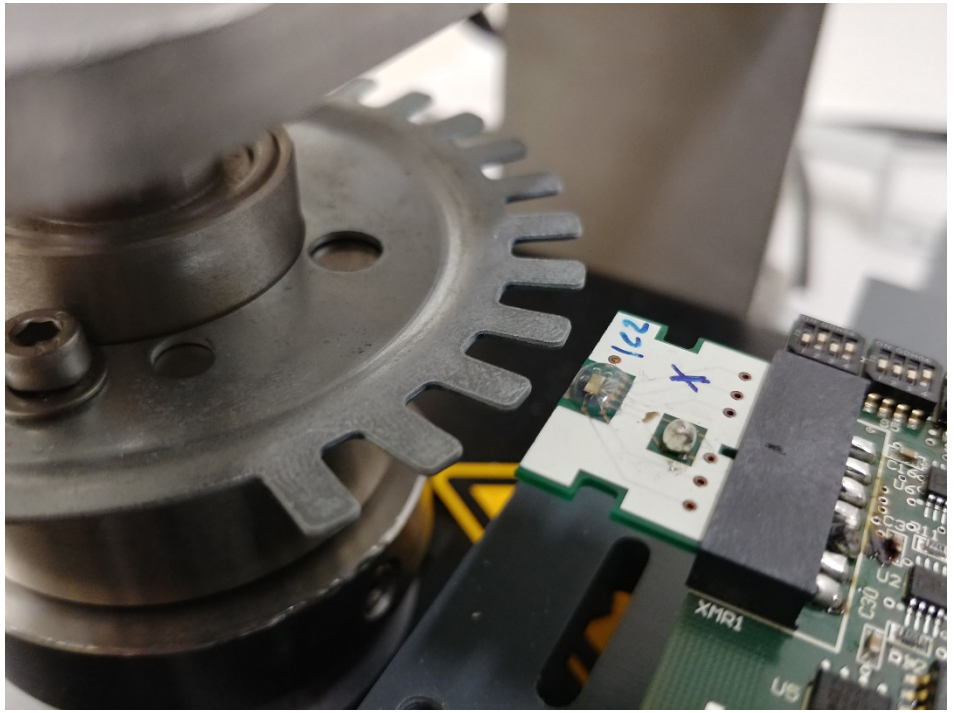


Moving to real HW

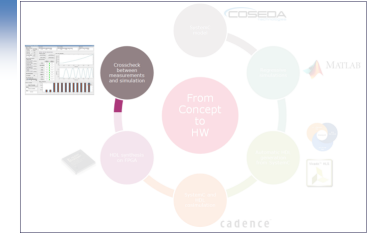


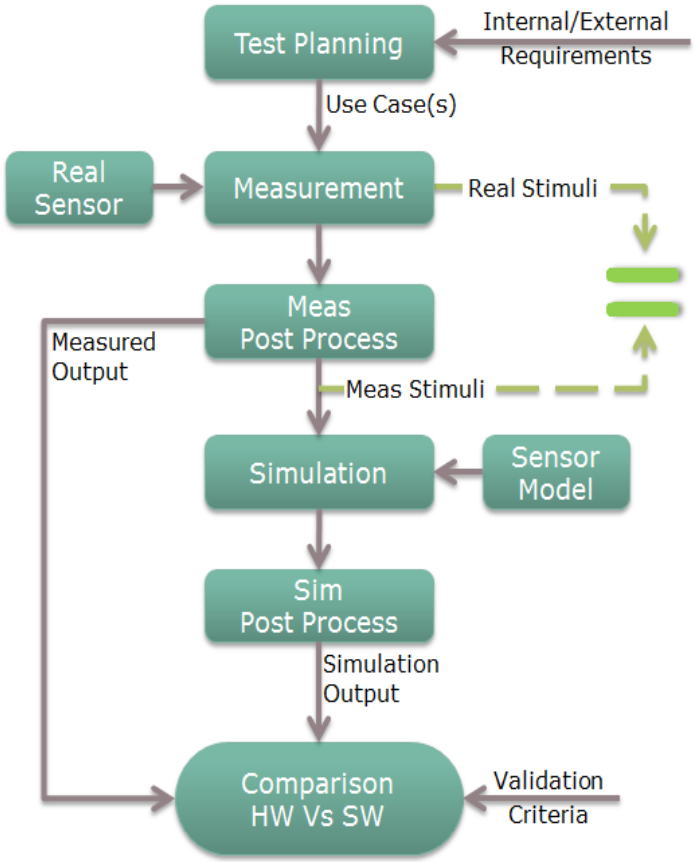
Measurements setup

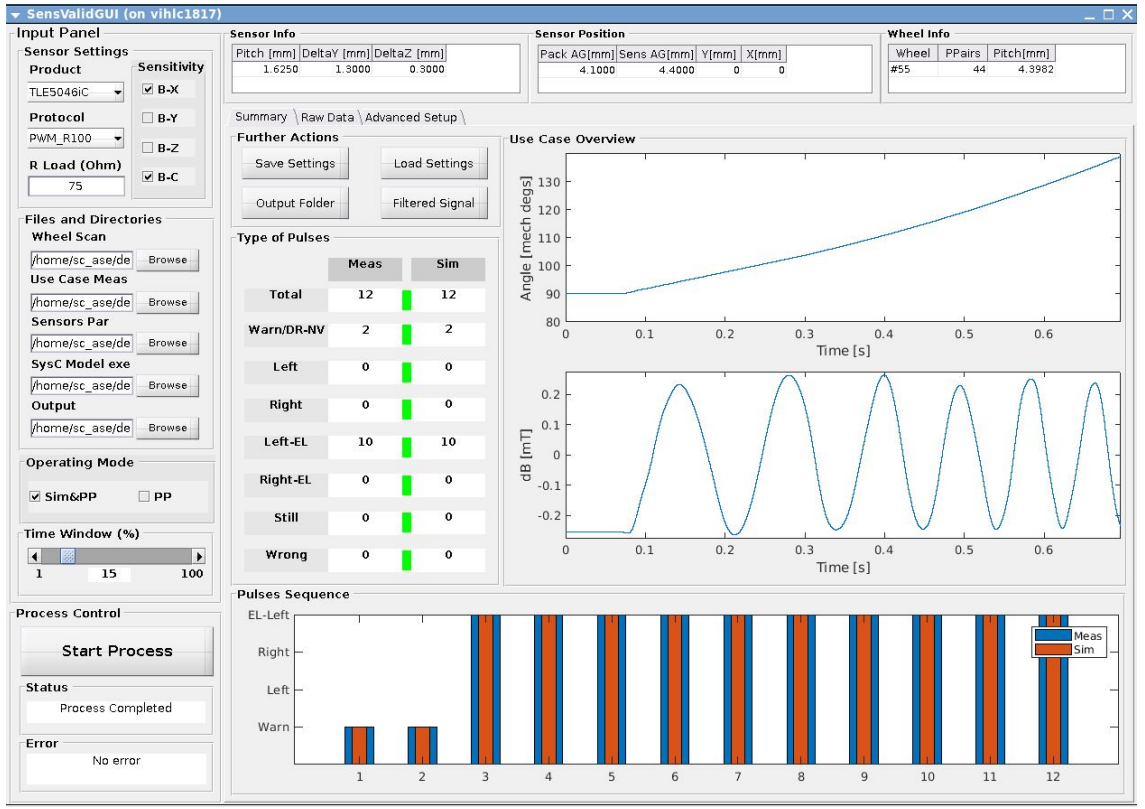




Measurement-simulation crosscheck







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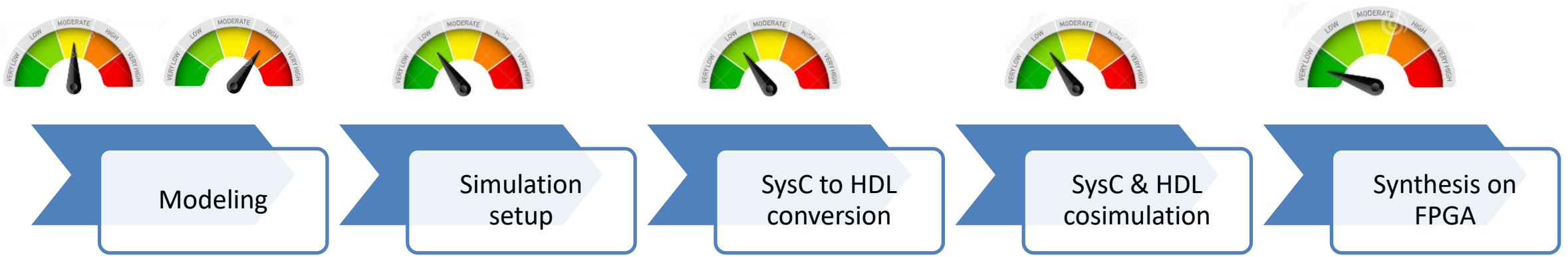
Results and Conclusion (1/3)

How much effort was spent for the different steps in the flow?



- Modeling: 1 month if concept available (SysC reuse) / up to 1 year if concept has to be developed
- Simulation setup: straightforward, just the parameter sweeps and their steps have to be defined
- SysC to HDL conversion: achieved with a one-click approach using Mentor Catapult software
- SysC & HDL cosimulation: made possible by Coseda-Cadence-Bridge (CCB) with one click export
- Synthesis on FPGA possible without any need of modifications, using Xilinx ISE synthesizer

Results and Conclusion (2/3)

- How much time was saved by this methodology?
  - From virtual to real HW prototype: 3 to 6 man / months faster!

- What is the simulation speed of SysC vs. Matlab vs. SysC/HDL co-sim?
  - SystemC : 1ms of simulation → ca. 5 s in the real world
  - Matlab: does not affect the simulation speed, only used to handle the regression
  - SystemC / HDL co-simulation: around 6 times slower than SystemC due to RTL simulation time (dominant)

Results and Conclusion (3/3)

- One-click conversion finally possible
- HDL and SystemC match 1:1 in cosimulation
- Measurements ongoing, correct functionality already observed

- High level synthesis approach
  - Saves development resources and time
  - Increase reuse and speed
- Rapid prototyping approach
  - Increase design confidence
  - Allow better customers interaction

Questions & Answers

Any questions?