Fast and Furious
Quick Innovation from Idea to Real Prototype

Simone Fontanesi, Infineon Technologies Austria AG, Villach, Austria
Gaetano Formato, Infineon Technologies Austria AG, Villach, Austria
Thomas Arndt, COSEDA Technologies GmbH, Dresden, Germany
Andrea Monterastelli, Infineon Technologies Austria AG, Villach, Austria
Agenda

- Motivation
- Methodology
- Results and Conclusions
Agenda

• Motivation
• Methodology
• Results and Conclusions
Selling an idea with a prototype
A possible approach...
...Our vision!

Concept/Application engineer with a smart product concept idea

From model...

...to prototype!
Agenda

• Motivation
• Methodology
• Results and Conclusions
Magnetic sensors for automotive applications
Virtual prototyping for concept definition
From simulation to real HW
Fast & Furious: the methodology in a nutshell
void gmr_bridge::processing()
{
    double V_p = Vdds_i.read() * R_right_i.read() / (R_left_i.read() + R_right_i.read());
    double V_n = Vdds_i.read() * R_left_i.read() / (R_left_i.read() + R_right_i.read());
    Vp_o.write(V_p);
    Vn_o.write(V_n);

    // calculate and write the current that flows in the bridge
    double current;
    if(Vdds_i.read() == 0) {
        current = 0;
    } else {
        current = (V_p - V_n) / (R_left_i.read() + R_right_i.read());
    }
    Io_o.write(current);
}
Regressive simulations

Ansys FEM simulator

Sensor and magnetic encoder model

Magnetic fields at GMR elements

Matlab scripts

SystemC TLE5046IC model

Sensor output

Postprocessing

Mechanical parameters

Magnetic parameters

X & Y tilt
Airgap
Y offset

© Accellera Systems Initiative
From SystemC to HDL in a few clicks

- SystemC „clean“ netlist from COSIDE®
- Conversion of each SystemC module
- Conversion of top-level
- High level synthesis
  - Vivado HLS
  - Mentor Catapult

VIDEO SHOWING THE AUTOMATIC CONVERSION PROCESS

I CANNOT PUT IT INTO THE SLIDES BECAUSE OTHERWISE THE FILE GETS TOO BIG AND CANNOT UPLOAD IT. FOR THE CONFERENCE I WILL BRING THE PPTX ON A USB STICK
SystemC & VHDL cosimulation (1/2)

Matlab Regressions
Cadence Virtuoso Analog-Mixed-Signal Design Environment

*Note: Mentor Catapult would also allow cosimulation in an integrated environment
SystemC & VHDL cosimulation (2/2)
Moving to real HW

Direction Signal Path

Digital core

Speed Signal Path

FPGA board

© Accellera Systems Initiative 17
Measurements setup
Measurement-simulation crosscheck
Agenda

• Motivation
• Methodology
• Results and Conclusions
How much effort was spent for the different steps in the flow?

- **Modeling**: 1 month if concept available (SysC reuse) / up to 1 year if concept has to be developed
- **Simulation setup**: straightforward, just the parameter sweeps and their steps have to be defined
- **SysC to HDL conversion**: achieved with a one-click approach using Mentor Catapult software
- **SysC & HDL cosimulation**: made possible by Coseda-Cadence-Bridge (CCB) with one click export
- **Synthesis on FPGA**: possible without any need of modifications, using Xilinx ISE synthesizer
Results and Conclusion (2/3)

• How much time was saved by this methodology?
  – From virtual to real HW prototype: 3 to 6 man / months faster!

• What is the simulation speed of SysC vs. Matlab vs. SysC/HDL co-sim?
  – SystemC: 1ms of simulation \(ightarrow\) ca. 5 s in the real world
  – Matlab: does not affect the simulation speed, only used to handle the regression
  – SystemC / HDL co-simulation: around 6 times slower than SystemC due to RTL simulation time (dominant)
Results and Conclusion (3/3)

• One-click conversion finally possible
• HDL and SystemC match 1:1 in cosimulation
• Measurements ongoing, correct functionality already observed

• High level synthesis approach
  – Saves development resources and time
  – Increase reuse and speed
• Rapid prototyping approach
  – Increase design confidence
  – Allow better customers interaction
Questions & Answers

Any questions?