FPGA Debug Using Configuration Readback

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Overview of topics

• The FPGA world as of Nov’15
  – The HW
    • Xilinx, Altera/Intel, others(?)
  – The SW, at least the third party tools
    • Synopsys, Mentor, et al.

• FPGA Debug
  – Overview of existing products
    • Why this is not a ‘rich’ selection products
    • Identify, ILA/ChipScope, SignalTap, ProtoLink, Certus
      – New variations such as Exostiv

• Remember to disable everything before shipping …
FPGAs ...

• Moore’s Law?
  – Certainly not healthy

• FPGAs no longer a growing market
  – Classically maturing
  – Down in revenue year-to-year
    • 6%-20% depending on how you count
    • Some segments growing
      – Emulation/prototyping

• Both Altera and Xilinx expanding into niches
  – Automotive
  – Embedded systems
  – Data Center

Figure 1 from Three Ages of FPGAs: A Retrospective on the First Thirty Years of FPGA Technology
Steve Trimberger (March 2015)
Figure 1. Xilinx FPGA attributes relative to 1988. Capacity is logic cell count. Speed is same-function performance in programmable fabric. Price is per logic cell. Power is per logic cell. Price and power are scaled up by 10,000. Data: Xilinx published data.
Xilinx

• In the midst of rolling out 20nm generation: UltraScale
  – Kintex/Virtex UltraScale, Zynq
  – Clear leader for the large FPGAs used in prototyping
    • Not the leader elsewhere ...

• MASSIVE consequential reorganization early in 2015 ...
  – Great turmoil

• Announced and claims to have shipped UltraScale+
  – TSMC 16 nm
  – Full roadmap not disclosed as of Nov’15
  – Changed the terminology (...again...) ‘system logic cell’
Altera (Intel...)

• Intel acquiring Altera for nearly $17N ($USD)
  – At a VERY high price
    • This is ... puzzling ... Datacenter?

• Stumbling a bit last 2 years
  – Switch to 14 nm Intel fab has not gone smoothly

• ARM in Altera FPGAs? As an Intel company?

• Don’t have pricing yet on Stratix-10, but it looks very good.
Everybody else ...

- **MicroSemi**
  - Anti fuse, flash-based, some mixed signal

- **Lattice**

- **Startups**
  - Flex Logic got funded for some reason.
  - Tabula went down in a big ball of flame.
  - Achronix still stumbling around
FPGA SW

• Synopsys
  – Synplify Pro/Premier
    • Suite
  – Certify -> ProtoCompiler
    • Partitioning

• Mentor is doing, uhh, something
  – Acquired: (Aspey, FlexRAS), Certus
    • Precision

• Startups
  – Plunify
Let’s discuss some philosophy

• FPGAs and ASICs share a very similar design methodology:
  – Describe the design
    • RTL: Verilog VHDL, or some new fangled abstracted method such as OpenCL
  – Simulate
  – Verification
  – Place/route and/or fab
  – Debug

• If ASIC: you’d better get it correct the first time
• If FPGA, I suggest you not
  – So you are going to debug
Market conditions for debug tools ...

- Market is stagnant and might be nonexistent...
  - Good reasons

- ChipScope/ILA, SignalTap
  - Are essentially free leaving no market opportunity
  - Productivity enhancement is notoriously difficult to sell

- Performance issues ... Resource issues ...
FPGA Debug – The Basics

• Once configured, in internal workings of an FPGA are opaque
  – So to debug, we need methods to gain internal visibility

• In the ancient times, we routed signal to pins and hooked up a logic analyzer
  – If you are REALLY old, you used an oscilloscope.
  – Still a valid mythology

• Now, we embed the logic analyzer in the FPGA
  – This is invasive – its presence affects to logic we are trying to view.
  – It turns most, if not all, approaches are invasive

• Seems like this is a market opportunity ...
How are the data captured? How do we get the data?

- This is where debug products start to differ
  - Where are the data stored?
    - On chip
    - Off chip
  - How are the data retrieved?
    - JTAG
    - Custom Interface
    - High-speed serial Interface
Xilinx ChipScope Pro/ILA

• ILA Integrated as part of Vivado tools
  – ChipScope is Virtex-7 and prior

• Standard embedded logic analyzer
Altera SignalTap II

- Integrated as part of Quartus
- Standard embedded logic analyzer
Synopsys Identify

• Bridges2Silicon acquired by Synplicity (2002)
  – Synplicity acquired by Synopsys

• Standard embedded logic analyzer
  – Very good integration into design flow.
Synopsys ProtoLink

- Proprietary connector added to UUT
  - 40+ pins required

- Custom HW cabled to this connector
  - Plugged into PCIe

- Allows for deep trace lengths.
  - Generally used for uP debug
Certus (now from Mentor)

- Startup (Veridae) -> Tektronix -> Mentor

- Embedded Logic analyzer
  - External connection is JTAG

- Allows visibility for thousands of signals
  - Adds compression
  - Dramatically reduces cycle time
  - Multiple FPGAs
• Connects to high-speed serial interface
  – SFP, SATA et al.
• High performance to FPGA
• Large memory depth: 8GB

They are here!
Configuration Readback

- Xilinx (and soon Altera) allow readback of the internal FFs.
  - This can then be correlated with the nets and displayed

- If careful about what is read, this is non-invasive
Example: DNV7F4A
DN Readbacker – Key Features

• Noninvasive real time readback of FPGA register state
  – 100% coverage of FPGA registers
  – 1 complete readback/second (depending on FPGA size)
  – Running clock or single step
  – Works on all DINI Group Xilinx-based FPGA boards:
    • Xilinx UltraScale, Virtex-7/Kintex-7, Virtex-6
    • Stratix-10 when available
  – Output to standard .vcd file and displayed in GTKWave
  – No RTL support required
  – Noninvasive observation of all FPGA registers
  – Not necessary to redo synthesis or place/route
Disadvantages

• Unless clock stopped you don’t get a frozen snapshot

• Slow: ~1Hz

• No understanding of clock domains