Enabling Digital Mixed-Signal Verification of Loading Effects in Power Regulation using SystemVerilog User-Defined Nettype

Alvaro Caicedo, Sebastian Fritz

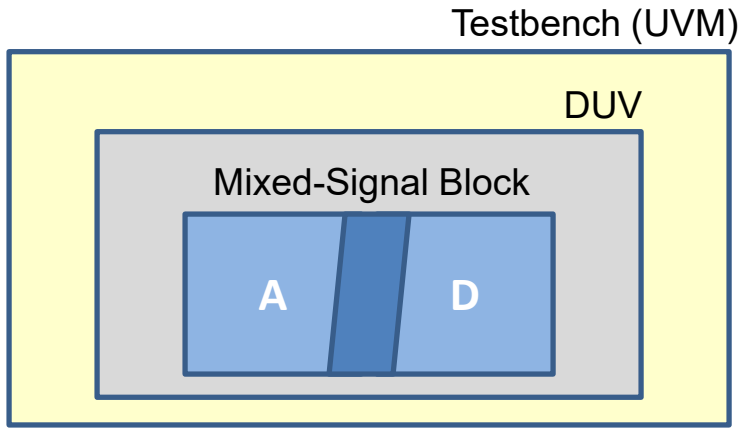
Agenda

- Verification Scope and Motivation
- Challenges in Real-Number (RNM) Modeling of Loading Effects
- SV-UDN for Electrical Equivalence: *EEnet*
  - Benefits of Modelling Loading Effects with *EEnet*
- Practical Power Regulation Circuit
  - Building Blocks modeled with *EEnet*
- Verification of *EEnet* models
- Mixed-Signal UVM Testbench for IP/SoC
- Summary and Conclusion

Verification Scope

- Power management system verification
  - **Robustness against load jumps caused by system activity**
  - Start up sequences
  - Low-power transitions
  - Interdependencies with other infrastructure blocks
  - Supply ramps

- Requirements of the verification environment
  - **Mixed-signal simulation support**
  - Affordable simulation runtimes
  - Reusable across several hierarchies



Motivation

- General Objective

1. Enable early proof of concept of power circuits in mixed-signal simulation

2. Check loading effects caused by system activity, off-chip components and the interaction of multiple driver blocks

3. Simulate voltage regulation of power management systems at IP and device level in big scale designs

Analog Mixed-Signal (AMS) simulations are very accurate but very slow in big designs.

We want the performance benefits of Digital Mixed-Signal (DMS) simulations! [1]

Challenges in Real-Number Modeling of Loading Effects

- DMS requires Real-Number (RNM) models.
  - Verilog-AMS *wreal* type is **scalar**. Wires modeled as either voltage or current. [2]
  - Voltage, current and impedance in the same net are needed to model loading effects. This suggests the need of a structured net type.
  - VHDL RNM supports structured net types but has limitations with coercion of wire to *wreal* and the connectivity from real to electrical. [3]
- Therefore, simulation of loading effects was normally left to expensive AMS simulations.
- As an alternative, SystemVerilog (SV) IEEE 1800-2012 introduced: [4]
  - User-Defined Nettype (UDN)
  - Explicit interconnects

SV-UDN for Electrical Equivalence: *EEnet* [5] [6]

What is *EEnet*?

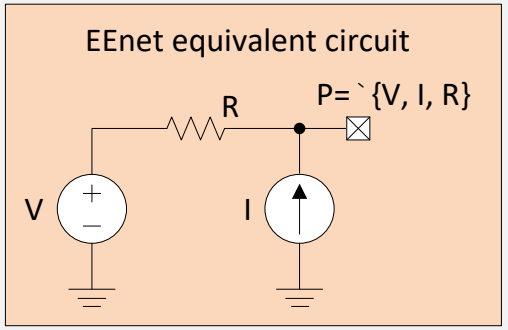
- Cadence implementation of SV-UDN for electrical equivalent modeling
- Combines voltage, current and resistive effects of all drivers

```
package EE_pkg;

// UDT struct to define voltage, current and resistance
typedef struct {
  real V, I, R;
} EEstruct;

// Usage as UDN
EEnet P;
real v1, i1, r1;
real v2, i2, r2;
real vp;

assign P = '{v1,i1,r1};   // Driver 1 for node P
assign P = '{v2,i2,r2};   // Driver 2 for node P
assign vp = P.V;          // Get resolved node voltage
```

UDT

UDN

UDR



UDN **_EEnet:_** User-Defined Nettype (UDN)

Associates nets of type ***EEstruct*** with resolution function ***res_EE***

=

UDT ***EEstruct:*** User-Defined Type (UDT)

Three real fields: voltage (V), current (I) and series resistance (R)

+

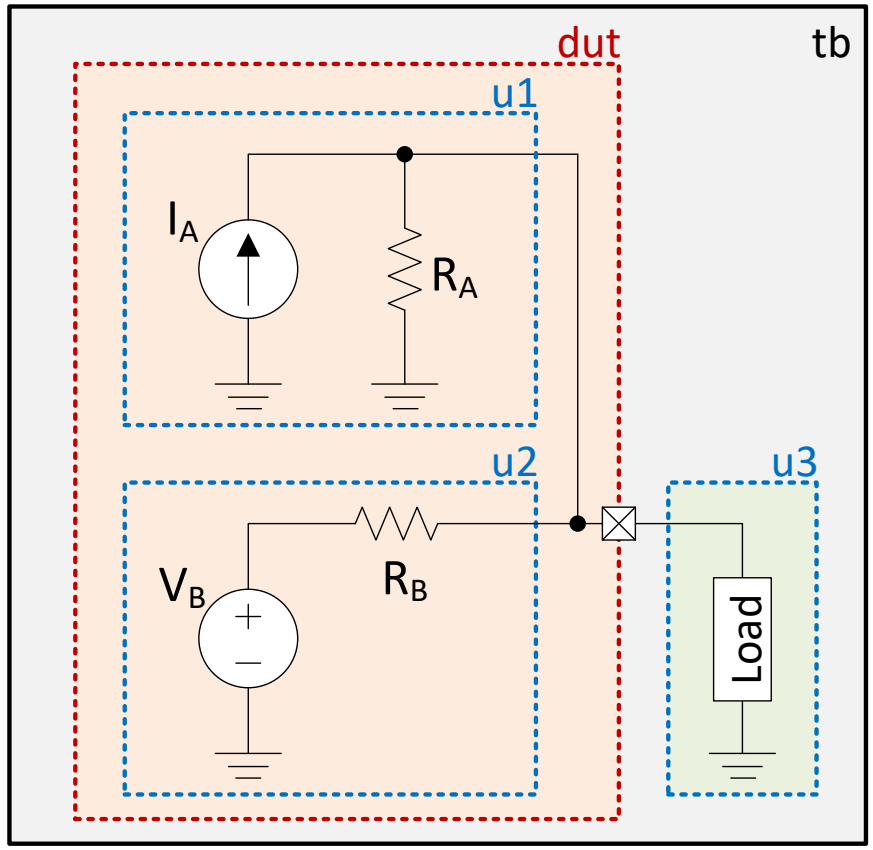
UDR ***res_EE:*** User-Defined Resolution (UDR) Function

Resolution of V, I and R in multiple driver following Kirchhoff's law

Benefits of Modelling Loading Effects with *EEnet*

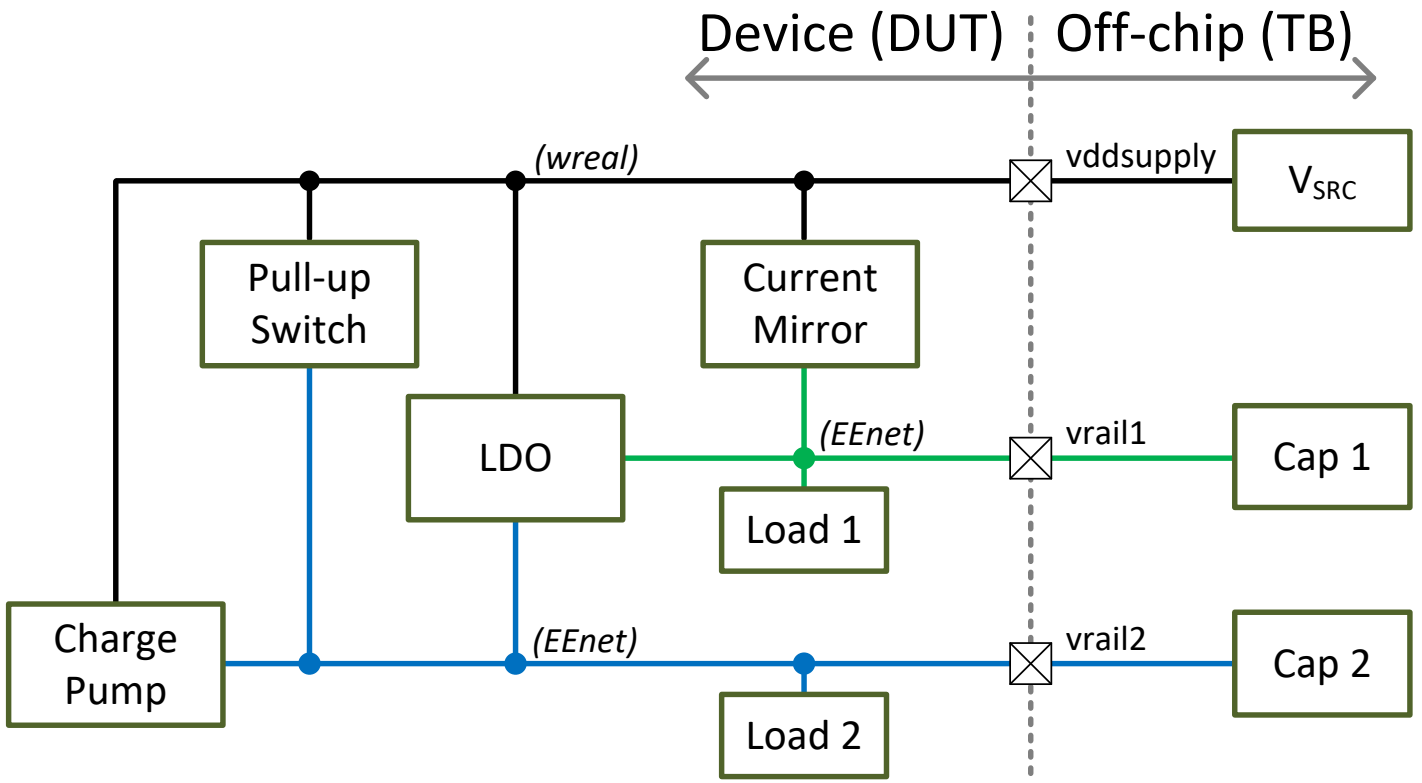
- Enables hierarchical modeling
  - No need to put all drivers and loads into a single behavioral model.
  - Nets are automatically coerced.
- Drivers and loads may differ in nature
  - Voltage and current sources.
  - Active and passive loads.
  - Passive load can be resistive, capacitive or inductive.
  - Use discrete integration for L/C models.

Sample circuit requiring load modeling

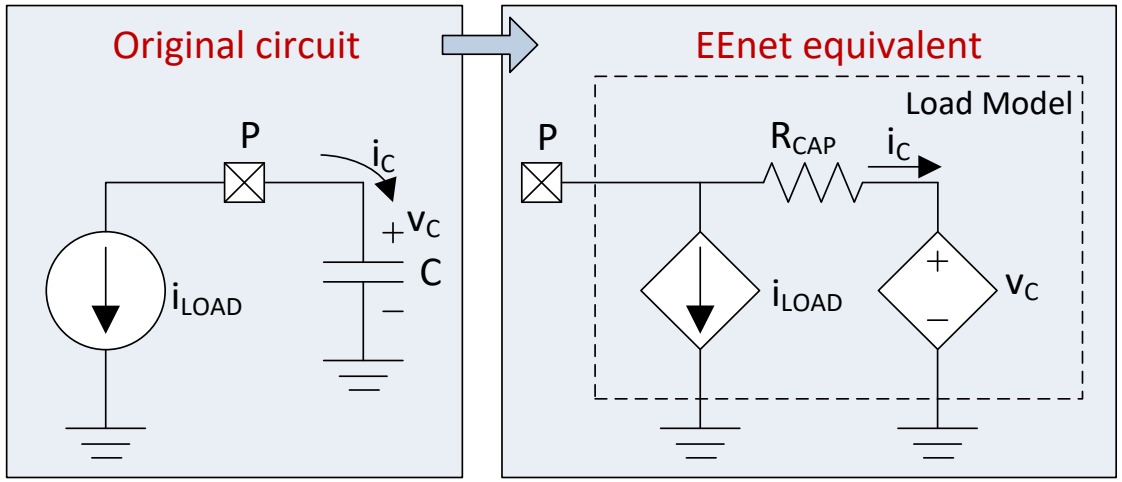


Practical Power Regulation Circuit

- Two regulated voltage rails
- *EEnet* Loads:
  - Off-chip capacitors
  - System load currents
- *EEnet* Drivers:
  - Pull-up switch
  - Current mirror
  - Charge pump
  - LDO
- *wreal* can still be used for scalar nets and drivers like the supply source



EEnet Models: Capacitor + Load Current



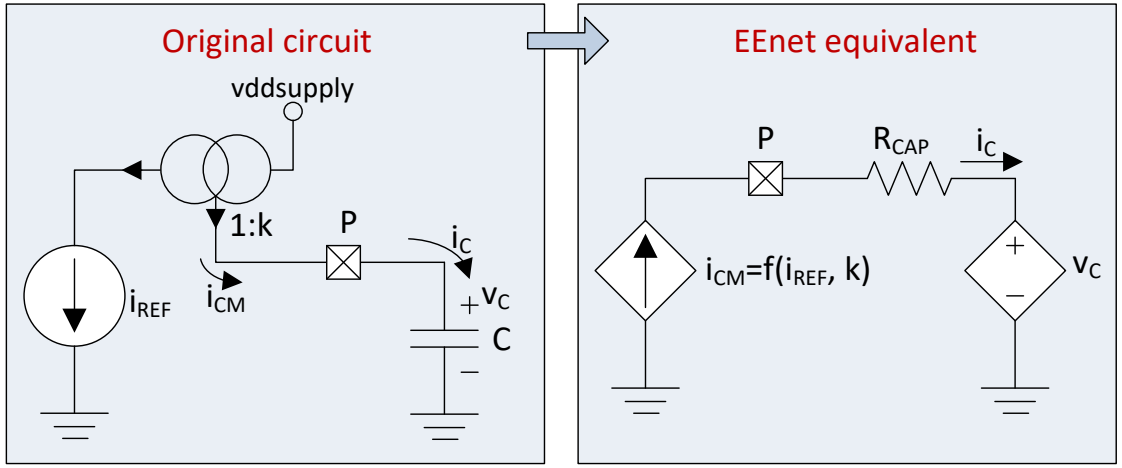
Capacitor (passive load)

- Big off-chip capacitor to be loaded with current from the system.
- To be placed at the IP/SoC TB.
- Discrete integration using averaging re-sampler [5]

Load current (active load)

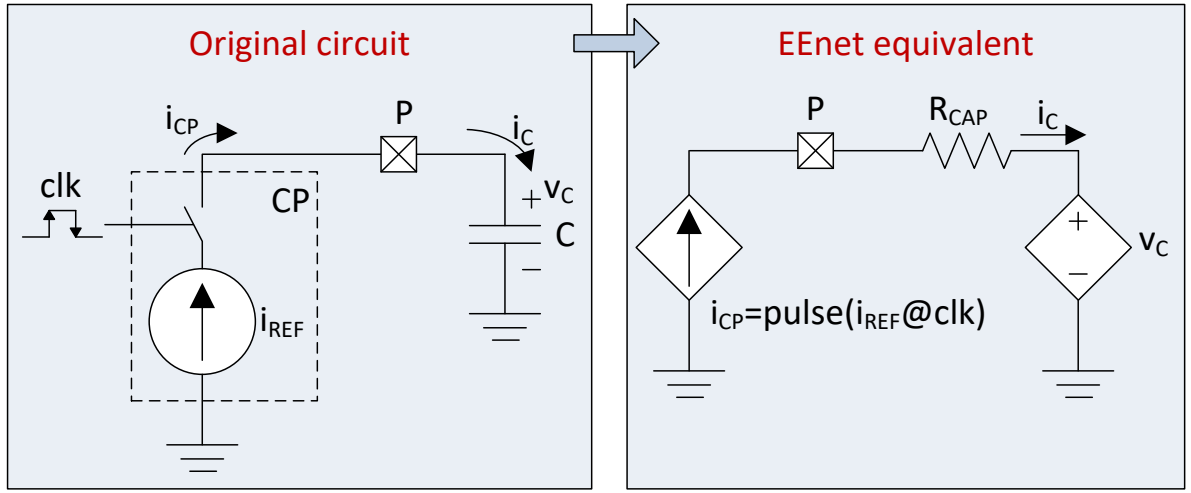
- Sink current represents current consumption of components supplied by the rail.
- Controlled by the IP/SOC testbench.

EEnet Models: Current Mirror



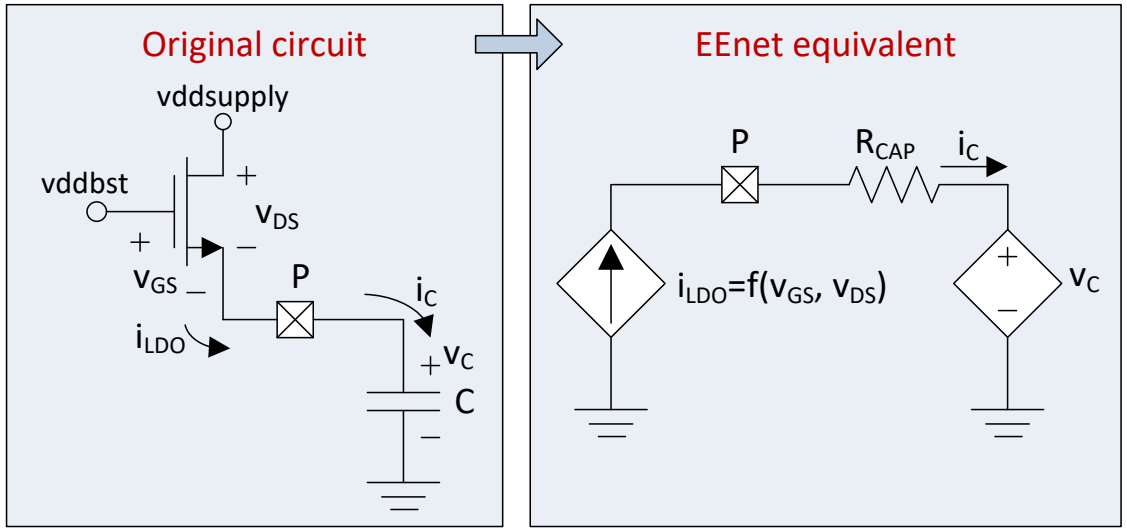
- Current source to load a big capacitance up to supply voltage.
- Simple model is linear in the whole voltage/current range.
- Saturation and nonlinearities can be added.

EEnet Models: Charge Pump



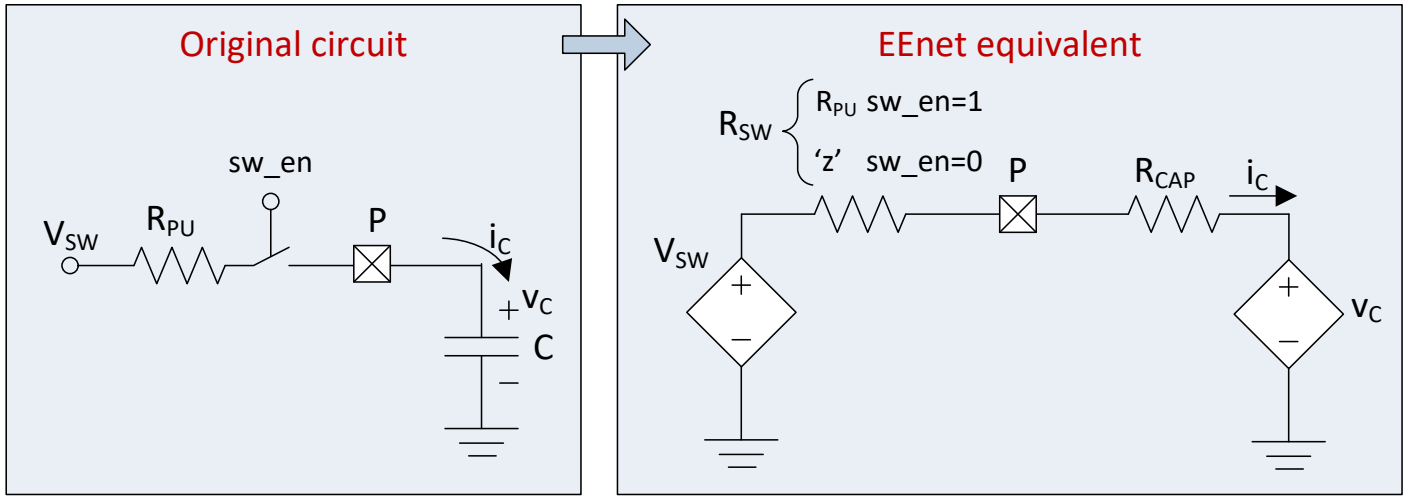
- Current source to load a big capacitance beyond the supply voltage.
- Generates short current pulses after every clock edge.

EEnet Models: LDO



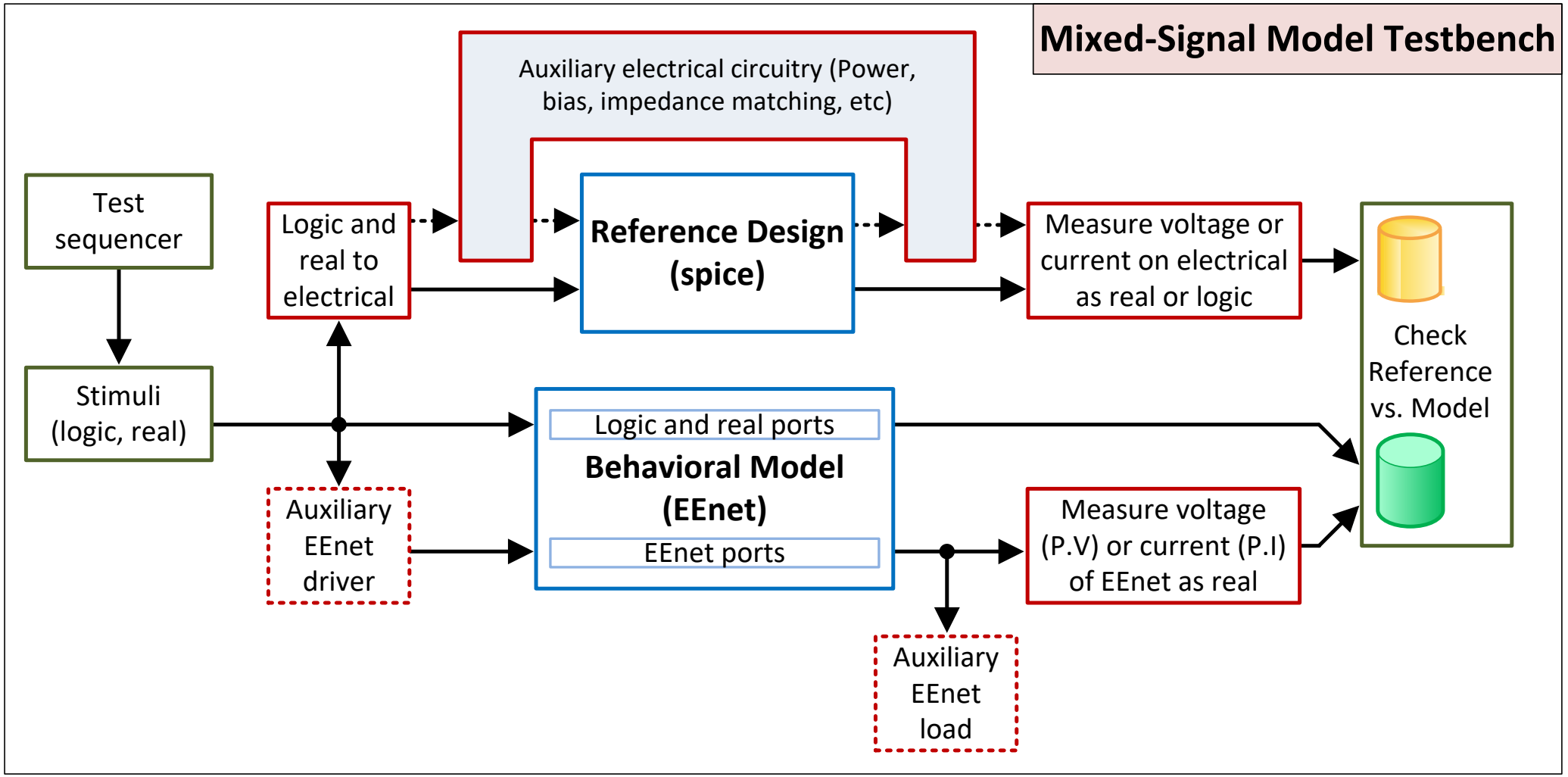
- DC linear voltage regulator.
- Modeled as a current source with $I_{LDO} = f(V_{GS}, V_{DS})$
  - Feedback between output voltage and output current might create unlimited recurrence in UDR. Broken in model by using tolerances.
- Using VAMS instance with table model. Equations would be faster.

EEnet Models: Pull-up Switch with Diode



- Pull-up resistor for fast charge of big capacitance up to supply level.
- Modeled as voltage source with series resistor controlled by a switch enable.

Verification of *EEnet* Models



Mixed-Signal UVM Testbench for IP/SoC

- Verification environment
  - Constrained random verification in SystemVerilog UVM
  - Fast sign-off of the design circuit via RTL regression runs
  - Reusable in device context
  - Low-power simulation support
- Multiple design configurations
  - DMS, AMS and AMS co-simulation for analog
  - RTL and gate-level netlists for digital
- Verification components need to drive **real** signals to:
  - control supply voltages and rail loads
  - monitor voltage rails, reference voltages and reference currents
  - configure parameters of *EEnet* load models
- Testbench randomization
  - Supply voltages
  - Load jump scenarios
  - System power states
  - System events and clocks

Summary

- Simulation of loading effects usually done in AMS due to limitations in real-number modeling with scalar types.
- Introduction of SystemVerilog UDN as electrical equivalent overcomes limitations of scalar VAMS *wreal* and allows to run loading effects in DMS.
- Cadence's *EEnet* SV UDN with electrical equivalency proven to be suitable to model loading effects.
- Presented several *EEnet* implementations of generic building blocks commonly used in power regulation.
- Presented model verification approach for *EEnet* models and usage in constrained random verification environments.

Conclusion

- ✓ Successfully proven the effectivity of the SV-UDN *EEnet* to model loading effects and interaction of multiple drivers in complex nodes for power regulation.
- ✓ Methodology improved quality of the product by extending functional coverage with loading scenarios in DMS and facilitating proof of concepts in an early stage.
- ✓ Methodology reduced overall project development time by leveraging AMS effort into the DMS domain. AMS still used for a selective number of tests to check over corners.

References

[1] R. Sanborn, R. Mitra, Z. Fan, "*Best Practices for Verifying Mixed-Signal Systems*", p. 43-52, Cadence Application Notes, USA and Canada, 2018.

[2] Accellera System Initiative, "*Verilog-AMS Language Reference Manual v2.4*", USA, 2014.

[3] A. Baguenier, "*Best Practices in Mixed-Signal Modeling and Verification*", p. 12, CDNLive Silicon Valley, USA, 2018.

[4] IEEE Computer Society, "*IEEE 1800-2012 - IEEE Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language*", USA, 2013.

[5] Cadence Design Systems, *"Real Modeling with SystemVerilog"*, Training, 2016.

[6] Cadence Design Systems, *"Using EEnet to perform Electrical Equivalent Modeling in SystemVerilog"*, Rapid Adoption Kits, 2017.

Questions