### Motivation
- Simulators are used for functional/Power verification
- Complex designs on simulators are of slow process
- Power and Performance benchmarks are not efficient to run on simulators due to their nature of complexity and longer runs
- Emulation is a proven flow for modern verification, and it helps significantly to reduce turnaround in Power and Performance coverage closure

### Power Analysis
- Power validation requires real applications to run for power calculation which takes significantly longer than verification tests
- Emulation helps to Power closure with significant gain in verification timelines
- Power tools are easily pluggable with Emulation/Hardware-Acceleration platforms to replace simulators with very low error margin
- By virtue of Emulation synthesis step, one has to make sure of replacing all RTL/TB memories to synthesizable models

### Methodology
- Accelera Co-emulation methods are adopted to migrate existing testbench to Emulators
- Transactor level modelling used to split the testbench into HDL and HVL, in which HDL contained DUT
- System verilog task and functions are used to transfer data between HDL and HVL

### Methodology Flow
- After compilation of HDL and HVL, real applications are executed to dump Power (SAIF/FSDB) and Performance data (Monitors/Counters)
- Emulators dump raw toggle data from Hardware, so there is an intermediate step to convert it into SAIF/FSDB which goes directly into power tools

### Challenges and Solution
- To understand the correct boundary of simulator testbench to split into HDL and HVL, Accelera standard based co-emulation technique is adopted
- To verify testbench change with full regression suites and debugs around HDL-HVL boundary, Emulator debug features are used
- To optimize Emulation modelling, EDA tools are tuned based on ML NPU design complexities
- Power benchmarks involved a validation of mismatch in signal toggles between simulation and emulation, switching off emulator logic optimization engine
- Performance benchmarks run for billions of cycles and occupies the emulator hardware for days, hardware stability is taken care by EDA
- To transfer raw emulator toggle data directly to Power tool, work is ongoing i.e. Online streaming mode

### Results and Next steps
- First milestone was of 330x runtime gain in emulation over simulation runtime
- Additional 2x gain (total 600-800x) was attained by optimizing HDL-HVL boundary communication (memory read/write calls are clubbed and few redundant calls are removed)
- Largest Power vector on simulator takes several days which came down in few hours on emulator
- Performance benchmarking was a challenge on simulator due to long runtime for billions of cycles, which was easily overcome on emulation
- Next step is:
  - To unify testbench to avoid maintenance of separate testbenches for simulation and emulation
  - To ensure scalability of existing efforts in future projects