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Early Chip-Level Power Estimation Using Digital Mixed-Signal Simulations

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Pre-Silicon Power Estimation Overview

- Part of verification process, required to ensure that power consumption does not exceed power budget
  - May lead to architecture/design changes if power specification is not met
- Common sign-off criteria in mixed-signal designs:
  - Analog domain: chip-level analog mixed-signal (AMS) simulation
    Very long simulations (days or weeks) at later phase of a project (when whole design is mature); limit turn-around time in case power violations are found
  - Digital domain: gate-level simulation (GLS) data processed by power estimation tools
    Possible only after place-and-route (PnR) but faster results than analog

Proposed Method

- Not a replacement for AMS simulations
  - The method is able to provide preliminary power estimation results, so that power violations can be detected before time-consuming AMS simulations start
- Based on digital mixed-signal (DMS) simulations
  - Chip-level simulations with analog behavioral models (instead of design schematics)
  - Analog models capable of inferring their own power states during simulation
  - Model power states mapped to current consumption (specified or simulated)
  - Overall current consumption consolidated per power domain/rail
  - Faster simulations (minutes or hours) able to run extensive/random scenarios

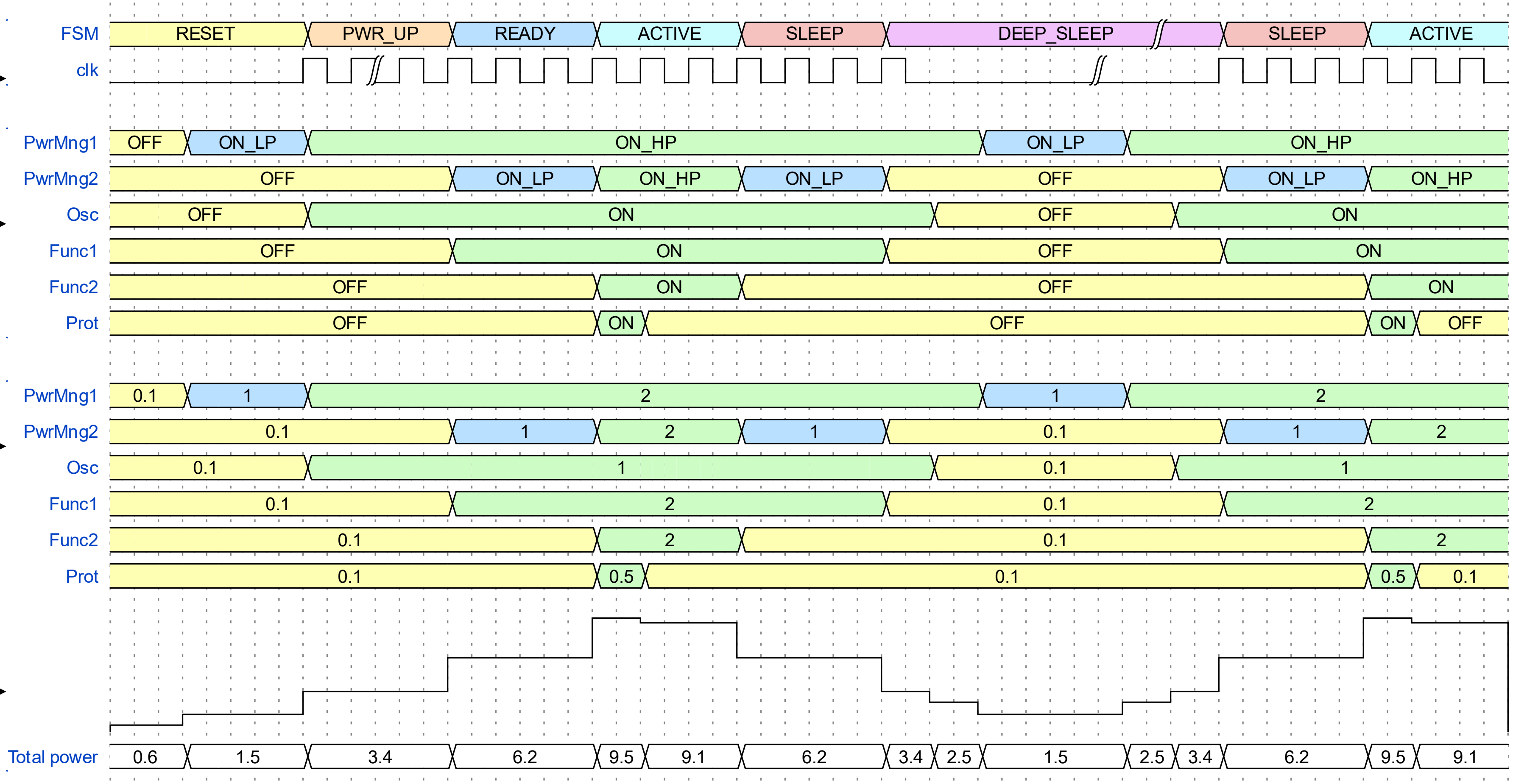
Method Example

Digital signals for reference (FSM state and clock)

Power states of individual analog models

Analog power consumption per model (arbitrary values)

Total analog power consumption (arbitrary values)



Power Mode Calculation

- Analog behavioral models infer their own current power state
  - Solely based on models input signals (combinational or sequential)
  - No information of chip’s current operation mode required
- Power states of all models “published” via System Verilog virtual interfaces

```
blk_if pwr_if();            // Interface to “publish” the current power mode

initial begin               // Make interface accessible to other components
  uvm_config_db #(virtual interface blk_if)::set(null,"*",blk_vif,pwr_if);
end

always_comb begin           // Definition of power modes
  if      (supply_ok & ref_ok & en & !en_dly) pwr_if.pwr_state = ON_LP; // low-power
  else if (supply_ok & ref_ok & en &  en_dly) pwr_if.pwr_state = ON_HP; // high-power
  else                                        pwr_if.pwr_state = OFF;   // disabled
end
```

Power states coded directly in the behavioral model file or in a standalone file connected to the model via System Verilog bind construct.

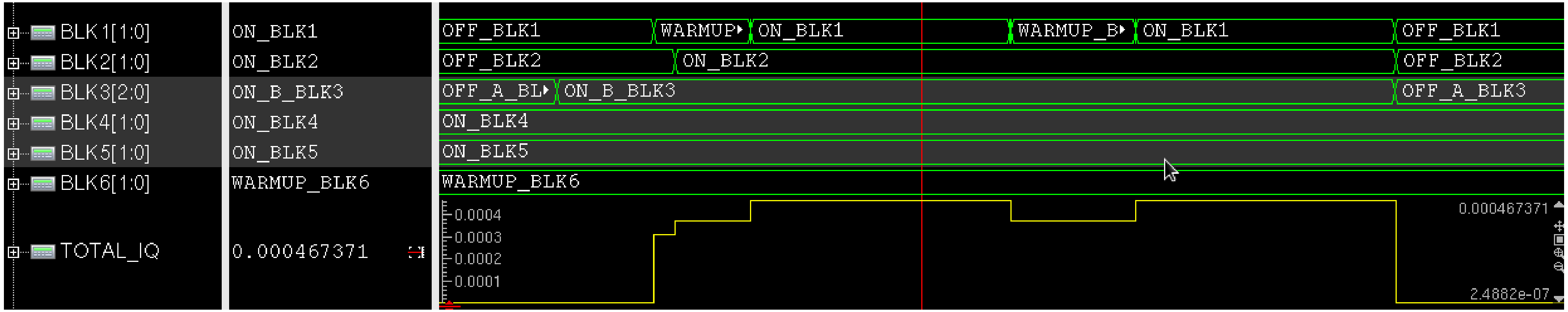
Power Mode Mapped to Current

- The DMS top-level testbench receives the power states of all models through their respective virtual interfaces and map them to quiescent current (Iq)
    - It is possible to use different Iq values, such as specified value, as well as corner figures obtained from block-level analog simulation, e.g., FF35C, FF75C

```
forever begin
  @(blk_vif.pwr_state);
  blk_iq =                          // FF @ 35C (sim)             // FF @ 75C (sim)             // typical (spec)
    (blk_vif.pwr_state == OFF   ) ?  ff35 ? pwr_pkg::FF35_OFF   :  ff75 ? pwr_pkg::FF35_OFF   : pwr_pkg::TYPOFF   :
    (blk_vif.pwr_state == ON_LP) ?  ff35 ? pwr_pkg::FF35_ONLP :  ff75 ? pwr_pkg::FF35_ONLP : pwr_pkg::TYPONLP :
    (blk_vif.pwr_state == ON_HP) ?  ff35 ? pwr_pkg::FF35_ONHP :  ff75 ? pwr_pkg::FF35_ONHP : pwr_pkg::TYPONHP :
                                    1e6; // large value to flag error (default)
end
```

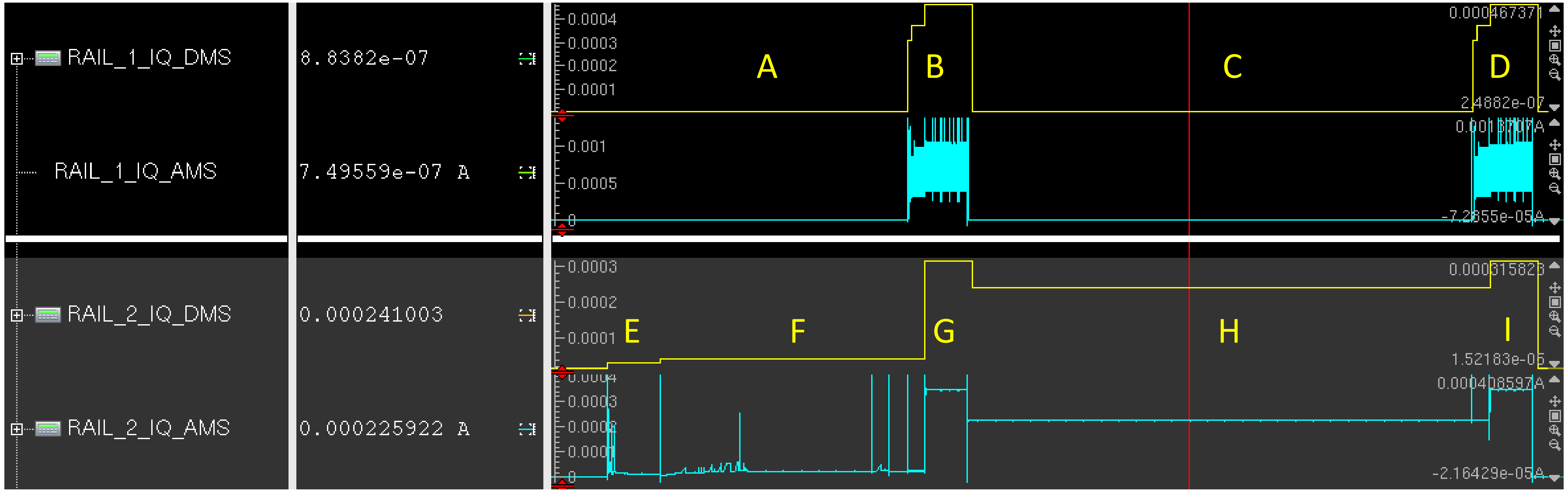
Results

- Power states of 6 models (BLK1 to BLK6) as well as consolidated Iq
  - If required, power states can be refined to include transient response
- Iq value and overall profile can help identify situations where the design functionality might be correct, but a given block is mistakenly enabled, therefore consuming excessive power



Results (cont.)

- Proposed method (yellow curves) compared with full schematic analog simulation (cyan curves) for two different rails (RAIL_1 and RAIL_2)
  - Comparison between both simulations (DMS and AMS) in the next slide



RAIL_1_IQ_DMS 8.8382e-07

RAIL_1_IQ_AMS 7.49559e-07 A

RAIL_2_IQ_DMS 0.000241003

RAIL_2_IQ_AMS 0.000225922 A

Results (cont.)

- Comparison of Iq estimation of DMS and AMS simulations
- Good correlation of power gain (in dB) between regions

	Rail 1				**Rail 2**				
Average Iq (µA)	***A***	***B***	***C***	***D***	***E***	***F***	***G***	***H***	***I***
DMS	0.25	441	0.84	414	29.7	41.1	315	24.1	315
AMS	0.29	344	0.75	341	19.3	27.1	349	22.6	349
Gain (dB)		$A \rightarrow B$	$B \rightarrow C$	$C \rightarrow D$		$E \rightarrow F$	$F \rightarrow G$	$G \rightarrow H$	$H \rightarrow I$
DMS		64.4	-53.9	53.9		2.8	17.7	-2.3	2.3
AMS		61.5	-53.2	53.2		2.9	22.2	-3.8	3.8

Conclusions

- The proposed method helps to anticipate power violations and avoid late issues demanding re-designs, which could impact the project schedule
  - It has been successfully used in circuits developed for consumer applications, where time cycles can be as short as 6 months
  - It also allows quickly exploration of longer or random scenarios, which would not be practical in full-schematic AMS simulation
- This method also allows the usage of assertions to self-check power intent
- AMS simulations are still executed for sign-off but with higher confidence that power violation bugs will not be found

Questions

Thank you