Design & Verify Virtual Platform with reusable TLM 2.0

By Ankush Kumar

3D IP Semiconductors Pvt. Ltd.

3D-IP Semiconductors
...next generation IPs

accellera SYSTEMS INITIATIVE™

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

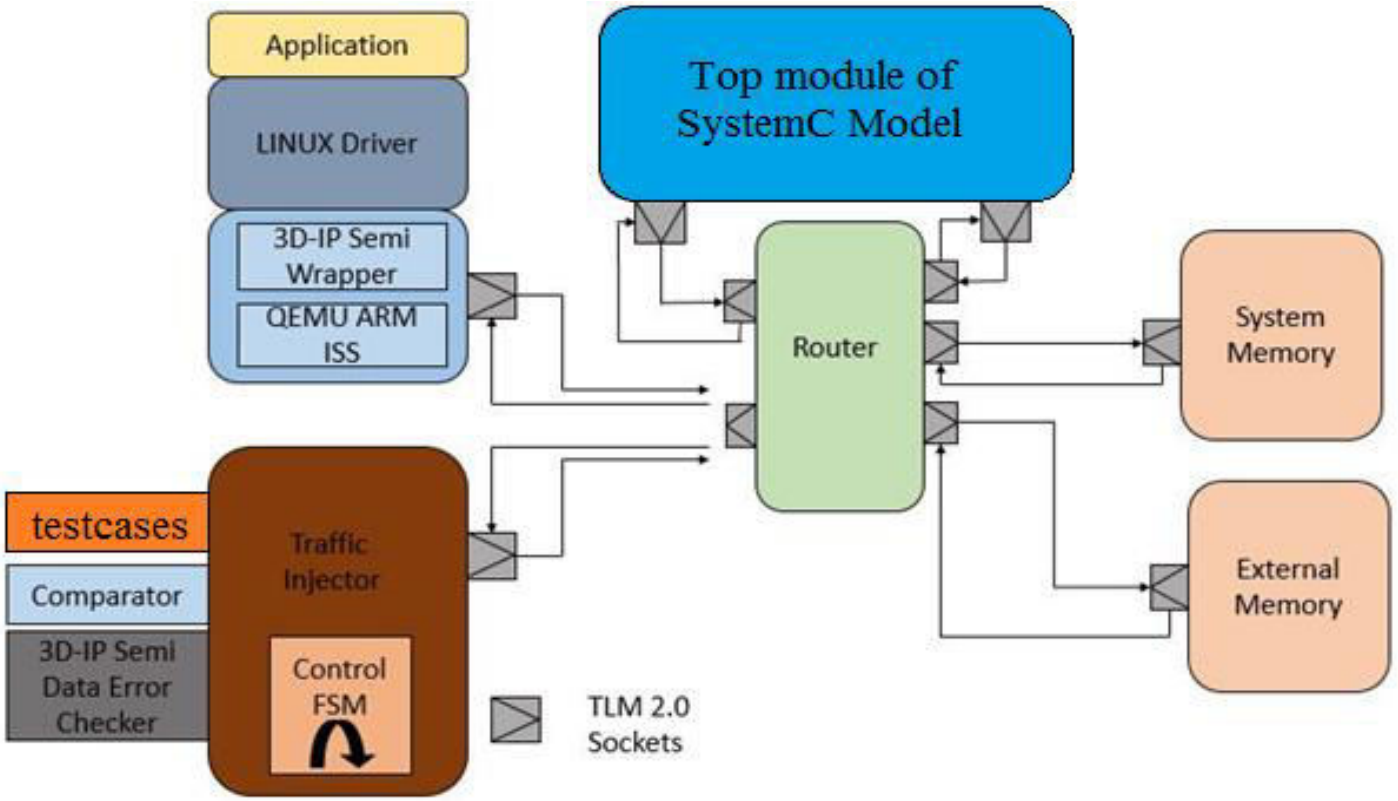
TOPICS

- Introduction
- Architecture & Methodology
  - Linux driver based verification
  - Unit module based verification
- Benefits
- Use case
- Conclusion & Future Work
- Questions

INTRODUCTION

- SystemC & TLM 2.0 in use for prototyping & at transaction level modelling
- Utilize SystemC/TLM 2.0 sockets for verification
- Easy testcase development
- Open source tools for development and automation

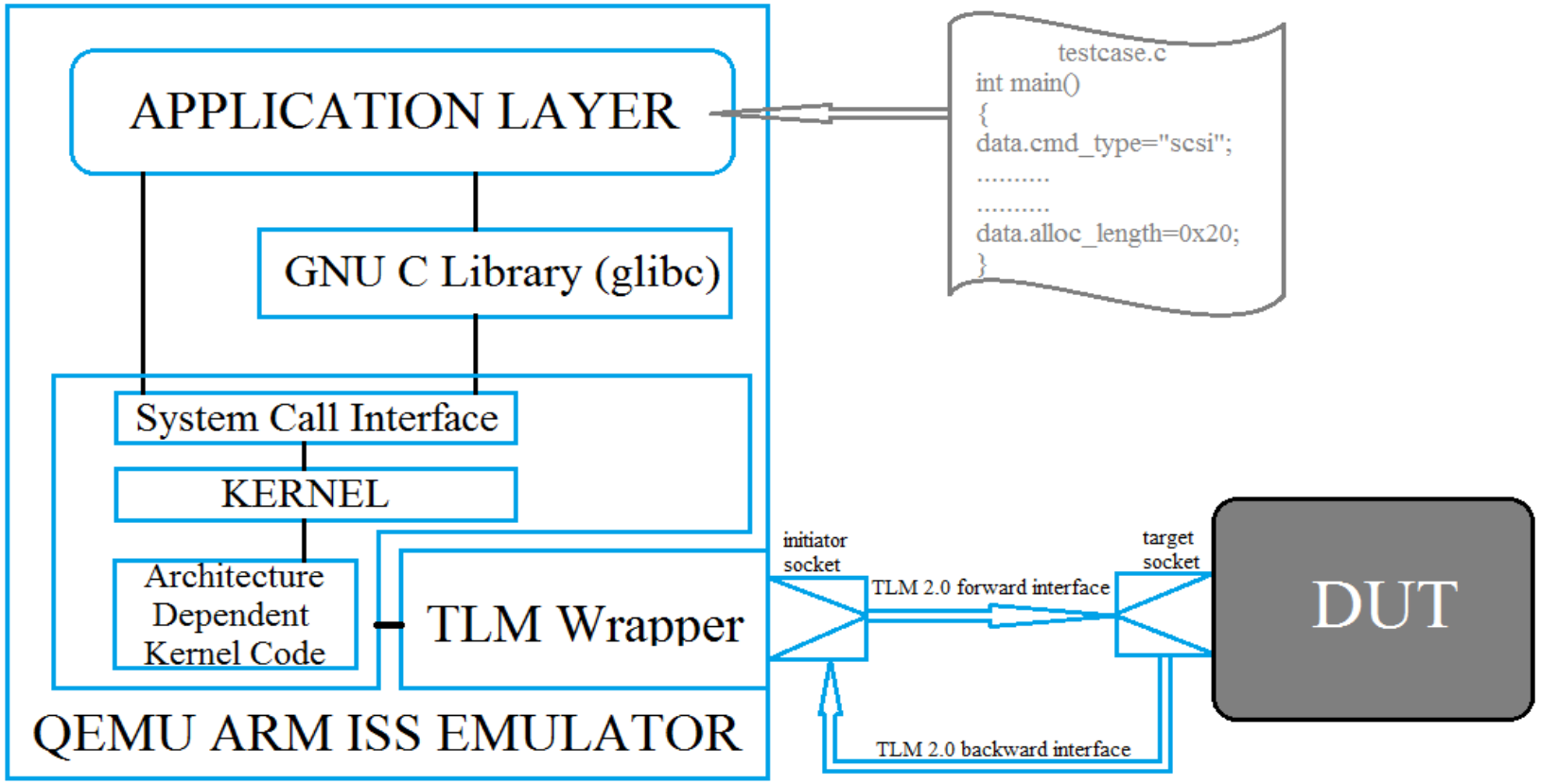
ARCHITECTURE



ARCHITECTURE

- Two verification methods
  - Linux Driver based verification
    - Embedded based s/w application models
    - Component used are free open sources
    - Performs hardware virtualization
  - Traffic injector
    - Unit Module testing
    - TLM 2.0 blocking transport call for read/write
    - several simulation cycles could elapse

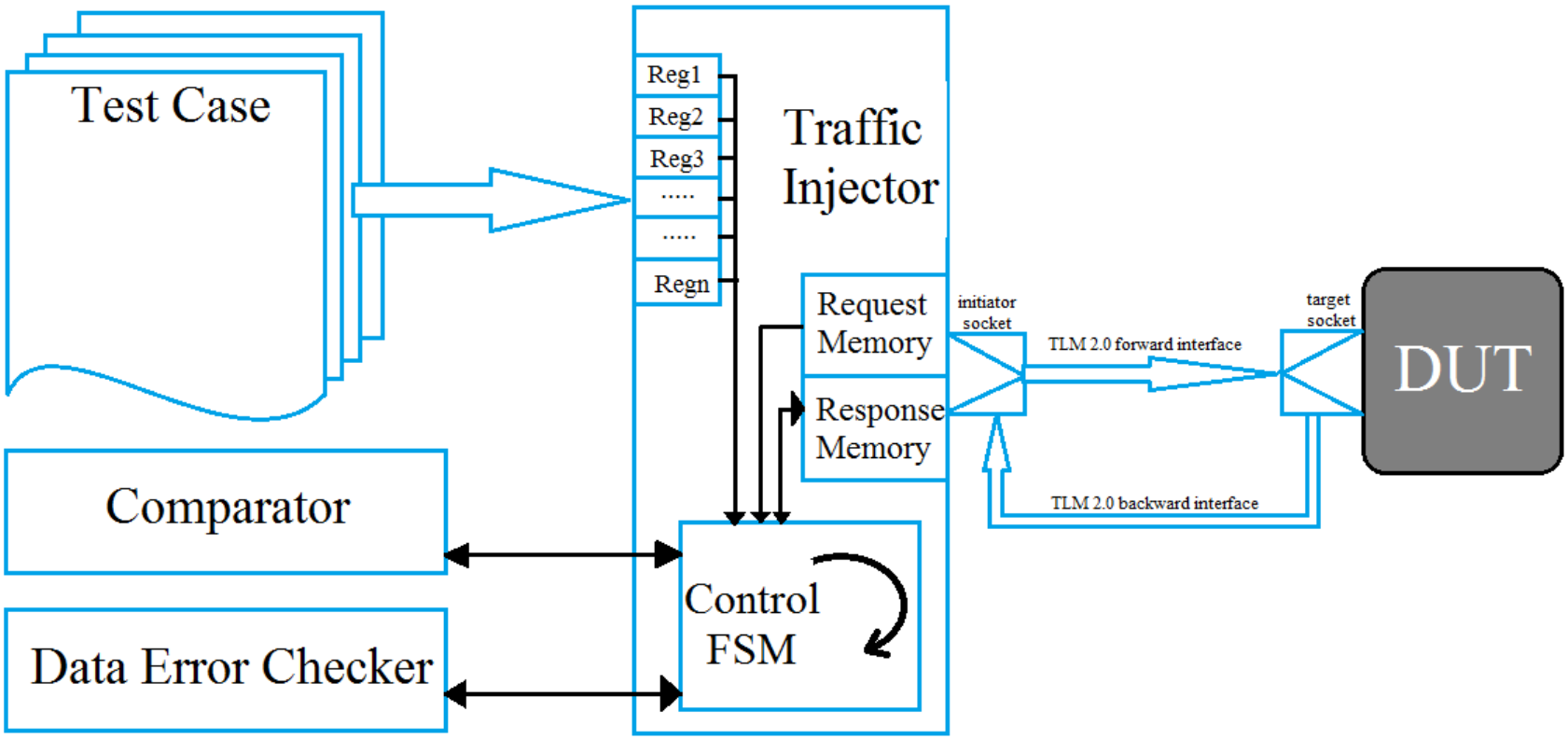
Linux Driver Based Verification



Linux Driver Based Verification

- Methodology
  - Employs : Linux kernel (core CPU) image built over QEMU emulator.
  - Root system file image provided with testcase executable
  - A TLM wrapper provides communication b/w Linux Kernel & SystemC IP model through TLM 2.0 interface.
  - Driver writes the testcases through TLM 2.0 initiator socket.

Unit Module Based Verification



Unit Module Based Verification

- Methodology
  - TLM 2.0 initiator socket bound to the verification component
  - TLM 2.0 target socket bound to the model for testing.
  - Read/Write the test cases onto the model through TLM 2.0 blocking transport calls.
  - Next transaction will takes place only after the completion of previous call.
  - Several simulation cycles could elapse by blocking transport call.

Benefits

- Less time will be used for integrating verification component with modules.
- Easy to develop the test cases.
  - Not much programming skills are required.
  - Only good understanding of protocol is required.
- Same test case at the module level can be reused with minor modifications.
- Only minor changes for verifying different protocols.
- Open source tools for development and automation.

Benefits

- Verified a Virtual Platform for an advance Memory Controller (*Universal Flash Storage (UFS) 2.0 JEDEC Standard)*.
- Same methodology can be utilized for other Controllers such as embedded Multimedia Controller (eMMC), Solid State Drives (SSD), etc.
- Allows the SOC Verification engineer to control the verification through the tools and languages familiar to him and saves time & effort on ramping up on a new module and language.

Future Work

- Testcases for both environment be unified to reduce writing effort and port the IP level testcases to system level environment.
- Enhance environment so that it can be used right from the SystemC modelling level to the actual design in HDL and further into the system integration domain.

Any Questions ?