DVCon India 2025: Selected Posters List

P1:782 - Beyond Traditional Testing: Integrating DV and DFT for Zero-Defect Goals *Jyothy Melaedavattil Jaganathan, Ann Keffer and Gaurav Goel,* Siemens
P2:1418 - AI-Enabled Formal Verification Flow: From Spec to Sign-off *Rinu Mathew,* SmartSoC Solutions Pvt Ltd.
P3:1542 - Adaptive Multi-Modal Sensor Fusion Accelerator with Real-Time On-Device Learning for Dynamic Environments *Ankush Kumar Jaiswal, Sanskruti Gole and Mayank Bhende,* VIT, Chennai
P4:1552 - Cognitive smoke testing *Nikhil Singla, Rohit Jindal, Pandithurai Sangaiyah, Debarati Banerjee and Krish Desai,* Google
P5:1947 - Truth Beneath the Trace: Formal Verification Revealing *Chepuri Venkatesh, Mahesh Shinde, Satish Singh and Nitin Neralkar,* Qualcomm
P6:2493 - PSS beyond reuse: Streamlining the DV effort for a low power multi-core SOC *Vivek Gopalkrishna, Nitish Swamy, Ponnambalam Lakshmanan, Santoshkumar Pathak and Sonal Patil,* Analog Devices
P7:3171 - Next-Generation CDC and RDC Closure: An AI/ML-Driven Approach for Automated and Validated Constraint Generation *Ravi Pathak and Abdul Moyeen,* Siemens
P8:3446 - Securing and Optimizing Data Flow by Validating Die Level Interconnect Stress with AES XTS 256-bit Encryption and Ring Interconnect Analysis on edge client SoCs *Gowri Shankar Somanjeri, Ashutosh Mishra, Pankaj Sharma, Naveen Urs T R, Aravind Krishnan and Srishti Singh Chauhan,* Intel
P9:3591 - Remote and Probeless Debug Methodology for Data Center Silicon Debugs *Mamatha Kallimatada, Sasidhar Sunkari and David Kapchit,* Google
P10:3645 - Overcoming the roadblocks in Display Port Automotive Extensions verification *Thenmozhy Kaliyamurthy, Meenakshy Ramachandran, Nusrat Ali and Pankaj Sharma,* Synopsys
P11:3773 - Bridging RISC-V Core Verification and PSS: A Portable-Stimulus Stress-Testing Approach *Darshan Shivsingh Patel and Swapnil Sindhur,* Vayavya Labs
P12:3945 - Comprehensive Formal Verification Methods for Data Sensitive ECC Design Fault Verification Closure *Arslan Naval and Sachin Kumar,* AMD
P13:4118 - Novel customized algorithms and verification checklist to improve the process of Register Verification in UVM *Sougata Bhattacharjee and Akshaya Jain,* Samsung Semiconductor India Research (SSIR)

P14: 4790 - TiDe : Timing diagram to Design verification model *Ramya B T,* Samsung Semiconductor India Research (SSIR)
P15: 4873 - SmartLint Booster: Automation of UVM Testbench Linting with AMIQ Verissimo *Gustavo Guzman Rosales, Gurudatt B M, Richa Gupta and Kanai Ghosh, NXP*
P16: 4891 - Advancing Early Enablement, Validation, and Signoff of Manageability IP for Seamless dGPU-Server Paring *Shyam Kumar Choudhary, Paras Agarwal and Madhusoodanan Pudhucherry, Intel*
P17: 5053 - Chain of Responsibility Design Pattern for scalable UVM drivers *Chandana Nallangi and Suresh Gandhi Subramaniam, Intel*
P18: 5976 - Novel and optimised solution to accelerate gate level simulation for complex SOC *Viral Vyas, Ravikiran Bondugula, Pradeep Kumar Sahoo, Sunil Shrirangrao Kashide and Garima Srivastava,* Samsung Semiconductor India Research (SSIR)
P19:6547 - Novel Use of Symbolic Map Based Input Driving for Synchronization Block Verification Using Formal Methods *Vikas Vikram Singh, Sanjana Jain, Patnala Naga Sai and Ipshita Tripathi,* Qualcomm
P20:6976 - An Ideal FuSa Verification Solution! *Prashantkumar Ravindra,* Analog Devices
P21:7003 – Precision Unveiled: Formal Methods in Dot Product *Suraj Kamble, Mohit Choradia and Vichal Verma,* Microsoft
P22:7050 - Emergency Band *Liya Jos, Henna Mariya Sathish, Sreehari Siju, Prashob Francis and Kalidasan P,* Sahrdaya College Of Engineering And Technology
P23:7357 - STEP (Smart Test Execution Prioritizer) System *Biju K and Aryan Kashyp,* NXP
P24:9184 - Test Smarter, Not Harder: GNN-Powered Automation for Post-Silicon Validation *Venkata Ajay Kolla,* Intel
P25:9660 - Analog feature modeling for memory devices in digital simulation *Shyam Sharma, Yoshiharu Kato and Tiffany Tamaddoni,* Cadence