DVCon India 2025: Selected Papers List

Paper Session 1A: Design Verification - SV & UVM
1A1: UVM based Generic Interrupt Service Routine (gISR) Ritesh Mehta & Nakul Sharma | *Google*
1A2: Accelerating Debug with Experience-Driven Insights: A Tool-Based Approach for IP and SoC-Level Verification Maitreyi Vemulapalli & Vinay Datta | *Marvell*
1A3: Pumping Up Test Development with Task Based, C-callable UVM based Tests Rich Edelman & Didan Francis | *Siemens*

Paper Session 1B: Design Verification - SV & UVM
1B1: A Summary and Examination of UVM Virtual Sequence Techniques Clifford Cummings, Mark Glasser & Smita Kulkarni | *Paradigm-Works/Sunburst Design*
1B2: Sequencer Coverage Exclusion Optimiser: Streamlining Coverage Closure in Dynamic Sequencer-Based Designs Alisha Parvez, Preethi Ashok Kumar, Ravi Mangal & Yashas Uppoor | *Google*
1B3: CVM - A Library for Unified C++ and SystemVerilog Testbench Development Varun Koyyalagunta, Jiahan Zhang, Mansoor Anees & Pravin Tavagad | *Tenstorrent*

Paper Session 1C: Design Verification - SV & UVM
1C1: Optimizing CPU-Based Configuration Path Verification Through Automated C Test Case Generation with UVM RAL Ravi Mangal, Alisha Parvez & Apurva Shah | *Google*
1C2: Ensuring Deadlock-Free ASIC Operation: A Comprehensive Integration of Frequency and Operation Coverage Matrices Sohel Langardar, Naman Kothari & Balwinder Sethi | *Micron*
1C2: Robust Verification of Clock Tree Network using "Clock Monitor" Integrated by ACRMG Tejas Dipakkumar Dalal, Giridhar S, Jeevan Nataraju & Garima Srivastava | *Samsung*

Paper Session 2A: Static/Formal Verification
2A1: Reducing Area and Leakage Power: Novel Formal Methodology for Retention Sufficiency in Low Power Designs Madan Kumar R, Chepuri Venkatesh, Durga Prasad, Kuber Derasari, Srobona Mitra, Jimik Shah & Nitin Neralkar | *Qualcomm*
2A2: Navigating Complexity to Convergence: Formal Verification for Single Precision FMA Units Swaresh Phadke & Madhurima Eranki | *Intel*
2A3: Solving Formal Complexity for Linked List Hardware Designs Ankit Saxena, Radheshyam Baviskar & Shubhangi Goel | *Marvell*

Paper Session 2B: Static/Formal Verification
2B1: Halstead, McCabe, and Lint in Action: Quality Metrics for SystemVerilog Testbenches Ajeetha Kumari Venkatesan, Hemamalini Sundaram, Sivabharati Chinnaswamy & Manoj Rajendran | *Verifworks*
2B2: Cherry-picking Assertions to Enhance Convergence Ayush Vajpeyi, Muralikrishna Kukkupuni, Sangamesh Kokatnur | *nVidia*
2B3: Breaking Barriers: Formal Verification in Complex Compressor Controller Architecture Namita Rawat, Usha Rani Bagadi, Rahul Dabur & Sarsij Saurabh | *Intel*

Paper Session 2C: Static/Formal Verification
2C1: Novel Formal Equivalence approach to verify yield improvement in Complex Design Sanjana Jain & Ipshita Tripathi | *Qualcomm*
2C2: Uncovering Hardware Vulnerabilities: Formal Verification for Security-Focused Negative Testing Vedprakash Mishra & Ravi Mugidi | *Intel*
2C3: Decoding the Unknown: A Synergy of Formal and Simulation Methods for Unclassified Faults Siri Rajanedi & Prashantkumar Ravindra | *Analog Devices*

Paper Session 3A: Design & Architecture
3A1: Efficient Booth Multiplier for FIR Filter Structure Jeet Gandhi, Deepak Nair & Nehal Shah | *SCET (Academic)*
3A2: Energy-Efficient Neuromorphic In-Memory Computing for Edge AIoT: A Crossbar-Based Architecture for Sustainable Intelligence Abhay Nayak, Sakshi Pai & Shubhan Kulkarni | *KLE Tech (Academic)*
3A3: Design and development of a Hybrid Out-of-Order RISC-V Processor Model Rajesh Kumar Jain, Mayuri Gadewar, Ashish Mathur & Sourav Roy | *NXP*

Paper Session 3B: Design & Architecture
3B1: PCIe and AXI Domain Ordering - A Novel Approach using Arteris NoC and Synopsys PCIe controller Sathish Sivakumar, Venkatesh Veluvolu, Suraj Augustine, Shibin Bose Kavara & Gaurav Agarwal | *Meta*
3B2: System design exploration with fully customizable NoC Tushar Garg & Ranjan Mahajan *Synopsys*
3B3: High-Bandwidth Memory (HBM) in Custom Compute Systems: An Architectural Exploration for Future Computing Paradigms Puneet Kaushik, Vishal Kumar & Ratnala Naga Sai Mani Krishna Madana | *Synopsys*

Paper Session 3C: RISC V/Processor
3C1: Decoding the RAS Maze: Microscopic Complexity Meets Verification Shubham Mathur, Nimesh Kharat, Hadmath Singh & Darshan Hadadi | *Tenstorrent*
3C2: Implementing and Verifying RISC-V Nexus Trace Compliant Trace Encoder for High Performance Cores Sajosh Janarthanam, Rahul Behl, Sharanesh R and Hitesh Pavan Oleti | *Tenstorrent*
3C3: Catching the Unseen: A Case Study on Conquering Caching and Ordering Verification Challenges in Release Critical Unit Ayush Saraogi, Gaurav Borkar, Vivek Singh, Atharva Kakde and Ketki Gosavi | *nVidia*

Paper Session 4A: 3DIC / Chiplet Design & Verification
4A1: Breaking barriers in Advanced Multi-Chiplet AI SoCs using scalable UCIe and Boot Verification techniques Harshal Kothari, Eldin Ben Jacob, Ayush Agrawal, Vaishali Sahu, Jerin M Jose, Jasobanta Sahoo & Madhukar Ramegowda | *Samsung*
4A2: Novel Approach For Verification Of Homogeneous Multi Die Booting Using Disruptive Distributed Simulation Methodology Manikanta Gummadidala, Chethan Kumar, Nitin Kumar M, Pradeep Kumar Sahoo & Sunil Shrirangrao Kashide | *Samsung*
4A3: Efficient Verification of Multi-Die Systems using Multi-Die Co-Simulation Framework Manvendra Singh, Lawish Deshmukh & Gaurav Jain | *Renesas*

Paper Session 4B: Emulation & Prototyping
4B1: Offline FSDB based Data-Integrity Debugger for Sub-System Emulation based Runs Alvin Alphonse, Shubham Sharma & Krishna Priyanka Immidisetti | *Qualcomm*
4B2: A Hybrid Functional Verification Approach of complex designs using Python based Models Nirmal Kumar S, Pujaben Joshi, Vinay K H, Kuntal Pandya & Anil Deshpande | *Samsung*
4B3: Accelerated Coverage Closure with Emulation: Covering Real-Time Use Case Corners Vivek Tiwari & Bichu Sajeev | *Qualcomm*

Paper Session 4C: Post Silicon
4C1: Enhancing Anomaly Detection in Post-Silicon Validation Using Unsupervised Learning Techniques Santosh R & T Nandha Kumar | *NXP*
4C2: Strategic Optimization of Process Parametric Sampling: Leveraging Skew Sample Selection in Derivative Programs Pankaj Sharma | *Intel*
4C3: Accelerating DPMO Workflows Using Jenkins & AI: A Cross-Platform Validation Framework Aditi Bharmaik, Lakshminarayana Kammath, Shiju Philip Samuel & Kishan Kumar | *Intel*

Paper Session 5A: AMS & Low Power
5A1: Optimizing CA-UDFM Models for Efficient Custom IP & Standard Cell Library Development Ravi J N & Pramod Gayakwad | *NXP*
5A2: Unified Digital Mixed-Signal UVM Checkers Framework: Enabling Reuse and Scalability Across Verification Projects Shruti Easwaran & Ameya Deshpande | *Analog Devices*
5A3: EEnet based Real-Number Modelling of an RF receiver Anirudha Tiwari, Anil Kumar Pedada & Gaurav Singh | *Analog Devices*

Paper Session 5B: Design Verification - AI & ML
5B1: Scaling Generative AI for Hardware Design Verification through Synthetic Data Augmentation and Adaptive Test Bench Validation Amarnath D & Harinagarjun Chippagi | *TCS*
5B2: RAG-Powered AI Agent for Verification: Accelerating CI, Regression Debug, and Document Intelligence Bhaskar Prakash, Gaurav Jain, Yash Agrawal, Harsh Vardhan Singh & Ishdeep Singh | *Renesas*
5B3: AI-Augmented and Automated Environment for Intelligent Verification Suguna Rasu, Sireesha Gedela, Harika Mali, Venkatasai Buthukuru & Issac B | *SmartSocs*

Paper Session 5C: Design Verification - AI & ML
5C1: RAG for Formal Aware Property Generation Pradip Prajapati & Anshul Jain | *Synopsys*
5C2: Coverage Prediction and Testcase Generation Framework using Machine Learning Vardhana M, Suban Basha Shaik & Kota Subba Rao Sajja | *Qualcomm*
5C3: Scalable and cost-effective mixed signal modelling using AI with SV-RNM Sathyanarayana Ramamoorthy, Rutvikkumar Patel, Anand Rahul, Kranthi Kiran & Hareesh Perumal | *Infineon*