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Implementing Functional Coverage for Analog IPs in Mixed-Signal Verification Environments

Cross-Compatible Functional Coverage Collection for Real Number Models and Analog Schematics in Mixed-Signal Verification

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***Abstract*— This paper proposes an approach for implementing functional coverage within a UVM-based top-level testbench for analog intellectual property (IP) in ASICs. The methodology is compatible with both Digital Mixed Signal (DMS) and Analog Mixed Signal (AMS) simulations. Functional covergroups are defined in the testbench environment based on the IP specification. These covergroups help extract coverage metrics to ensure that critical chip-level features are exercised and captured by the verification plan. A key focus of this work is the adaptation of metric-driven verification techniques—common in digital verification—for use in analog IPs. The approach supports both real number models and analog schematics in mixed-signal simulations, helping to bridge the gap between analog and digital design and verification processes.**

Keywords—Metric Driven Verification (MDV), Mixed Signal Simulations, Application Specific Integrated Circuits (ASICs), Analog Mixed Signal (AMS) and Digital Mixed Signal (DMS), Real Number Modeling (RNM)

I. INTRODUCTION

With increasing demand for features in modern integrated circuits, the complexity and the size of mixed signal systems continues to grow [1]. Ensuring effective verification of such systems is therefore more crucial than ever. A traditionally well-established method for verifying digital designs and ensuring that all key aspects and features of the system are adequately tested, is the use of functional coverage in a metric-driven verification environment. However, the analog portion of the chip presents unique challenges for coverage collection and analysis, due to its continuous and highly dynamic behavior at the schematic level [2].

To facilitate fast integration, simulation acceleration, and early participation of analog IPs in the digital simulation environment, modern techniques have emerged that abstract analog behavior into discrete-time, real-valued signals compatible with digital verification tools—an approach known as Real Number Modeling (RNM) [3]. While RNM has significantly advanced analog-digital co-simulation, functional coverage for analog IPs—especially at the schematic level—remains in an underdeveloped area [4].

Prior work has been attempted to close this gap using RNM and UVM integration. McGrath et al. [5] in their work have introduced a flow combining RNMs with UVM to enable analog-digital stimulus coverage measurement and stimulus reuse. Dančak [6] proposed a UVM-based mixed signal testbench that includes SPICE-level accuracy, including analog assertions and coverage collection on a programmable analog filter but the work was based on primarily using the model abstraction rather than schematic instrumentation. Z. Ye et al. [2] showed in their work a coverage collector which required the designer to instantiate it into the actual schematic. In contrast, this paper enables direct coverage instrumentation on analog schematics and RNM by applying appropriate conversion to have signals into real-value monitors. This provides a scalable way of metric-driven verification application rigor to analog blocks, like digital IPs, with better alignment to design intent.

This paper explores a method of implementing cross-compatible functional coverage collection for real number models and analog schematics within a common UVM based top level testbenches [7]. A key contribution of this work is the possibility of defining and capturing functional coverage using SystemVerilog covergroups on analog schematic after the successful conversion of the continuous voltage and current signals into discrete, monitorable real values. The base development of these covergroups is created with the information extracted from the block specification to ensure meaningful metric reflects real operating scenarios and corner cases.

The conversion of the analog schematic internal nodes or output into discrete signals makes it possible to bridge the gap between traditional analog verification and coverage-driven digital verification. This makes these techniques, which have been long used in digital verification flows, possible to be used on analog IPs in a scalable and practical manner. Our approach supports pure analog schematic and real number model representation of the same IPs in a wide range of AMS and DMS verification setups. This work provides a systematic way of including analog schematics in functional coverage collection and improving verification quality and confidence in mixed signal ASIC designs.

II. METHODOLOGY

In a mixed-signal system, it is important to identify the key characteristics of the analog IP as well as the relevant nodes and signals required to observe them. Equal importance lies in the development of an effective strategy for implementing observable metrics that capture critical scenarios, ensuring proper operation of the block in real-world applications. Functional coverage is such a metric that can play a vital role in verifying analog schematic meets the design specification intent and the in-depth feature information extracted from the IP designer but also assessing the selected verification approach generates the appropriate stimulus at the system level to effectively exercise all important aspects of the IP [8].

The testbench structure used for this work is illustrated in Figure 1, where the key components required have been shown. The two main components of interest are the Mixed-Signal (MS) samplers and a SystemVerilog based interface called the Analog Interface.

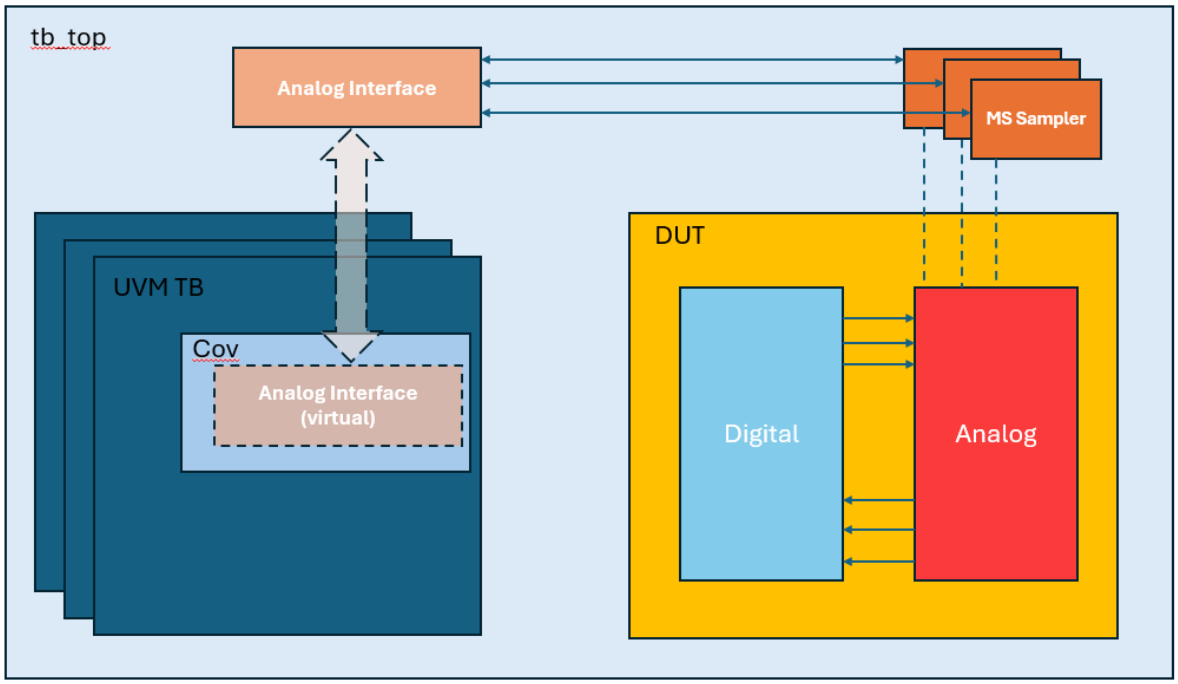

Figure 1 : Testbench architecture for sampling and covering analog portion signals

A. *Identification and Extraction of Key Analog IP Signals and Nodes*

Once the critical signals and nodes have been identified, a unified method with the MS-Sampler as shown in Figure 2 is employed to extract these signals from the boundaries of the blocks. The extracted signals are then routed as real-type values to SystemVerilog interface within the testbench architecture (TB), in the form of real type signal. The analog interface is then broadcasted to the UVM components using the uvm_config_db::set() method and respective components obtain the reference handle of the interface using uvm_config_db::get() method

into a virtual interface, giving them access to the analog component signals. This enables the reusable approach of accessing analog signals for functional coverage analysis within a UVM based mixed-signal verification environment. The relevant input and output signals of the analog IPs are extracted using the sampler on which the coverpoints were implemented. This ensures that the control signals received from the digital controller actually propagate to the respective IP.

In the MS-sampler illustration in Figure 2, READ PORT is a simulator-driven mechanism that allows access and check the hierarchical path provided to determine if the signal belongs to discrete or electrical domain. Depending on mode settings specified by CURRENT parameter _MODE and LOGIC_MODE the sampler determines if SAMPLE_CURRENT or SAMPLE_VOLTAGE is invoked. These methods allow the conversion of analog signals to levels, using the threshold provided when the type set is voltage, or real values supporting accurate monitoring of the signals across DMS and AMS simulation modes.

```
BEGIN
  INPUT : STRING PATH, LOGIC_HI, LOGIC_LO
  OUTPUT : DISCRETE REAL SIGNAL, LOGIC SIGNAL

  READ PORT FROM STRING PATH
  IF ANALOG PORT
    IF CURRENT_MODE
      SAMPLE CURRENT @ ANALOG STEP
      CONV TO DISCRETE REAL → OUTPUT REAL SIGNAL
    ELSE
      IF LOGIC MODE
        SAMPLE VOLTAGE @ ANALOG STEP
        CONV TO LOGIC USING LOGIC_HI, LOGIC_LO → OUTPUT LOGIC SIGNAL
      ELSE
        SAMPLE VOLTAGE @ ANALOG STEP
        CONV TO DISCRETE REAL → OUTPUT REAL SIGNAL
  ELSE
    IF LOGIC MODE
      SEND DISCRETE FROM PATH → OUTPUT LOGIC SIGNAL
    ELSE
      SEND DISCRETE FROM PATH → OUTPUT REAL SIGNAL
END
```

Figure 2 : Pseudo code of the MS-sampler

B. Creation of coverpoints and their sampler

To ensure specification aligned verification of the Analog-Mixed Signal (AMS) IPs a comprehensive analysis of the design specification was done as the initial step of a structured methodology. The process also included technical alignment with the respective analog IP designers. As an outcome of these sessions the required electrical characteristics such as operating voltage range, current limits and relevant timing cases to be covered were gathered.

Based on designer input and specification information, a dedicated SystemVerilog package was defined to store the design attributes which were encapsulated in real type parameters for representing continuous valued metric precisely. The package acts as the reference for the verification environment, ensuring all users operate with accurate set of values throughout the verification cycle. A sample package is shown in Figure 3 below.

Following this, a coverage plan was developed to capture functional behaviors that are critical for ensuring

```
package ams_spec_pkg;
   localparam real POR1_THRESH_UL        = X.XX; // Upper limit of threshold region
   localparam real POR1_THRESH_LL        = X.XX; // Lower limit of threshold region
   localparam real POR1_THRESH_WC        = X.XX; // Selected during Worst-case sims
   …
   localparam real LDO_A_NOM_TRIM_OUT_LL = X.XX; // Nominal OUT lower limit
   localparam real LDO_A_NOM_TRIM_OUT_UL = X.XX; // Nominal OUT UPPER limit
   localparam real UVA_MAX_THRESH        = X.XX; // Maximum Trim Threshold
   localparam real UVA_MIN_THRESH        = X.XX; // Minimum Trim Threshold
   localparam real UVA_NOM_THRESH        = X.XX; // Nominal Trim Threshold
endpackage
```

Figure 3 : Sample specification parameter package with arbitrary values

compliance with the specification. The plan was tabularized by listing the items to cover, target functional behavior and the relevance to the specification as the sample illustrated in Table 1.

Table 1 : Sample coverage plan items for analog IPs

Block	Coverage_Item	Functional Behavior	Specification Relevance
LDO_A	cp_LDO_A_sel	Selection bits exercised	Selection Settings
	cross_LDO_A_sel_x_SUPPLY	Impact of output voltage selection	Output response match selection setting
POR1	cross_SUPPLY_VOLTAGE_x_POR_TRIGGER	Expected POR1 triggers for different supply voltage region	Validate voltage trip window sensitivity
	cp_RAMP_TIME	Fast, Nominal and slow ramping of input supply	Capture ramp sensitivity
	cross_RAMP_DIRECTION_RAMP_TIME	Fast and slow ramping in both direction	Power Sequencing
UVA	cross_SUPPLY_VOLTAGE_x_UV_A_OUT_TRIGGER	UVA supply threshold match with output response	Expected UV condition trigger
	cross_RAMP_TIME_x_GLITCH_DETECTION	Rejection and Glitch Exercise	Corner Case Stimulus

The parameters from the specification package were then used for the SystemVerilog functional coverage constructs to be implemented that included relevant individual and cross coverages to address the defined coverage plan. An illustration of the sample covergroup and the respective sampling task is shown in Figure 4.

To ensure the functional intent, the targeted testcases were first launched in Digital Mixed-Signal (DMS) environment before engaging in computational exhaustive analog simulations. In the DMS setup, the analog portion of the system is represented by SystemVerilog based RNMs, which have been cross validated with the actual schematic in the block level testbenches, providing a suitable approximation of the analog blocks in the digital simulation environment.

The aim of this stage was to achieve a 100% functional coverage within the DMS environment which portrays a preliminary indicator that the testbench and stimulus logic were sufficiently specification aware and are adequately developed.

```
class ams_fcoverage extends uvm_component;
  `uvm_component_utils(ams_fcoverage)
  covergroup cg_POR_A
     option.per_instance = 1;
     cp_SUPPLY_VOLTAGE : coverpoint dut_monitor_ams_vif.POR_A_SUPPLY  {
        bins LOW       = {[0.0                 : POR_A_LOW]          };
        bins THRESHOLD = {[POR_A_THRESH_LL     : POR_A_THRESH_UL]    };
        bins NOMINAL   = {[POR_A_THRESH_NOM_LL : POR_A_THRESH_NOM_UL]}; }
     // Coverage for how fast voltage ramps up/down
     cp_RAMP_TIME : coverpoint dut_monitor_ams_vif.ramp_time {
        bins SLOW   = {[POR_A_SLOW_RAMP_LL : POR_A_SLOW_RAMP_UL] };
        bins MID    = {[POR_A_NOM_RAMP_LL  : POR_A_NOM_RAMP_UL]  };
        bins FAST   = {[POR_A_FAST_RAMP_LL : POR_A_FAST_RAMP_UL] };}
     // Voltage ramping direction up/down
     cp_RAMP_DIRECTION: coverpoint dut_monitor_ams_vif.ramp_dir {
        bins rise = {1};
        bins fall = {-1};}
     // Whether POR trip output asserted
     cp_POR_TRIGGER :coverpoint dut_monitor_ams_vif.POR_A_OUT {
        bins yes = {1};
        bins no  = {0};}
    cross_RAMP_TIME_x_POR_TRIGGER: cross cp_RAMP_TIME, cp_POR_TRIGGER;

    cross_SUPPLY_VOLTAGE_x_POR_TRIGGER: cross cp_SUPPLY_VOLTAGE, cp_POR_TRIGGER {
      ignore_bins ignore_0 = binsof(cp_SUPPLY_VOLTAGE.LOW) && binsof(cp_POR_TRIGGER.no);
      ignore_bins ignore_1 = binsof(cp_SUPPLY_VOLTAGE.NOMINAL) && binsof(cp_POR_TRIGGER.yes);}

    cross_RAMP_DIRECTION_RAMP_TIME: cross cp_RAMP_DIRECTION, cp_RAMP_TIME;
endgroup: cg_POR_A

task cg_POR_A_sample();
  forever begin
     @(dut_monitor_ams_vif.POR_A_SUPPLY_change or dut_monitor_ams_vif.ramp_time);
     cg_POR_A.sample();
  end
endtask: cg_POR_A_sample

endclass
```

Figure 4 : Example covergroup and sampling method

Once the target in the DMS simulation were achieved, the same testcases were then executed in an AMS simulation where the blocks of interest are ensured to be actual transistor level schematics by run command settings configured according to the configuration of the system. This is a crucial step as coverage holes or unexpected behavior during these simulations would indicate a schematic-level issue, potential modeling gap or even oversight of analog corner cases during the initial specification review. In Figure 5 it can be seen during pure DMS simulation the sampling of all the analog IPs (RNMs) were done but, during AMS simulations however, to ensure analog IP schematic coverage is not masked by the RNM in mixed configuration setting, sampling is enabled only if the block of interest in the configuration is set to the actual schematic. The layered approach adopted in this work, starting with the models in DMS and closing with the schematic based AMS simulations, promotes early-stage verification

```
task ams_fcoverage::run_phase(uvm_phase phase);
   super.run_phase(phase);
   fork
      `ifdef AMS_SIM
      // Invoke Sample Task for Covergroups
      `ifdef LDO_A_SCHEM
        cg_LDO_A_OUT_sample();
      `endif
      `ifdef POR_A_SCHEM
        cg_POR_A_sample();
      `endif
      `ifdef UV_A_SCHEM
        cg_UV_A_sample();
      `endif
      `else
        cg_LDO_A_OUT_sample();
        cg_POR_A_sample();
        cg_UV_A_sample();
      `endif
      join_none
endtask: run_phase
```

Figure 5 : Invoking covergroup sample method for DMS and AMS simulations

gap detection while ensuring any analog-specific anomalies are detected and resolved prior to tape-out.

C. Merger of all coverage database across configuration mix

In a pure DMS environment, a SystemVerilog RNM of the analog IPs were used to sample and observe the functional checks using assertion and functional coverage metric applied on the interface real signal sampled from the boundary of the block.

In contrast, AMS simulations have more diverse configurations, where an analog block can either remain as the model for simulation speed or the actual schematic-level block for more accuracy depending on the target portion of the system to be verified.

While DMS configuration enables to extract, consolidating and merging coverage data across regressions quite straightforward, AMS-based simulations require special consideration. This strongly holds true since analog operating points may vary under corner conditions, process-voltage-temperature (PVT) variations and test-specific modes.

To address this, in unified coverage strategy, the functional coverage models were reused in both DMS and AMS simulations. For the cases where the AMS simulations were under worst-case/ best-case corner set, the appropriate parameter value was selected from the specification package. This ensured consistency in both stimulus and observability, allowing accurate comparison of results and to detect any missed behaviors or schematic mismatches. The merged database thus reflected the real analog simulation under practical operating scenarios along with the stimulus reachability of the digital.

III. RESULTS

This method was successfully applied to both DMS and AMS simulation environments to verify various analog IPs on a chip-level design in an UVM testbench. The functional coverage from both the DMS and AMS were

analyzed thoroughly to validate the thoroughness of the targeted block verification process and to ensure complete coverage of the blocks' functionality.

Figure 6 below shows all individual coverpoints of the cg_POR_A group presented in Figure 4 achieved 100% coverage with the dedicated tests in both the DMS and AMS simulations which demonstrated full observability of the targeted signal domains. The supply voltage bins (low, threshold, nominal) and the ramp time characteristics (fast, mid and slow) were completely exercised, along with the ramping directions and POR output states. For the cross-coverage items shown in Figure 7 below, cross coverage between ramp time and POR trigger as well as between the POR trigger and the supply achieved a 100% verifying the correctness of the POR behavior across dynamic conditions. Selected irrelevant combinations were excluded using ignore_bins to focus on the spec-relevant interactions. These results demonstrated the comprehensiveness of the method to ensure not only all

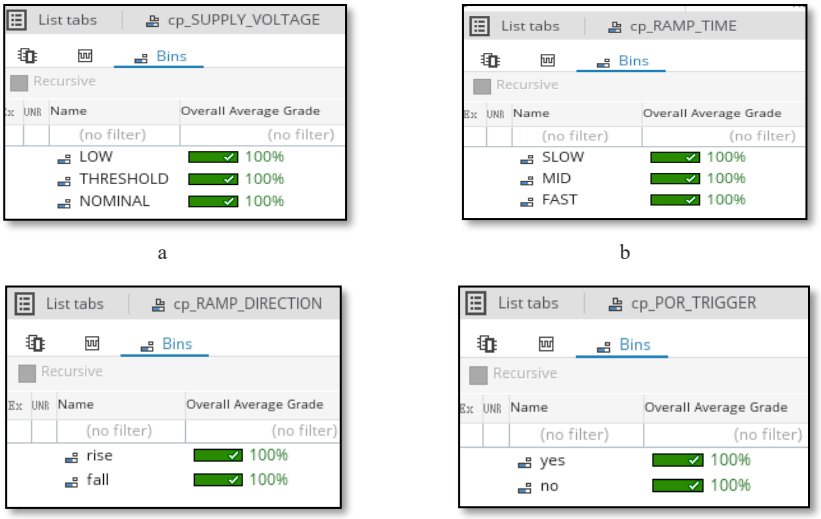

Figure 6 : Full activation of Individual coverpoint cg_POR_A group a) supply voltage, b) ramp time, c) ramp direction, d) POR trigger status

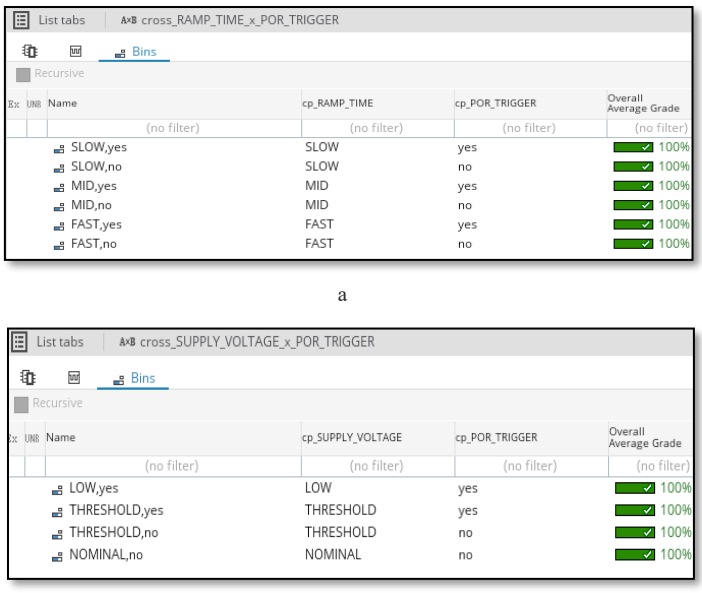

Figure 7 : Cross-Coverage Results for POR Analog Block a) ramp time x por trigger, b) supply voltage x por trigger

stimulus conditions are met but also validates the interactions of the actual schematic signals by functional coverage metric in the AMS simulation.

Following the successful coverage application on the cg_POR_A group, the methodology was extended to other analog IP blocks, such as LDO_A and UVA circuits. Dedicated AMS testcases were then developed and launched in both DMS and AMS simulations, keeping the same structural approach of parameter abstraction, sampling and coverage implementation. A unified view of the verification process was achieved by merging all testcase coverage contributions in DMS and AMS separately. As illustrated in Figure 8 , this analysis highlighted the comparative effectiveness of the DMS and AMS simulations in capturing analog behaviors. DMS simulation achieved coverage

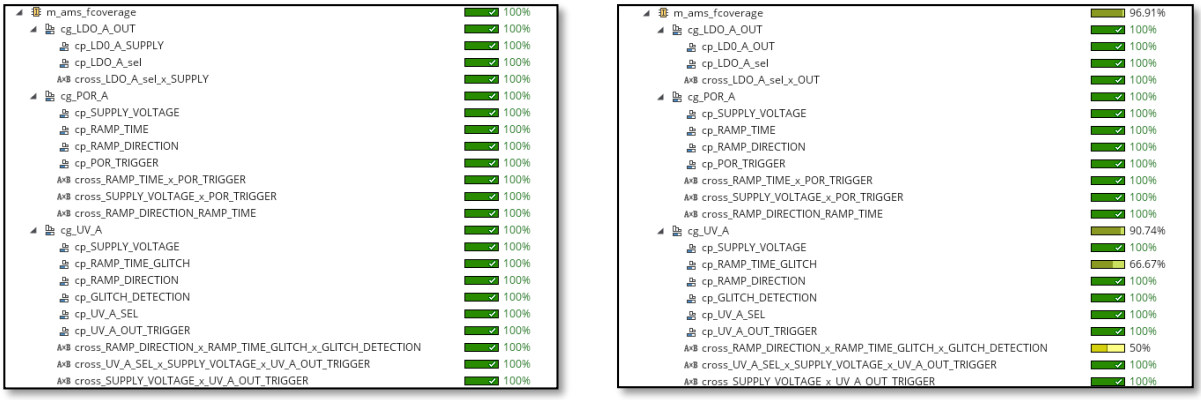

Figure 8 : a) DMS Simulation – 100% coverage across all bins; b) AMS Simulation – partial coverage due to schematic-level effects

across all individual and cross items showing the completeness of the stimulus activation through RNMs whereas AMS simulation revealed gaps, particularly in the fast corner ramping bin implemented in cp_RAMP_TIME_GLITCH (66.67 %) and the three-way cross between RAMP_DIRECTION, RAMP_TIME_GLITCH and GLITCH_DETECTION achieved 50 % overall coverage. The findings show the value of AMS simulations in exposing the real-world schematic effects, such as glitch filtering, which was not fully represented in abstraction-based models. Thus, this validates the importance of incorporating AMS coverage into the verification flow to ensure robustness, specification accurate validation of analog functionality for higher quality of verification.

IV. CONCLUSIONS

The proposed method enables the adaptation of functional coverage strategies commonly used in digital verification onto the digital/analog mixed-signal simulation environment to strengthen the bridge between analog and digital design and verification worlds. The methodology starts with the thorough analysis of the design specification and alignment with analog designers to define real-type parameter packages which serve as a single source of reference across the testbench. Using a unified MS-Sampler infrastructure, signals were probed from the schematic or model ports and then routed into the UVM environment, enabling reusable and consistent models across both DMS and AMS platforms. Results from both simulations reveal while DMS simulations ensure the stimulus reachability and rapid coverage closure, AMS simulations are essential to capture real-world effects such as glitch filtering that might be invisible to abstract RMN models. The approach showed effective bridging of the abstraction gap and validates both functional intent and schematic integrity before tape-out. As future work, once the signals are available, using the MS-Sampler, within the environment, the same probing method can be extended to develop and drive analog-aware assertions and scoreboards, increasing integration of analog observability into mainstream digital flows. Additional automation can be introduced for the sampler insertion along with adaptive bin sizing and corner-aware coverage that offer promising directions for the extension of the methodology’s reach.

V. REFERENCE

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