The Next Generation Of EDA

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History of EDA and Chip Design

Source: Alberto Sangiovanni-Vincentelli, “The Tides of EDA”, 2003
Rapid Growth of Chip Scale and Cost

Source: DARPA, IDEA Project
End of Moore’s Law?

We’re now in the Post Moore’s Law Era

Based on SPECintCPU. Source: John Hennessy and David Patterson, Computer Architecture: A Quantitative Approach, 6/e. 2018
End of Moore’s Law? No and Yes

No,
3rd dimension comes to rescue

Yes,
Less gain regarding power/performance/cost

Source: IRDS, International Roadmap for Devices and Systems
“Post-Moore” Chip Design

- No more automatic improving
- Design is tradeoff by applications
- Needs system and software efforts

Heterogeneous computing

New Memory Hierarchy and Types

I/O Integration and Optimization

Chips in Post Moore's Era

Deeper Architecture Optimization

More Instructions and Accelerators

More or Less Cores
Applications Vendors are Driving Customized Chips

Google, Microsoft, Amazon, Tesla, Apple, Alibaba, ByteDance, Midea, ....

AI, 5G, Auto-driving, Server, Desktop, Mobile Phone, Industry, ....
Chip Design is Bottlenecking System Innovations

Challenges in chip design & EDA

- Gap between system requirements and hardware chip design
- Long cycle from chip to application
- Growing cost and complexity, and risks
- Highly depends on engineer experience and efforts
- Schedule delayed by license and computing resources
Required Next Gen EDA in Post-Moore-Era

- Fill the SW-HW gap with tools
- Automatic and intelligent process
- Customizable service platform
- Shorter “Time to application”
Approaches to Next Gen EDA

More Open EDA
- Open tools interface and data for smoother process
- Open IP interface and models

Intelligent EDA
- Automate the process iterations
- Smart design, verification and implementation

EDA in the Cloud
- Flexible computing and storage
- Use computing power to reduce human efforts
X-EPIC fills in the gaps of EDA verification in China
Gather global EDA elites to accelerate the breakthrough in the integration of EDA and cutting-edge technologies

Ph.D. TC Lin
Chief Scientist

Zhenghua Qi
VP R&D
Expert in dynamic simulation and formal verification

Lanbing Chen
VP R&D
Expert in hardware verification

YT Lin
VP R&D
Expert in EDA and algorithm

Ph.D. Ti-Yen Yen
VP R&D
Expert in system design EDA
X-EPIC Verification Product Lines
Cloud-based Customized Chip Verification Solutions

- Drive Innovation
- Accelerate Product Launch
- Optimize Cost

Technical Expert Support
Scalable Cloud Ecology
Functional Safety Solution in Automotive

- Experienced automotive chip consulting and service team
- Consulting and services on chip modeling, verification, functional safety design, and DFT solutions
- Partner up with organizations such as China Automotive Technology and Research Center and Tsinghua University to provide top-to-toe functional safety solutions
Thank You