

2022
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES
VIRTUAL
FEBRUARY 28 - MARCH 3, 2022

2022 CONFERENCE PROCEEDINGS

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DVCon U.S. 2022



Welcome Message from DVCon U.S. General Chair, Vanessa Cooper General Chair – Vanessa Cooper, Verilab, Inc.

I am pleased to welcome you to our virtual DVCon U.S. 2022 conference and exhibition! This year, DVCon will offer attendees a combination of recorded presentations and live Q&A to provide an interactive, high-quality virtual experience. Attendees can look forward to outstanding technical sessions and virtual discussions on many hot topics, as well as networking during the virtual breakout sessions and opportunities to preview the latest industry design and verification tools and services from the best in the industry.

We are proud of continuing our tradition of providing an annual technical forum that serves the needs of the practicing design and verification community, organized by dedicated volunteers from the community itself.

Now in its 34th year, DVCon U.S. has established itself as the must-attend industry and user-focused conference for design and verification engineers, EDA developers, IP integrators and design managers, focusing on design and verification of electronic systems and integrated circuits. We are proud that this conference attracts wide participation from the industry from the smaller to the larger companies throughout the program and exhibition.

Our four-day virtual program contains many key design and verification topics including RISC-V, cloud-based design, open source, formal verification, portable stimulus, IP security, UVM, functional safety, prototyping and emulation, SystemC, and many others. The event provides an opportunity to discuss challenges and solutions that can be beneficial in current and upcoming projects as electronic designs and verification complexities and challenges continue to increase exponentially. Attendees will find each of these areas addressed at the conference's sessions, panels, posters, tutorials, and short workshops with an emphasis on solutions to engineers' real-world problems.

We are pleased to offer attendees an in-depth technical program with a wide variety of choices. We received numerous outstanding submissions for papers, panels, tutorials, and short workshops from the best technical minds and organizations in the industry. Our focus on the users of Accellera standard EDA languages, tools, and methodologies continues to be a DVCon 2022 hallmark. Attendees can expect to learn about both practical solutions to their pressing problems and preview the technologies that will affect them in the near future.

One of the benefits of a virtual conference is the on-demand availability of the sessions. With such an extensive program, full-conference attendees will have access to the entire program and will not have to choose between parallel sessions. They can enjoy the recorded sessions at their leisure, and from anywhere in the world.

I am pleased to present the work of the DVCon Steering Committee and Technical Program Committee, who have put together an excellent 2022 program with the support of our conference management specialists, Conference Catalysts.

Highlights of the conference include:

Accellera Day: On Monday, February 28, our conference sponsor, Accellera Systems Initiative, kicks off DVCon U.S. with Accellera Day. We will have a morning Accellera tutorial on Portable Stimulus focused real-world examples, as well as three Accellera short workshops presented by Accellera standards working group members. We will have four sponsored short workshops in the afternoon presented by design verification industry members covering topics such as RISC-V verification, emulation, power dissipation estimation, and co-verification.

Keynote: This year's keynote, "Unleashing AI/ML for Faster Verification Closure," will be given by Dr. Manish Pandey, Vice President R&D and Fellow at Synopsys, Inc.. In his presentation Dr. Pandey will discuss how the advances of utilizing Machine Learning algorithms have enabled significant gains in the verification flow.

Technical papers and posters: Technical Program Chair, John Dickol, and Poster Chair, Xiaolin Chen, have organized an excellent technical program on Tuesday and Wednesday that includes 42 papers and 14 posters. We are very grateful for the outstanding submissions and the work done by the technical program committee volunteers to review the submissions and encourage the community to keep submitting. There are so many good choices that you will want to go through the program and review it thoroughly as you plan each day. There is something for everyone in this broad, in-depth technical program. With so many interesting options, we look forward to your votes for the best paper and best poster awards after the last program session on Wednesday.

Tutorials and Short Workshops: Tom Fitzpatrick, Tutorial and Short Workshop Chair, has put together an outstanding selection of tutorials and short workshops for Monday and Thursday. The short workshops are extremely popular and are intended to give more organizations, mostly smaller companies, greater opportunity to participate in the program and give attendees more variety in shorter educational and learning sessions. We have 13 sponsored short workshops in this year's program—seven on Monday and six on Thursday—covering a wide variety of topics.

We will have three sponsored tutorials on Thursday with topics covering: Verification Strategy and Methodology, Security, and Machine Learning.

Panels: Ambar Sarkar, Panel Chair, has organized two interesting and thought-provoking panel sessions: "The Meeting of the Soc Verification Hidden Dragons," and "Going Faster – How to Cope with Shrinking Schedules and Increasing Complexity." Both panels will offer attendees an opportunity to ask questions during a live Q&A on the conference platform.

Virtual Exhibition: We are in the process of creating an interactive expo that will be a fun gathering place for attendees to connect with colleagues as well as learn about the latest products in the design and verification industry. Attendees can visit our exhibitors using the virtual space called Gather that will be integrated into the platform.

My sincere thanks to our program sponsor, Accellera Systems Initiative, industry sponsors, steering committee volunteers, technical program committee volunteers, past chairs and Conference Catalyst staff who have worked hard to put together a program that makes DVCon "the" conference for design and verification engineers.

I sincerely look forward to "seeing" you online at DVCon U.S. 2022!

Vanessa Cooper

DVCon U.S. 2022 General Chair

CONFERENCE SPONSOR



SYSTEMS INITIATIVE

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modelling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- » Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- » Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- » Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- » Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- » Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- » Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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CONFlux Platform

URL: dvcon-us-virtual.org

This platform will be used for the following:

- » Display DVCon U.S. Schedule with live Zoom links to sessions
- » Exhibit spaces for all sponsors & exhibitors
- » Live session recordings will be posted on the platform for viewing after the sessions take place
- » There will be opportunities to ask questions on presentations synchronously and asynchronously so authors can respond throughout the conference
- » The platform will be accessible to registrants through **March 31, 2022 at 23:59 PST**

Virtual Exhibit & Poster Hall (Gather.Town)

DVCon U.S. 2022 is pleased to be partnering with Gather.Town to enhance the exhibit hall and networking experience for companies and attendees. The virtual pages used at last year's virtual conference will still be available for on-demand viewing and to chat with attendees at any time. The addition of Gather.Town will make spending time with attendees just as easy as in real life. Allowing attendees to walk in and out of conversations in a natural and seamless way.

DVCon U.S. encourages all attendees to stop by the Exhibit Hall during networking, poster, sponsor, and break sessions. Allowing our attendees, sponsors and exhibitors to communicate face to face.



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A conceptual illustration of a sea where the waves are composed of binary code (0s and 1s). The sea is a deep blue color. In the foreground, a large green paper boat is prominent. In the background, three other paper boats in blue, orange, and yellow are visible, sailing towards the horizon under a bright sun. The overall scene is set against a blue sky with light clouds.

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DVCon U.S. 2022 – Technical Program

28 February 2022

All times in PST.

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
9:00 – 11:00	<p>Tutorial: PSS In The Real World</p>  <p>SYSTEMS INITIATIVE</p>	<p>Tutorial: Introduction to the 5 levels of RISC-V Processor Verification</p> 	
11:00 – 11:30	Break		
11:30 – 12:30	<p>Workshop: UVM-AMS: An Update on the Accellera UVM</p>  <p>SYSTEMS INITIATIVE</p>	<p>Workshop: IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 90 Minutes!</p> 	<p>Workshop: In-emulator UVM++ Randomized Testbenches for High Performance Functional Verification</p> 
12:30 – 13:00	Lunch Break		
13:00 – 14:00	<p>Workshop: An Overview of Security Annotation for Electronic Design Integration (SA-EDI) Standard -IPSA WG</p>  <p>SYSTEMS INITIATIVE</p>	<p>Workshop: Estimating Power Dissipation of End-User Application on RTL</p> 	
14:00 – 14:30	Break		
14:30 – 15:30	<p>Workshop: FuSa: An Update on the Accellera Functional Safety Standard</p>  <p>SYSTEMS INITIATIVE</p>		
15:30 – 17:00	Networking		



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DVCon U.S. 2022 – Technical Program

1 March 2022

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
8:00 – 8:45	Opening Session		
8:45 – 9:00	Break		
9:00 – 10:30	Portable Stimulus Standard (PSS)	Mixed Signal Verification	Memory and Cache Verification
10:30 – 12:00	Posters		
12:00 – 12:30	Break		
12:30 – 13:30	Sponsor Sessions (Cadence & Imperas) / Networking 		
13:30 – 14:00	Break		
14:00 – 15:00	Keynote: Unleashing AI/ML for Faster Verification Closure		
15:00 – 17:00	Automating Stimulus Generation	Formal Verification 1	Potpourri

imperas

Taking the RISK out of RISC-V



Tutorial: [‘Introduction to the 5 levels of RISC-V Processor Verification’](#)

Date: Monday, February 28, 2022

Time: 9:00 – 11:00am PST

Presentations:

‘Introduction to RISC-V CPU design verification’, Tuesday, March 1 2022, 12:30pm

‘Imperas RISC-V Design Verification solutions’, Tuesday, March 1 2022, 1:00pm

Visit the Imperas booth at DVCon 2022

<https://www.imperas.com/ImperasDV>

DVCon U.S. 2022 – Technical Program

2 March 2022

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
8:30 – 9:30	Panel: Panel: The Meeting of the SoC Verification Hidden Dragons		
9:30 – 10:00	Break		
10:00 – 12:00	Regression Runtime and Debug Optimization	Formal Verification 2	Automation and Other Languages
12:00 – 13:00	Panel: Going Faster – How to Cope with Shrinking Schedules and Increasing Complexity		
13:00 – 14:00	UVM Birds of a Feather		
14:00 – 15:00	Sponsor Sessions (AMIQ & Synopsys, Inc.) / Networking		
	 		
15:00 – 16:30	UVM: Knobs & Sequences	Low Power and UPF	Prototyping
16:30 – 17:00	Break		
17:00 – 18:00	Best Paper Presentation		



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DVCon U.S. 2022 – Technical Program

3 March 2022

TIME (PST)	Zoom Room #1	Zoom Room #2	Zoom Room #3
9:00 – 11:00	<p>Tutorial: The Best Verification Strategy You've Never Heard Of</p> 	<p>Tutorial: Is your Hardware Dependable? – Practical Applications for Managing Security and Safety from Software to Silicon</p> 	<p>Tutorial: ML-Driven Verification: A Step Function in Productivity and Throughput</p> 
11:00 – 11:30	Break		
11:30 – 12:30	<p>Workshop: System Verification with MatchLib</p> 	<p>Workshop: Building a Comprehensive Hardware Security Methodology</p> 	<p>Workshop: UVVM: Bringing UVM to VHDL</p> 
12:30 – 13:00	Break		
13:00 – 14:00	<p>Workshop: Finding Hidden Bugs In Deep Cycles – Advanced Debug Methodologies for Software-first System Validation</p> 	<p>Workshop: Leveraging Virtual Platforms to Shift-Left Software Development and System Verification</p> 	<p>Workshop: Proven Strategies for Better Verification Planning</p> 

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BAE SYSTEMS

Technical Program: Monday, February 28

Time Zone is PST

9:00–11:00

Tutorial: PSS In The Real World

Presented by members of Accellera System Initiative



By: **Tom Fitzpatrick**, Siemens EDA; **Matan Vax**, Cadence Design Systems; **Adnan Hamid**, Breker Verification Systems; **Hillel Miller**, Synopsys, Inc.

The tutorial will highlight the power and flexibility of the Portable Stimulus Standard from Accellera by walking through several real-world examples. Beginning with a brief overview of the standard, we will show how to use PSS to model stimulus for a variety of applications, from which multiple target-specific test implementations may be generated.

9:00–11:00

Tutorial: Introduction to the 5 levels of RISC-V Processor Verification

Presented by Imperas Software



By: **Lee Moore**, Imperas Software; **Simon Davidmann**, Imperas Software

The RISC-V open standard ISA (Instruction Set Architecture) offers developers the opportunity to configure the features and functions of a custom processor to uniquely address their target end application needs and requirements. RISC-V has a modular structure with many standard instruction extensions for additional dedicated hardware features such as Floating Point, Bit Manipulation, DSP, Cryptographic, Vectors, and many others currently under development. In addition, custom instructions can be added to further optimize the design. This tutorial covers some of the options and latest trends in simulation-based RISC-V processor verification based on industry standards with UVM and SystemVerilog testbenches. Starting with entry level, and basic trace compare followed by a detailed review of the latest approaches with Data-path lockstep-compare and Asynchronous lockstep-compare. Examples will be shown based on some popular open-source cores, including a comparison of the different DV methods and options.

11:00–11:30

Break

Technical Program: Monday, February 28 (cont.)

Time Zone is PST

11:30–12:30

Workshop: UVM-AMS: An Update on the Accellera UVM
Presented by members of Accellera System Initiative



By: **Tom Fitzpatrick**, Accellera UVM-AMS Working Group

In this workshop, the WG would share the findings, requirements and ideas collected so far and the next step plan for the standardization and would like to receive feedback from the analog/mixed-signal verification community. The UVM-AMS tutorial will also share the latest standardization and technology developments as (being) published in the Accellera UVM-AMS whitepaper.

The following main aspects of the UVM-AMS standard under consideration will be discussed at high level in this Workshop.

1. A UVM-ASM framework for the creation of analog/mixed-signal verification components and test benches by introducing both extensions to digital centric UVM verification IP classes and also related module-based components to facilitate interactions between the class-based and structural environments.
 2. A set of class-based extensions to UVM related to driver, monitor, scoreboard, etc., to support analog/mixed-signal verification
 3. A set of components and/or packages in SystemVerilog and/or Verilog-AMS to facilitate interactions between the class-based and structural environments and to interface with various types of Analog Design Representations.
 4. A set of Application Programming Interfaces (APIs) to enable the development of modular, scalable, and reusable verification components and test benches, including stimulus, sequence and analysis functions, etc.
 5. A framework for creation of Mixed Signal Verification UVM verification components (UVCs) or extensions of existing UVCs for enhanced stimulus, analysis, monitoring and debug capabilities.
-

Technical Program: Monday, February 28 (cont.)

Time Zone is PST

11:30–12:30

Workshop: IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 90 Minutes!



Presented by Agnisys

By: **Amanjyot Kaur**, Agnisys; **Neena Chandawale**, Agnisys; **Anupam Bakshi**, Agnisys;

System-on-chip (SoC) projects are naturally complex, and difficult to complete successfully in a short span of time and with limited resources. From the specification, architecture, RTL design, and software design to verification and validation, all aspects are challenging. This workshop will focus on the challenges faced by designers, driven by the convergence of applications onto a single SoC device, and will suggest methodology improvements using a revolutionary multi-platform solution, such as IDesignSpec NextGen™ (IDS-NG), for creating IPs, stitching them together into an SoC, building software and test sequences for the entire design, and documenting it. Following are the must-have features in any SoC project, which will be discussed in this workshop:

» **End-to-end automation**

- Easy mechanism for generating IP blocks with minimal time and effort
- Generated code not encrypted and indistinguishable from hand-crafted code
- Ability to target multiple aspects (firmware, verification, validation, and documentation)

» **Ability to reuse the IPs**

- Customizing the designs
 - ◇ Example: adding functionality such as additional fields and registers to the IP's reg-map
- Configuring the designs
 - ◇ Example: setting values for the parameters

» **Ability to handle different bus protocols for high performance data transfers**

» **Horizontal and vertical reuse**

- Verification is not the end: firmware, prototype, and validation are also required
- Test sequences and register specifications created at block or IP level can be run at subsystem or system level
 - ◇ Changes in bus protocol
 - ◇ Differences in configuration
 - ◇ Differences in the way transaction are carried out

» **Multiple people should be able to collaborate on a project**

- Teams must be able to keep track of changes

IDS-NG is one such cross-platform Integrated Development Environment (IDE) that helps users to create SoC specifications at an enterprise level. It handles individual IP to sub-system to SoC level and is compatible with Word, Excel, IP-XACT, RALF, CSV, and SystemRDL. This workshop will deep dive into an SoC design and complete it from start to finish, considering safety-critical design, verification, firmware, and documentation aspects. It will show how automated SoC assembly techniques are emerging as the preferred approach for reducing manual assembly and integration of IPs, and boosting productivity of SoC design teams significantly further, leading to faster time-to-market for competitive advantage. Since creating a fully validated design requires a strenuous effort from several teams working together, this workshop will help attendees learn how to automate their development process such that there is zero redundancy and zero debug time. It will take a sample SoC design and create it in RTL, stitch it together with a CPU core and other IPs, verify it with UVM, and validate it in a bare-metal C-UVM environment. All in the span of 90 minutes!

Technical Program: Monday, February 28 (cont.)

Time Zone is PST

11:30-12:30

Workshop: In-emulator UVM++ Randomized Testbenches for High Performance Functional Verification
Presented by Breker Verification Systems



By: **David Kelf**, Breker Verification Systems

A major issue with emulation today is the inability to run randomized functional verification testbenches without a performance-degrading simulator integrated “on-the-side.” This workshop will demonstrate a method to execute randomized testbenches directly on the emulator, allowing for the high-performance functional verification of large blocks, sub-systems, and full SoCs. Combined with the use of system-level encapsulated test IP and coverage-driven test synthesis, the workshop will provide participants with methods to fully test large blocks and SoCs in a manner that will uncover complex corner-cases not found with real-world test workloads. Such a solution allows companies to leverage their considerable investment in these devices more fully by extending them into the simulation acceleration space. The two major elements of modern verification processes today are:

- » The functional verification of design blocks using regression simulation and SystemVerilog/UVM test content.
- » SoC validation leveraging real world workloads and booting operating systems employing an emulator or prototyping mechanism.

However, there is a desired middle ground between these two processes where randomized functional tests executed at emulation performance will uncover additional bugs. Typical issues that could be targeted include:

- » Design functionality no longer contained within a single block, and could involve firmware as well as hardware, requiring subsystem functional verification.
- » SoC integrity, for example cache and system coherency, power domain operation, security, etc., can be fully explored.
- » Corner-cases caused by functional errors or performance bottlenecks that are harder to discover at the SoC level.

This workshop will demonstrate the use of test suite synthesis methods by which a large block, sub-system or SoC may be fully, functionally verified on an emulator using functional techniques akin to block verification, as follows:

- » Running randomized, pre-compiled test content on an emulator without a performance degrading simulator on the side executing the testbench.
- » Leveraging pre-defined infrastructure validation test content IP or configurable apps to verify common SoC issues, such as cache coherency.
- » Synthesizing test content that explores the relevant SoC state-space to track corner cases without every case having to be pre-determined.
- » SoC coverage closure prior to the availability of the RTL blocks.

Participants will learn proven, practical methods by which complex blocks, SoCs and sub-systems may be verified within ever-constrained schedules to a high degree of quality.

12:30-13:00

Break

Technical Program: Monday, February 28 (cont.)

Time Zone is PST

13:00–14:00

Workshop: An Overview of Security Annotation for Electronic Design Integration (SA-EDI) Standard

Presented by **IPSA WG**



By: **Sohrab Aftabjahani**, member of the IP Security Assurance Working Group

The importance of security in the electronic systems many of us rely on has become obvious to semiconductor design and manufacturing companies but most hardware security assurance practices in industry are still performed manually using proprietary methods. This approach is very expensive, time consuming, and error prone due to the ever-increasing complexity of systems. To address the issue, the Accellera IP Security Assurance (IPSA) Working Group was formed in 2018 by a team of security and EDA experts to work on developing a general and portable IP security specification standard to describe the IP security concerns (threat model) and to guide EDA vendors on how to produce security assurance collateral and use it for the automation of security verification. The specification was approved as an Accellera standard for Security Annotation for Electronic Design Integration (SA-EDI) in 2021. We will give an overview of this standard by going over the related collateral, methodology, a case study of the application of the standard and the roadmap of the standard.

13:00–14:00

Workshop: Estimating Power Dissipation of End-User Application on RTL

Presented by **Siemens EDA**

The Siemens logo, consisting of the word "SIEMENS" in a bold, teal, sans-serif font.

By: **Kevin G. Hotaling**, Sr. Director S2S R&D; **Magdy A. El-Moursy**, Sr. Engineering Manager
Solution Prototypes

A methodology to estimate the power dissipation of an end-user application on the Register Transfer Level (RTL) model of the target SoC platform is presented. Advanced Driving Assistance System (ADAS) of a vehicle is used as a case-study for the presented methodology. The methodology uses hybrid RTL simulation and emulation to run the heterogeneous automotive system. The methodology allows Software and Model to be included in the simulation Loop (known as Software and Model in the Loop, SiL and MiL, respectively). Virtual sensors provide a representation for the basic components of ADAS (allowing MiL). Virtualizing the system including support for the communication protocol and devices is also presented. The methodology allows simulating multiple Electronic Control Units (ECUs). The ECUs communicate using virtual buses and they are synchronized. The framework simulates/emulates real system including real Software (SW) to run on RTL model for the ECUs. It allows Co-development of the automotive system SW and HW including the mechanical parts. Power dissipation of real SW is estimated while running the target Operating System (OS) on the RTL. Power is also determined using real board to compare the power estimate with the actual power dissipation.

14:00–14:30

Break

Technical Program: Monday, February 28 (cont.)

Time Zone is PST

14:30–15:30

Workshop: FuSa: An Update on the Accellera Functional Safety Standard
Presented by Accellera System Initiative



By: **Alessandra Nardi**, Accellera Functional Safety Working Group Chair
Darren Galpin, Principal Digital Verification Engineer @ Renesas
Vatsa Prahallada, Technical Director, Design Enablement @ NXP Semiconductors

This workshop presents an update on the work performed by Accellera's Functional Safety Working Group over the past year and gives a preview of the white paper the group is planning to publish in 2022. The presentation first introduces the formalization of the Failure modes, effects, and diagnostic analysis (FMEDA) process and how it has led to the initial high-level definition of the data model, which will be the basis for the emerging functional safety standard.

The workshop will then provide detail on the data model and describe the necessary attributes to perform an FMEDA, followed by a description of some of the methodology discussions that are captured or assumed in the data model.

The workshop will also explore some directions connected to the development of the Functional Safety data format standard that the working group has identified and that will form the basis for the next steps for the working group.

15:30–17:00

Networking

Technical Program: Tuesday, March 1

Time Zone is PST

8:30–8:45

Opening Session

8:45–9:00

Break

9:00–10:30

Portable Stimulus Standard (PSS)

Session Chair: **Phu Huynh**

1088. PSS action sequence modeling using Machine Learning

Moonki Jang, Samsung Electronics; **Myeongwhan Hyun**, Samsung Electronics; **Hyunkyu Ahn**, Samsung Electronics; **Jiwoong Kim**, Samsung Electronics; **Yunwhan Kim**, Samsung Electronics; **Dongjoo Kim**, Samsung Electronics

1078. Using Portable Stimulus Standard's Hardware-Software Interface (PSS HSI) to validate 4G/5G Forward Error Correction Encoder/Decoder IP in emulation & silicon

Vinit Shenoy, Intel; **Suresh Vasu**, Intel; **Joydeep Maitra**, Intel; **Nithin Venkatesh**, Intel; **Suhas Reddy**, Intel; **Luis Campos**, Intel

1030. Co-Developing IP and SoC Bring-up Firmware with PSS

Matthew Ballance, Siemens Digital Industries Software

9:00–10:30

Mixed Signal Verification

Session Chair: **Kamel Belhous**

1091. A UVM SystemVerilog Testbench for Analog/Mixed-Signal Verification: A Digitally-Programmable Analog Filter Example

Charles Dancak, Betasoft Consulting Inc

1054. Mixed-signal Functional Verification Methodology for embedded Non-volatile Memory using ESP simulation

SangGi Do, Samsung Electronics; **Jieun Park**, Samsung Electronics; **Dohui Kim**, Samsung Electronics; **Jungkyu Jang**, Samsung Electronics

1051. Mixed-Signal Design Verification: Leveraging the Best of AMS and DMS

Rock Shi, Analog Devices; **Padmashree Bhinge**, Analog Devices; **Preston Birdsong**, Analog Devices; **Geeta Chaitanya**, Analog Devices; **Kunal Jani**, Analog Devices

9:00–10:30

Memory and Cache Verification

Session Chair: **Vibarajan Viswanathan**

1005. Modeling Memory Coherency during concurrent/simultaneous accesses

Subramoni Parameswaran, Xilinx

1007. BatchSolve: A Divide and Conquer Approach to Solving the Memory Ordering Problem

Debarshi Chatterjee, Nvidia Corporation; **Ismet Bayraktaroglu**, Nvidia Corporation; **Nikhil Sathé**, Nvidia Corporation; **Kavya Shagrithaya**, Nvidia Corporation; **Siddhanth Dhodhi**, Nvidia Corporation; **Spandan Kachhadiya**, Nvidia Corporation

1017. CAMEL: A Flexible Cache Model for Cache Verification

Yue Liu, Mediatek.inc; **Fang Liu**, Mediatek.inc; **Yunyang Song**, Mediatek.inc

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Technical Program: Tuesday, March 1 (cont.)

Time Zone is PST

10:30–12:00

Poster Session

Session Chair: Xiaolin Chen

1008. Emulation based Power and Performance Workloads on ML NPUs

Pragati Mishra, Arm Ltd; **Ritu Suresh**, Arm Ltd; **Issac Zacharia**, Arm Ltd; **Jitendra Aggarwal**, Arm Ltd

1012. Hybrid Emulation: Accelerating Software driven Verification and Debug

Issac Zacharia, Arm Ltd; **Jitendra Aggarwal**, Arm Ltd

1040. Left Shift Mechanism to Mitigate Gate Level Asynchronous Design Challenges

Rohit Sinha, Intel; **Kavya Kotha**, Intel

1042. Modeling Analog Devices using SV-RNM

Mariam Maurice, Siemens EDA (formerly Mentor Graphics)

1045. A Low Maintenance Infrastructure to Jumpstart CPU Regression and Performance Correlation

Thomas Soong, Intel; **Chenhui Huang**, Intel; **Christopher Browne**, Intel

1050. Case Study: Successes and Challenges of Reuse

Mike Chin, Intel; **Jonathan Edwards**, Intel; **Hooi Jing Tan**, Intel; **Josh Pfrimmer**, Intel

1058. Enhanced Dynamic Hybrid Simulation Framework for Hardware–Software Verification

Victor Besyakov, Untether AI

1064. Confidently Sign-off any Low-Power Designs without Consequences

Madhur Bhargava, Siemens EDA; **Jitesh Bonshal**, Siemens EDA; **Progyna Khondkar**, Siemens EDA

1067. Successive Refinement – An approach to decouple Front-End and Back-end Power Intent

Kavya Kotha, Intel Technology Pvt Ltd; **Rohit kumar Sinha**, Intel Technology Pvt Ltd

1068. Novel GUI Based UVM Test Bench Template Builder

Vignesh Manoharan, Aeva

1073. Accelerating Performance, Power and Functional validation of Computer Vision Use cases on next generation Edge Inferencing Products

Yoga Priya Vadivelu, Intel Technology India Pvt Ltd; **Arpan Shah**, Intel Technology India Pvt Ltd; **Deepinder Singh Mohoor**, Intel Technology India Pvt Ltd; **Ullas Piyush kanti karmaka**, Intel Technology India Pvt Ltd; **Praveen Buddireddy**, Intel Technology India Pvt Ltd

1082. Pre-Silicon Validation of Production BIOS, Software Use Cases and Accelerator IP Workloads using Hybrid System Level Emulation SoC Platform

Neeraj Gupta, Intel Technology India Pvt Ltd; **Reddaiah Yedoti**, Intel Technology India Pvt Ltd; **Dixit Sethi**, Intel Technology India Pvt Ltd; **Sarvesh Kumar Pandey**, Intel Technology India Pvt Ltd

1085. Avoiding Confounding Configurations: An RDC Methodology for Configurable Designs

Eamonn Quigley, Arm; **Jonathan Niven**, Arm; **Kurt Takara**, Siemens; **Christopher Giles**, Siemens

1090. Why not “Connect” using UVM Connect: Mixed Language communication got easier with UVMC

Vishal Baskar, Siemens Industry Software Inc – Siemens EDA

Technical Program: Tuesday, March 1 (cont.)

Time Zone is PST

12:00–12:30

Break

12:30–13:30

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imperas

12:30–13:30

Networking

13:30–14:00

Break

14:00–15:00

KEYNOTE: Unleashing AI/ML for Faster Verification Closure

Design verification is one of the most expensive and time-consuming activities undertaken in electronic system development. Advances in machine learning (ML) algorithms, software and practices in the last few years have given verification engineers a powerful suite of tools to attack this problem. Verification tool builders have leveraged these ML advances to accelerate coverage closure, generate better simulation distributions, and improve core verification algorithms. We will explore how exploiting supervised, unsupervised and reinforcement learning have enabled order of magnitude gains in closure convergence and verification cycle reduction.



Manish Pandey is Vice President R&D and Fellow at Synopsys, Inc., and an Adjunct Professor at Carnegie Mellon University. He completed his PhD in Computer Science from Carnegie Mellon University and a B. Tech. in Computer Science from the Indian Institute of Technology Kharagpur. He currently leads the R&D teams for formal and static technologies, and machine learning at Synopsys, Inc.. He previously led the development of several static and formal verification technologies at Verplex and Cadence which are in widespread use in the industry. Manish has been the recipient of the IEEE Transaction in CAD Outstanding Young author award, and holds over two dozen patents and refereed publications.

Technical Program: Tuesday, March 1 (cont.)

Time Zone is PST

15:00–17:00

Automating Stimulus Generation

Session Chair: Kelly Larson

1024. Systematic Constraint Relaxation (SCR): Hunting for Over-Constrained Stimulus

Debarshi Chatterjee, Nvidia Corporation; **Spandan Kachhadiya**, Nvidia Corporation; **Ismet Bayraktaroglu**, Nvidia Corporation; **Siddhanth Dhodhi**, Nvidia Corporation

1037. Two-stage framework for corner case stimuli generation Using Transformer and Reinforcement Learning

Chung-An Wang, MediaTek Inc.; **Chiao-Hua Tseng**, MediaTek Inc.; **Chia-Cheng Tsai**, MediaTek Inc.; **Tung-Yu Lee**, MediaTek Inc.; **Yen-Her Chen**, MediaTek Inc.; **Chien-Hsin Yeh**, MediaTek Inc.; **Chia-Shun Yeh**, MediaTek Inc.; **Chin-Tang Lai**, MediaTek Inc.

1001. Test Parameter Tuning with Blackbox Optimization: A Simple Yet Effective Way to Improve Coverage

Qijing Huang, UC Berkeley; **Hamid Shojaei**, Google; **Fred Zyda**, Google; **Azade Nazi**, Google; **Shobha Vasudevan**, Google; **Sat Chatterjee**, schatter@google.com; **Richard Ho**, riho

1020. Adaptive Test Generation for Fast Functional Coverage Closure

Azade Nazi, Google Research; **Qijing Huang**, UC Berkeley; **Hamid Shojaei**, Google; **Hodjat Asghari Esfeden**, Google; **Azalia Mirhosseini**, Google Research, Brain; **Richard Ho**, Google

15:00–17:00

Formal Verification 1

Session Chair: Mitchell Poplinger

1033. Accelerating Error Handling Verification of Complex Systems: A Formal Approach

Bhushan Parikh, Intel Corporation; **Peter Graniello**, Intel Corporation; **Neha Rajendra**, Intel Corporation

1086. How to Avoid the Pitfalls of Mixing Formal and Simulation Coverage

Mark Eslinger, Siemens; **Joe Hupcey III**, Siemens; **Nicolae Tusinschi**, Siemens

1060. A Hybrid Verification Solution to RISC-V Vector Extension

Chenghuan Li, Mediatek.inc; **Yanhua Feng**, Mediatek.inc; **Liam Li**, Mediatek.inc

1018. Innovative Uses of SystemVerilog Bind Statements within Formal Verification

Xiushan Feng, Samsung Austin R&D Center; **Christopher Starr**, Samsung Austin R&D Center

15:00–17:00

Potpourri

Session Chair: Nagi Naganathan

1003. A New Approach to Easily Resolve the Hidden Timing Dangers of False Path Constraints on Clock Domain Crossings

Yossi Mirsky, Intel; **Omri Dassa**, Intel

1070. Advanced Functional Verification for Automotive System on a Chip

Jaemin Hong, Samsung Electronics; **Jieun Jeong**, Samsung Electronics; **Namyoung Kim**, Samsung Electronics; **Hongkyu Kim**, Samsung Electronics; **Sungcheol Park**, Samsung Electronics; **Sangjun Mun**, Cadence Design Systems

1055. Leaping Left: Seamless IP to SoC Hand-off

Swetha Thiagarajan, INTEL; **Rashika Madan**, INTEL; **Hiran Morar**, INTEL; **Sangeivi Sivagnanasundaram**, INTEL

1048. Is it a software bug? It is a hardware bug?

Horace Chan, Microchip; **Mame Maria Mbaye**, Microchip; **Sim Ang**, Microchip

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Technical Program: Wednesday, March 2

Time Zone is PST

8:30–9:30

Panel: The Meeting of the SoC Verification Hidden Dragons

Organizer: Dave Kelf, Breker Verification Systems



Moderator: Brian Bailey, Semiconductor Engineering

Panelists:



Mike Chin, Intel

Adnan Hamid, Breker Verification Systems

Balachandran Rajendran, Dell EMC



Ty Garibay, Mythic AI



A gap in semiconductor verification has formed between block functional verification and system SoC validation. Gap requirements for large block, sub system and early SoC verification have been extended to include device integrity (cache coherency, security, etc.), together with multi-block and SW functionality. This is at odds with the inability to run high performance random tests on an emulator and the coverage that can be achieved using real world workloads. Multiple methods, some in conflict with each other, are being explored to close this gap that include formal methods, synthesis with Portable Stimulus, improved hardware execution platforms and others. This panel will compare and contrast these methods from different verification viewpoints, hashing out the pros and cons while taking input from the virtual audience.

9:30–10:00

Break

10:00–12:00

Regression Runtime and Debug Optimization

Session Chair: Dave Rich

1034. Caching Tool Run Results in Large-Scale RTL Development Projects

Ashfaq Khan, Intel Corporation

1041. Finding a Needle in a Haystack: A Novel Log Analysis Method with Test Clustering in Distributed System

Jin Choi, Samsung Electronics Co., Ltd.; **Sangwoo Noh**, Samsung Electronics Co., Ltd.;

Sooncheol Hong, Samsung Electronics Co., Ltd.; **Hanna Jang**, Samsung Electronics Co., Ltd.;

Seonhee Yim, Samsung Electronics Co., Ltd.; **Seonil Brian Choi**, Samsung Electronics Co., Ltd.

1043. Machine Learning Based Verification Planning Methodology Using Design and Verification Data

Hanna Jang, Samsung; **Seonghee Yim**, samgsung; **Sunchang Choi**, samgsung; **Seonil Brian Choi**, Samgsung

1057. Optimizing Turnaround Times In Continuous Integration Using Scheduler Implementation

Robert Strong, Samsung

Technical Program: Wednesday, March 2 (cont.)

Time Zone is PST

10:00–12:00

Formal Verification 2

Session Chair: Xiaolin Chen

1061. Raising the level of Formal Signoff with End-to-End Checking Methodology

Ping Yeung, Oski Technology; **Arun Khurana**, Oski Technology; **Dhruv Gupta**, Oski Technology; **Ashutosh Prasad**, Oski Technology; **Achin Mittal**, Oski Technology

1099. Hopscotch: A Scalable Flow-Graph Based Approach to Formally Specify and Verify Memory-Tagged Store Execution in Arm CPUs

Vikram Khosa, Arm; **Sai Komaravelli**, Arm; **Madhu Iyer**, Arm; **Abhinav Sethi**, Arm

1011. Never too late with formal: Stepwise guide for applying formal verification in post-silicon phase to avoid re-spins

Anshul Jain, Intel Corporation; **Aarti Gupta**, Intel Corporation; **Achutha KiranKumar V M**, Intel Corporation; **Bindumadhava Ss**, Intel Corporation; **Shivakumar S Kolar**, Intel Corporation; **Siva Gadey NV**, Intel Corporation

1032. Maximizing Formal ROI through Accelerated IP Verification Sign-off

Hao Chen, Intel Corporation; **Kamakshi Sarat Vallabhapurapu**, Intel Corporation; **Scott Peverelle**, Intel Corporation; **Rosanna Yee**, Intel Corporation; **Hee Chul Kim**, Intel Corporation; **Johann Te**, Intel Corporation; **Jacob Hotz**, Intel Corporation

10:00–12:00

Automation and Other Languages

Session Chair: Erik Seligman

1053. Metadata Based Testbench Generation

Daeseo Cha, Samsung Electronics

1013. Automatic Translation of Natural Language to SystemVerilog Assertions

Abhishek Chauhan, Agnisys Technology Pvt. Ltd.

1065. A Comparative Study of CHISEL and SystemVerilog, Based on Logical Equivalent SweRV-EL2 RISC-V Core

Junaid Ahmed, Lampro Mellon; **Waleed Bin Ehsan**, Lampro Mellon; **Laraib Khan**, Lampro Mellon; **Asad Aleem**, Lampro Mellon; **Agha Ali Zeb**, Lampro Mellon; **Sarmad Paracha**, Lampro Mellon; **Abdul Hameed Akram**, Lampro Mellon; **Aashir Ahsan**, Lampro Mellon

1094. Flattening the UVM Learning Curve: Automated solutions for DSP filter Verification

Avinash Lakshminarayana, Silicon Laboratories, Inc.; **Eric Jackowski**, Silicon Laboratories, Inc.; **Eric Cigan**, MathWorks; **Mark Lin**, MathWorks

Technical Program: Wednesday, March 2 (cont.)

Time Zone is PST

12:00–13:00

Panel: Going Faster – How to Cope with Shrinking Schedules and Increasing Complexity



Moderator: Eric Decker, Mythic

Panelists:



Dan Romaine, AMD
Bryan Murdock, Cruise
Jason Sprott, Verilab
Mark Glasser, Cerebras



Factors conspire to put pressure on design verification schedules. Faster product release cycles, late feature requests, late delivery of feature implementation, incomplete architectures, and more numerous features. Our coping mechanisms are failing us, as a large number of devices are either delivered late compared to baseline schedule or risk is taken from incomplete testing. Is it the level of abstraction of our day to day work? Do we need new EDA tools? Do we just need to use what we've already got? Do we need more collaboration outside our own companies? Why is our approach very different from our software counterparts? Join us in a conversation about problems with our current approaches and what comes next for design verification.

13:00–14:00

UVM Birds of a Feather

At the UVM Birds of a Feather meeting at DVCon U.S. 2021, the Accellera UVM Working Group heard from users how backward compatibility issues held back migration to the latest library. The Working Group is preparing to release a new library version (targeted for summer 2022) that reduces these issues greatly. At this meeting, the Working Group will present the expectations for this library, including the few remaining situations that may require user code updates, to again get feedback from the user community. There should also be time remaining for an open Q&A. Attendance to the Birds of a Feather is free, but registration through DVCon is required to access the platform.

14:00–15:00

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14:00–15:00

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Technical Program: Wednesday, March 2 (cont.)

Time Zone is PST

15:00–16:30

UVM: Knobs & Sequences

Session Chair: **Cliff Cummings**

1049. Advanced UVM command line processor for central maintenance and randomization of control knobs

Siddharth Krishna Kumar, Samsung Austin Research Center

1004. Knob: Command Line–Dynamic Random Generator

Haoxiang Hu, Facebook, Inc.; **Tuo Wang**, Facebook, Inc.

1093. What Does the Sequence Say? Powering Productivity with Polymorphism

Rich Edelman, Siemens EDA

15:00–16:30

Low Power and UPF

Session Chair: **Rohit Sinha**

1100. Hierarchical UPF: Uniform UPF across FE & SD

Dipankar Narendra Arya, Intel; **Balaji Vishwanath Krishnamurthy**, Intel; **Aditi Nigam**, Intel; **Tahir Ali**, Intel

1047. Path-based UPF Strategies Optimally Manage Power on your Designs

Progyna Khondkar, Siemens EDA

1029. Problematic Bi-Directional Port Connections: How Well is Your Simulator Filling the UPF LRM Void?

Brandon Skaggs, Cypress Semiconductor, An Infineon Technologies Company

15:00–16:30

Prototyping

Session Chair: **Josh Rensch**

1107. Extension of the power-aware IP reuse approach to ESL

Antonio Genov, NXP

1081. SystemC Virtual Prototype: Ride the earliest train for Time-To-Market !

Shweta Saxena, Analog Devices Inc; **Mahantesh Danagouda**, Analog Devices Inc

1071. Evaluating the feasibility of a RISC-V core for real-time applications using a virtual prototype

Juan Santana, Fraunhofer IIS/EAS; **Gabriel Pachiana**, Fraunhofer IIS/EAS; **Thomas Markwirth**, Fraunhofer IIS/EAS; **Christoph Sohrmann**, Fraunhofer IIS/EAS; **Bernhard Fischer**, Siemens AG; **Martin Matschnig**, Siemens AG

16:30–17:00

Break

17:00–17:30

Best Paper Presentation

Technical Program: Thursday, March 3

Time Zone is PST

9:00–11:00

Tutorial: The Best Verification Strategy You've Never Heard Of
Presented by Siemens EDA

SIEMENS

By: **David Aerne**, Siemens EDA; **Vijay Chobisa**, Siemens EDA; **Kurt Takara**, Siemens EDA;
Harry Foster, Siemens EDA

The latest data from the bi-annual Wilson Research Group Functional Verification survey show that, despite more than a decade of effort in establishing new verification methodologies and techniques, the problem of how to produce functionally-correct ASIC or FPGA based electronic components is still a challenge. The median project schedule for both ASIC and FPGA projects is 10-12 months, which isn't really that much time. Digging a little deeper, however, we see that over two thirds of the projects surveyed, both ASIC and FPGA, are completed behind schedule. A cynical observer might conclude that this also shows that one third of the respondents are lying, but even if that is not the case, clearly there is a problem. Looking at it another way, when we consider that only one third of ASIC projects achieve first-pass success while 83% of FPGAs have non-trivial bugs escape into production, it's not really surprising that so many projects are behind schedule. The question then becomes, is the way to hit schedules to just build in respins to account for bugs getting through, and is it okay to live with the resulting longer schedules? Or is there a way to shrink instead of pad the schedule? And if we haven't been able to do that in over a decade of focusing almost exclusively on improving verification, what is there to do? Of course, verification methodology hasn't remained static over the years, but then, neither have designs. The problem is that, as design complexity grows according to Moore's Law, verification complexity grows at a substantially greater rate. The Wilson Research Study shows that, since 2007, the mean peak number of design engineers working on a project has increased by 32% while the mean peak number of verification engineers has increased 143%. Clearly this is unsustainable. So, what is to be done? And when the huge amount of software functionality, that must also be verified, is taken into account, is there any hope at all? This tutorial will approach the question of design quality from a unique perspective. Instead of trying to verify the bugs out, what if we could avoid putting them in in the first place? The first question to answer is: Who is ultimately responsible for functional quality? To answer this question, we will explore the design and verification landscape, including the sometimes competing but hopefully complementary roles of design and verification teams throughout the process. Since there is so much software content in designs today, we must have a way of verifying a system pre-silicon to make sure it will work. But the software integration phase is not the place to be trying to debug hardware failures. Rather, we need a way to ensure bug-free hardware well before the integration phase. We will explore two approaches to minimizing hardware bugs. The first will be to apply various static and formal analysis techniques to the design to eliminate bugs before simulation even starts. We will walk through several approaches to bug avoidance, such as linting, automatic formal applications, and other static analysis techniques and see how this pro-active strategy is a clear win compared to bug detection and correction as you may be used to. Secondly, it is well known that, regardless of the programming language used, the number of bugs is directly proportional to the number of lines of code being written. Therefore, by designing and verifying at a higher level of abstraction using fewer lines of code, we can minimize the number of bugs introduced. We will step through how a design and verification flow using C++ and high-level synthesis can deliver reduced verification time and quantify the improved design quality. Additionally, once the abstract HLS design is verified, an automated RTL generation process and verification re-use methodology delivers RTL that is correct-by-construction, thus avoiding any additional bugs as we move towards integration. Once the various blocks of the system are ready for integration, we need a platform that will allow us the capacity to execute what could be a huge design, and as importantly, the speed to run near-production software while providing the visibility to ensure that our goals are being met. We will see how a unified hardware-assisted verification system, that can take you all the way from hybrid virtual platforms to emulation and FPGA-based prototyping, can achieve your quality goals in one seamless environment.

Technical Program: Thursday, March 3 (cont.)

Time Zone is PST

9:00–11:00

Tutorial: Is Your Hardware Dependable? – Practical Applications for Managing Security and Safety from Software to Silicon
Presented by Synopsys, Inc.

SYNOPSYS[®]

By: **Meirav Nitzan**, Program Management Director, Synopsys, Inc.; **Serge Leef**, Microsystems Technology Office, Program Manager, ARPA; **Bala Chavali**, Principal Member of Technical Staff, AMD; **Balaji Venu**, Arm; **Reiley Jeyapaul**, Arm

The development of secure and safe systems is of paramount importance in this age of vertically integrated electronic systems. The dependability of a system reflects the user's degree of trust in that system. It reflects the extent of the user's confidence that it will operate as users expect and that it will not 'fail' in normal use. Dependability covers the related systems attributes of reliability, availability, and security. Security weaknesses in the SoC hardware can lead to vulnerabilities that may be exploited later on by malicious intent in software or hardware. These challenging problems must be addressed pre-silicon and require rigorous methodology combined with technology to provide increased security assurance. Safety assurance requires a full product life cycle approach and is also tightly linked with security and lack of one, jeopardizes the other. In this tutorial, leading-edge SoC companies and Synopsys, Inc. experts will discuss the safety and security solution for a hardware development lifecycle to achieve pre-silicon signoff. Users will also learn the recommended methodology and best practices to address common weakness enumerations (CWE) and add counter measures to build threat and fault resilient designs. Additionally, the panel will discuss the challenges, new trends and requirements in next generation verification solutions for both ASIC and FPGA based designs. Target audience: RTL designers, Verification engineers, Project Leads and Managers.

9:00–11:00

Tutorial: ML-Driven Verification: A Step Function in Productivity and Throughput
Presented by Cadence

cadence[®]

By: **Matt Graham**, Manager Product Engineering Group Director, Cadence; **Amit Dua**, Sr. Xcelium Product Engineering Group Director, Cadence; **Daniel Hansson**, Principal ML Software Engineer, Cadence

Verification productivity has historically been largely dependent on performance tooling, and engineering ingenuity in driving these tools. The entire verification loop from test content composition, execution, debug and coverage management features engineers manually devising test programs and analyzing the results. Verification continues to evolve as block-level functional complexity increases and SoC verification becomes more relevant. Engineering teams must verify SoC infrastructure and device integrity as well as IP functionality. The complexity of 5G, Autonomous Driving, Quantum Computing and other applications shows no sign of decreasing. Verification methodologies continue to progress to meet these challenges. Engineers need some help to contain the verification explosion driven by this expansion. Machine Learning (ML) is proving itself a powerful weapon across many facets of engineering where increased complexity spills over the bounds of the human mind. Semiconductor verification clearly falls into this realm as tasks such as debug, test composition and coverage management require super-human intelligence just to perceive the problem. ML can be a vital aid to engineers struggling with these challenges in ever decreasing schedules and pressing quality demands. This workshop will guide participants through the myriad of emerging ML applications within various verification tools, demonstrating how this new technology may make their everyday efforts more effective. ML applications to be considered will include:

- Simulation regression performance and efficiency. This includes regression compression, multi-core optimization, coverage closure through UNR, etc.
- Proof engine selection and application in the use of formal methods, to maximize the capacity and convergence of this powerful tool.
- Improved efficiency and automation of the regression triage and analysis flow, accelerating both the identification and categorization of bugs, as well as the debug and re-verify loop.

Participants in this workshop will be provided a perspective on how to employ these new techniques on next generation verification environments, as they continue to drive towards first time silicon success.

Technical Program: Thursday, March 3 (cont.)

Time Zone is PST

11:00–11:30

Break

11:30–12:30

Workshop: System Verification with MatchLib

Presented by Siemens EDA



By: **Russell Klein**, Siemens EDA

MatchLib is a SystemC based throughput accurate communication package developed by Nvidia and available as open-source. It can be used to model common buses like AXI. It enables much faster simulation of a design while retaining throughput accuracy. At some point in the design cycle one or more processors will be included in the design, along with software. This workshop will describe how to bring a processor into a MatchLib design in 3 forms: host code execution, fast processor model, and RTL. We will walk through examples using the RISC-V Rocket core, a MatchLib modeled interconnect, and a simple inferencing application. The inferencing application will be run in simulations both as an abstract model in SystemC and as RTL. We will use High-Level Synthesis to create the RTL from the SystemC implementation. This workshop will show the example design running at different levels of abstraction, exploring the different verification objectives that can be achieved at each stage of the design process.

11:30–12:30

Workshop: Building a Comprehensive Hardware Security Methodology

Presented by Tortuga Logic



By: **Anders Nordstrom**, Tortuga Logic; **Jagadish Nayak**, Tortuga Logic

There has been an exponential growth in hardware security vulnerabilities over the last several years. To address this, many companies have created dedicated security teams that span across the organization. For example, marketing, legal departments and design and verification engineers are frequently involved to effectively mitigate and understand the security risks. For this entire process to be productive, an end-to-end methodology from security requirement specification to security sign-off is required. In this short workshop, we will propose a robust security program that helps prevent semiconductor security vulnerabilities during chip design and verification. The proposed steps can broadly be broken down into three concise steps: Defining Security Requirements Executing Security Verification Performing a Security Sign-off For step 1, security requirements are collected before or during the early stages of architecture design and include specifying relevant business requirements, identifying critical design assets, and addressing known hardware weaknesses from industry established weakness databases such as the Common Weakness Enumeration (CWE) list maintained by MITRE. For step 2, the security requirements are encoded into verifiable rules which are regularly applied as the chip is designed and verified. Lastly, in step 3, a security signoff phase is executed before tape-out to ensure compliance against all specified security requirements, and proper execution of the specified security rules. Throughout the workshop, participants will learn about security verification challenges and limitations of existing approaches as well as the steps required for an efficient methodology. They will also learn how Tortuga Logic's information flow based security verification technology can provide a powerful and natural approach to verify security requirements. Attendees will learn how security requirements can be easily translated to verifiable rules which are integrated in existing verification environments from Cadence, Synopsys, Inc., and Siemens EDA. Finally, to demonstrate this by example, several customer case studies showing real identified security vulnerabilities and a comprehensive live demo on an Arm Cortex-M3 based SoC will be shown. This will allow participants to understand the scope of real vulnerabilities and the operation of Radix to identify and debug SoC security issues.

Technical Program: Thursday, March 3 (cont.)

Time Zone is PST

11:30–12:30

Workshop: UVVM: Bringing UVM to VHDL

Presented by EmLogic



By: **Espen Tallaksen**, EmLogic

The UVVM (Universal VHDL Verification Methodology) is the fastest growing FPGA verification methodology – independent of language. This is due to the improvement UVVM yields in both FPGA quality and development time. This open source Library and Methodology has the most extensive VHDL verification support available and lets you verify really complex DUTs in a very efficient manner providing modularity, reusability, constrained-random stimulus and functional coverage similar to UVM. UVVM also has the largest library of open source VHDL verification models and components. With more than 50% of all FPGA designers using VHDL, UVVM provides a great verification solution for these users. This Workshop will provide an introduction to UVVM and get you started using UVVM on your next (or current) project.

12:30–13:00

Break

13:00–14:00

Workshop: Finding Hidden Bugs In Deep Cycles – Advanced Debug Methodologies for Software-first System Validation

Presented by Synopsys, Inc.



By: **Youcef Qassid**, Synopsys, Inc.; **Andy Jolley**, Synopsys, Inc.

With the complexity of today's software the length of workloads to validate hardware and software has increased to 100s of billions of cycles. As teams adopt a software-first validation strategy, modern emulation and prototyping platforms are needed to enable the highest performance as well highly efficient debug technology. In this two part tutorial (part 1: emulation, part 2: prototyping) we will use a multi-processor design case study to illustrate how emulation with Zebu® EPI emulation system and HAPS®-100 FPGA prototyping are ideal platforms to achieve software-first system validation. We will show how to rapidly identify design issues using emulation and run extremely long scenarios to find the deep cycle issues using prototyping.

13:00–14:00

Workshop: Leveraging Virtual Platforms to Shift-Left Software Development and System Verification

Presented by Cadence



By: **Ross Dickson**, Cadence Design Systems; **Pankaj Kakkar**, Cadence Design Systems

Achieving necessary throughput gains in modern semiconductor development requires new methodology thinking. The concept of "Shift-Left," where development content is composed as early in the process as possible, holds great promise. But given the range of content that is required in a modern SoC, coordinating these activities is a complex task. All too often the development process becomes serialized, driving schedule elongation and risky debug loops. What is required is a common platform that allows the early development of the various SoC components in parallel. Virtual platforms have proven an effective method for architects, designers, software engineers and verification specialists to collaborate during the design process enabling pre-silicon software development and validation. However, setting these environments up requires some specific knowledge. This workshop uses an example of early firmware development to introduce the participants to the careful planning and implementation needed to build an environment that works for all teams. Key complexities around rapid creation of models with the right balance of functionality, timing and performance are introduced and management techniques are reviewed. Emphasis is placed on the value of a consistent and coordinated debug and configuration environment to interface the Virtual Platform with software environments and to maximize performance. This workshop will provide participants with an overview of SoC modeling, tool and content interfacing, working with a platform to enable software development, and reusing the virtual platform in a hybrid mode with hardware verification solutions. Methodology aspects will also be explained to allow for appropriate configurations of the Virtual Platform for various environment requirements and constraints.

Technical Program: Thursday, March 3 (cont.)

Time Zone is PST

13:00–14:00

Workshop: Proven Strategies for Better Verification Planning
Presented by Verilab



By: **Jeff McNeal**, Verilab, Inc.; **Jeff Vance**, Verilab, Inc.; **Paul Marriott**, Verilab, Inc.

Workshop Motivation

We have found over the years that design projects face unnecessary risks and inefficiencies due to insufficient or ineffective verification planning. A poor (or missing) plan does not allow the team to easily track actual progress towards the planned schedule. On many projects, verification plans are often written early in the project, and then completely ignored by the team, never getting updated or revised as the project changes and progresses. Additionally, it is rare to find training on how to do verification planning, resulting in ad-hoc approaches. The following consequences are typically seen as a result:

- There is ambiguity on the verification status throughout the project. The team is unable to accurately articulate where the project is in the development cycle, which can cause mistrust from management.
- Tasks are given inappropriate priority, often block-based instead of feature-based.
- There is poor communication within the team. Without clearly defined deliverables and schedules from the verification team, the rest of the project members can't plan their work.
- There is a lack of risk management for common surprises, such as requirements changes, unclear specifications, blocking bugs, and implementation challenges.

Ultimately, these problems will reduce design quality, result in missed milestones, and generally make everyone's lives unnecessarily stressful.

Workshop Content

In this lecture-style workshop, we will address some common problems we have seen faced by verification teams, and provide techniques and guidelines based on extensive project experience. Attendees will learn how to identify common pitfalls that can doom a verification plan, and how to avoid them. These include the following:

- **Focus on Features:** We will demonstrate techniques for feature identification that allow us to be more strategic and accurate in our planning. These techniques produce better plans than the common approach of merely dividing a design by RTL blocks. We show how to break features into smaller sizes for more accurate scheduling, define agile-based user stories, and apply Mutually Exclusive, Collectively Exhaustive (MECE)
- **Linear Progress:** Attendees will learn how to divide work based on incremental sections, building on what is already completed. By verifying smaller sets of features, we can break away from the restrictions of block-based testbench features that limit our progress.
- **Actionable Definitions of Done:** Defining deliverables in terms of what will be demonstrated provides more clarity and accuracy over the lax definitions of done that are commonly used. It reduces the chance of work falling through the cracks and ensures the team is in alignment from the beginning. Attendees will learn how to craft deliverables that clearly communicate what feature is being verified without ambiguity from project changes.
- **Modern Methodology:** New standards and larger chip sizes mean greater reuse than ever, both of the RTL components as well as the testbench. Modern verification means that it is necessary to address items such as UPF, PSS, emulation, as well as requirements tracing in addition to the traditional tasks like scheduling and coverage planning.
- **Efficiency:** Our techniques help to simplify and compartmentalize verification plans. This can assist in getting work started sooner, as well as avoid documentation rot and allow the verification team to be more responsive to changes during the project.

By combining these techniques teams will be able to plan more efficiently, begin verification more quickly, and progress more steadily. They will also be better able to communicate their progress and status with the rest of the development team. The techniques we will be teaching are compatible with, but do not depend on, agile development, UVM/SV, or any particular vendor's tools. The techniques will touch on how to plan the development of various blocks of the testbench in a UVM style testbench, including TB infrastructure, sequences, coverage and checking.

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