2025
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES
SAN JOSE, CA, USA
FEBRUARY 24-27, 2025

- Welcome Message
- Table of Contents
- Technical Papers

2025 CONFERENCE PROCEEDINGS

SPONSORS AND ORGANIZERS

accellera
SYSTEMS INITIATIVE

Technical Support

Conference Catalysts
Phone: +1 352 872 5544
lleblanc@conferencecatalysts.com

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Table of Contents

DVCon U.S. 2025

Welcome Message from DVCon U.S. General Chair, Tom Fitzpatrick

General Chair – Tom Fitzpatrick, Siemens EDA

Welcome to DVCon U.S. 2025! For those of you for whom this is not your first DVCon, welcome back!

It is my pleasure to serve once again as the General Chair for DVCon U.S. and I truly hope that you will enjoy the program we have in store for you. In addition to the many technical sessions, which I'm sure you will find as interesting, insightful, and informative as you've come to expect from DVCon, I urge you also to take full advantage of the many networking and social opportunities that are in many ways the heart of the conference. When you put it all together, there is no better opportunity for design and verification engineers to learn the latest news, preview the hottest tools and technology, renew old friendships, and make new ones.

As always, DVCon is focused on you, whether you are a design or verification engineer, EDA developer, IP integrator, engineering manager or anyone involved in developing or using EDA tools for the design and verification of electronic systems and integrated circuits. We are proud that this conference attracts such wide participation from both user and vendor companies, both large and small. Regardless of your role in our industry, I promise that you will find information, whether from the technical program or from the exhibition, that will help you do your job better.

We will be keeping with our traditional four-day program this year, with a few modifications from what you may be used to. Monday and Thursday continue to be dedicated to Tutorials and Workshops, although you'll notice that there are many more Workshops than we typically have, providing you the opportunity to take a "deep dive" into a wider range of topics than you may have at past DVCon conferences. Tuesday and Wednesday will include the Technical Sessions in which our colleagues share in-depth presentations on the work they've done at the "bleeding edge" of our industry that you may be able to apply to your latest project. We will also continue this year with our Poster Ninja Warrior contest where the best posters, as voted for by you, will be given an opportunity to do a short presentation to the full conference attendees to vie for the title of Best Poster. This has quickly become a DVCon favorite that you won't want to miss. I encourage you to look through the Conference Program so you can tailor your DVCon experience to get the most out of it based on your particular interests.

I am particularly excited about our Keynote presentations this year. Our Industry Keynote on Tuesday will feature Ravi Subramanian, Chief Product Management Officer of the Systems Design Group at Synopsys, and Artour Levin, VP of AI Silicon Engineering at Microsoft, who will give us their perspectives on how our "AI-driven Era of Pervasive Intelligence Necessitates New Design, Optimization and Verification Strategies." On Wednesday, we'll have our Invited Keynote presentation from Rob Aitken, a long-time EDA veteran and current Program Manager at the National Advanced Packaging Manufacturing Program (NAPMP), which is part of the CHIPS for America initiative. Rob will discuss "The Role of EDA in U.S. Economic Security" to help us all better understand the impact of our industry, and our individual contributions, on the wider world beyond just getting the next chip out the door. Wednesday morning will feature a great panel addressing the pressing question, "Are AI Chips Harder to Verify?", featuring several industry luminaries who will share their unique perspectives everything from applying traditional verification techniques to these massively complex systems, to considering the application of AI-assisted approaches to help close the loop.

In addition to all of this, we'll have an exciting announcement at the conference that you'll want to hear.

I'd like to thank the steering committee, as well as our sponsors and exhibitors, for all their hard work to make this the best design and verification conference in the industry.
Thank you in advance for attending DVCon U.S. DVCon is truly one of my favorite weeks of the year, and I hope this year's conference will make you feel the same way.

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

CONFERENCE SPONSOR

Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modelling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE
- **Accellera Global Sponsors**

cadence SIEMENS SYNOPSYS®

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

2025 STEERING COMMITTEE

General Chair
Tom Fitzpatrick, Siemens EDA

Vice Chair
Xiaolin Chen, Synopsys, Inc.

Past Chair
Vanessa Cooper, Verilab, Inc.

Program Chair
Josh Rensch, Arteris

Program Vice-Chair
Dave Rich, Siemens EDA

Tutorial & Workshop Chair
Mike Meredith, Cadence Design Systems, Inc.

Panel Chair
Ambar Sarkar, Ph. D, NVIDIA

Publicity & Marketing Chair
Barbara Benjamin, HighPointe Communications

Accellera Representative & Finance Chair
Lynn Garibaldi, Accellera Systems Initiative

Conference Manager
Laura LeBlanc, Conference Catalysts, LLC

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

Technical Program Committee

Kamel Belhous
Allegro Microsystems

Rohit Bhan
Rohitbhan

Dave Burgoon
Microsoft Corporation

Xiaolin Chen
Synopsys Inc

Chandrashekar Chetput
Cadence Design Systems

Mike Chin
Intel Corporation

Vanessa Cooper
Verilab, Inc.

Clifford Cummings
Paradigm Works

Stephen Donofrio
Paradigm Works

Harry Foster
Siemens EDA

Peter George
Enfabrica

Ning Guo
AMD

Kaiming Ho
Indepentent

Saurabh Jain
AMD

Kedar Karandikar
Ampere Computing

Jonathan Karnuth
Intel Corporation

Ann Keffer
Siemens EDA

Progyna Khondkar
Cadence Design Systems

Santosh Kumar
Qualcomm Technologies Inc

David Landoll
Siemens EDA

Ahlam Lee
Andes Technology

Paul Marriott
NXP Canada

Don Mills
Microchip Technology Inc.

Nagi Naganathan
Northrop Grumman Corporation

Eldon Nelson
Synopsys Inc.

Harish Patel
Apple Inc

Mitchell Poplingher
Lockheed Martin

Ahdel Rahimi
Amazon

Logie Ramachandran
Verikwest Systems Inc

Jamie Ridgeway
Paradigm Works

Aditya Sarda
Silicon Labs

Erik Seligman
Cadence Design Systems

Rohit Kumar Sinha
Nvidia

Amit Srivastava
Synopsys Inc

John Thomson
Nvidia

Benjamin Ting
Microsoft Corporation

Greg Tumbush
EM Microelectronic US Inc.

Srivatsa Vasudevan
Ublinx

Bhaskar Vedula
Intel Corporation

Kaushik Velapa Reddy
Microsoft Corporation

Srinivasan Venkataramanan
Svenka3

Vibarajan Viswanathan
Condor Computing

DVCon U.S. 2025 - Program Grid
February 24, 2025 - Registration opens at 8:30 AM.

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
9:00 - 10:30	**Modernizing the Hardware / Software Interface - Life beyond spreadsheets. How to bring your SoC register design into the 21st Century** ARTERIS IP	**Accelerating Functional Verification with Machine Learning** TEXAS A&M UNIVERSITY	**Introduction of IEEE 1801-2024 (UPF4.0) improvements for the specification and verification of low-power intent** accellera SYSTEMS INITIATIVE	**Venue Set Up**
10:30 - 11:00	**Coffee Break** (Gateway Foyer)			
11:00 - 12:30	**Moving Forward with IEEE 1800.2 UVM: Practical Insights and the Benefits of Migration** accellera SYSTEMS INITIATIVE	**Accelerating Design & Verification with AI Agents** ChipAgents AI	**Emulation Driven Power Estimation for Real World Application** cadence	
12:30 - 13:30	**Lunch Sponsored by:** accellera SYSTEMS INITIATIVE (Pine Cedar)			**Exhibitor Set Up**
13:30 - 15:00	**PSS case studies in real-life projects** cadence	**Step Function Leaps in RTL Functional Verification Powered by AI/ML Innovations** SIEMENS	**Moving Application-level Power Optimization to Pre-silicon with Advanced Hybrid Emulation and Power Exploration Technologies** SYNOPSYS	
15:00 - 15:30	**Coffee Break** (Gateway Foyer)			
15:30 - 17:00	**PSS Comes of Age: Runtime Behavioral Coverage, Methodology and More** accellera SYSTEMS INITIATIVE	**Complex Verification Example: RISC-V MMU Verification of Virtualization and Hypervisor Operation for CPU and SOC platforms** BREKER	**Power Dynamics: Shaping the future of the data centric era** accellera SYSTEMS INITIATIVE	
17:00 - 18:00	**Welcome Reception** (Bayshore Ballroom)			

DVCon U.S. 2025 - Program Grid

February 25, 2025 - Registration opens at 8:00 AM.

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
8:30 - 9:00	**Opening Session** (Oak)			
9:00- 11:00	**Session 1: Low Power UPF**	**Session 2: Functional Safety**	**Session 3: AI & ML in Verification**	
11:00 - 11:30	**Coffee Break** (Gateway Foyer)			
11:00 - 12:30	**Poster Session** (Gateway Foyer)			
12:30 - 13:30	**Lunch Sponsored by** SIEMENS (Pine Cedar)			
13:30 - 14:30	**Industry Keynote: AI Factories Drive Re-invention of Chip Design, Verification, and Optimization** SYNOPSYS® (Oak/Fir)			**Exhibit Hall Open**
14:30 - 15:00	**Coffee Break** (Gateway Foyer)			
15:00 - 17:00	**Session 4: Portable Stimulus**	**Session 5: AI & ML Coverage Closure**	**Session 6: Regression Management**	
17:00 - 18:00	**Reception** (Bayshore Ballroom)			

DVCon U.S. 2025 - Program Grid

February 26, 2025 - Registration opens at 8:30 AM.

TIME (PST)	Monterey Carmel	Oak	Fir	Bayshore Ballroom
9:00- 10:00	**Panel: Are AI Chips Harder to Verify?** (Oak/Fir)			
10:00-10:30	**Coffee Break** (Gateway Foyer)			
10:30- 12:00	**Session 7: Formal Verification**	**Session 8: UVM in Practice**	**Session 9: Coverage Modeling**	
12:00- 13:00	**Lunch - 2026 Announcement** (Pine Cedar)			
13:00- 14:00	**Invite Keynote: The Role of EDA in U.S. Economic Security** (Oak/Fir)			**Exhibit Hall Open**
14:00- 15:00	**Poster Ninja** (Oak/Fir)			
15:00- 15:30	**Coffee Break** (Gateway Foyer)			
15:30- 17:00	**Session 10: Verification IP**	**Session 11: Testbench Generation**	**Session 12: Analog/ Digital Mixed Signal**	
17:00-18:30	**Reception & Best Paper Presentation (Bayshore Ballroom)**			

DVCon U.S. 2025 - Program Grid

February 27, 2025 - Registration opens at 8:30 AM.

TIME (PST)	Cascade	Donner	Siskiyou
9:00 – 10:30	**Next-Gen Verification Technologies for Processor-Based Systems** SYNOPSYS®	**Beyond Integers and Floating Point – Designing and Verifying with Alternate Number Representations** SIEMENS	**SoC development automation using IP-XACT 1685-2022 standard** accellera SYSTEMS INITIATIVE
10:30 – 11:00	**Coffee Break** (Bayshore Foyer)		
11:00 – 12:30	**Next-Gen Verification Technologies for Processor-Based Systems** SYNOPSYS®	**Comprehensive Glitch Signoff – Learnings and experiences from industry use cases** REAL INTENT	**CDC/RDC Interchange Format Standard** accellera SYSTEMS INITIATIVE

THANK YOU TO OUR SPONSORS

DVCON U.S. 2025 GOLD SPONSORS

AMIQ EDA

cadence®

SIEMENS

SYNOPSYS®

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCON U.S. 2025 SILVER SPONSORS

axiomise®
predictable formal verification

LUBIS EDA

BAE SYSTEMS

KEYSIGHT TECHNOLOGIES

ausdia

mirafra TECHNOLOGIES

DVCON U.S. 2025 TUTORIAL SPONSOR

SYNOPSYS®

DVCON U.S. 2025 ACADEMIC WORKSHOP SPONSOR

TEXAS A&M UNIVERSITY

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCON U.S. 2025 WORKSHOP SPONSORS

accellera SYSTEMS INITIATIVE

ChipAgents AI

SYNOPSYS®

cadence®

SIEMENS

ARTERIS IP

BREKER™

REAL INTENT

– DVCON U.S. 2025 STUART SUTHERLAND BEST PAPER AWARD SPONSOR –

AMIQ EDA

DVCON U.S. 2025 PROMOTIONAL ITEMS SPONSORS

AMIQ EDA

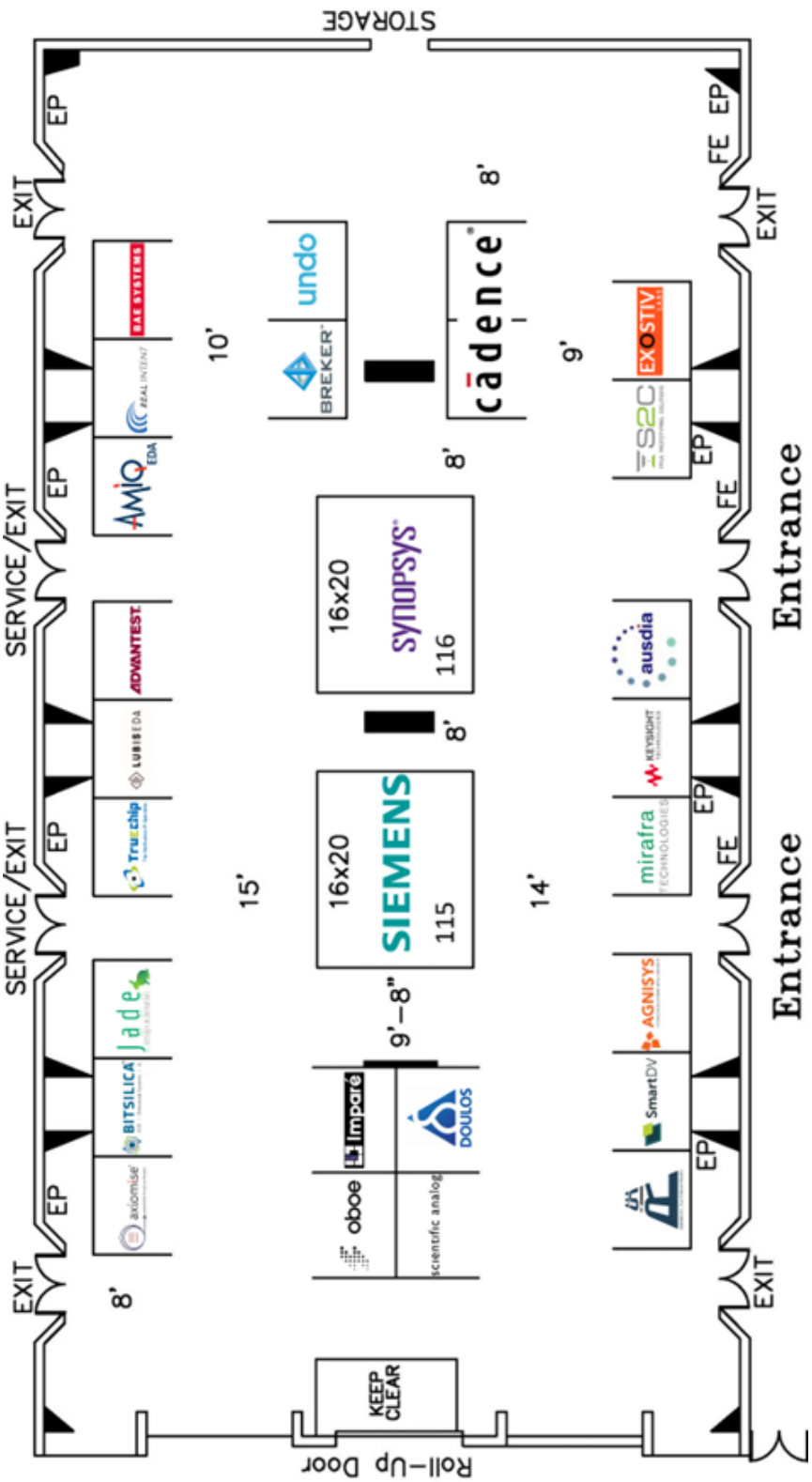
rydev ASIC Design House

chipright design and verification consultants right from the start

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

DVCON U.S. 2025 EXHIBITORS

DVCON U.S. 2025 EXHIBIT HALL MAP



Technical Program: Monday, February 24
Time Zone is PST

9:00–10:30
Modernizing the Hardware / Software Interface - Life beyond spreadsheets. How to bring your SoC register design into the 21st Century
Room: Monterey Carmel

ARTERIS IP

Speakers: **Tim Schneider**, Sr. Manager of Field Application Engineering

Advanced semiconductor designs have many components, including multi-core architectures, programmable peripherals, and purpose-built accelerators. These design elements require a pathway for embedded system software to communicate with them. This is the hardware/software interface (HSI) and it forms the foundation for the entire design project. There are many activities that need information about the HSI. These activities include device drivers and firmware, hardware design and verification, technical documentation, system diagnostics and application software. All of them need accurate, up-to-date HSI information in many different and specialized formats. A lack of unified, up-to-date information results in poor collaboration and an increased opportunity for design errors. This can lead to costly last-minute fixes or even design re-spins, impacting team productivity and compromising, the end quality of the SoC.

Arteris addresses these challenges with Magillem Registers. Magillem Registers is tool for a better HSI solution with a scalable infrastructure that promotes a rapid, highly iterative design environment to specify, document, implement, and verify address maps for complex SoCs and FPGAs.

During this tutorial, we will explain how Magillem Registers has the features and flexibility to speed development of the largest and most complex designs.

9:00–10:30
Accelerating Functional Verification with Machine Learning
Room: Oak

TEXAS A&M UNIVERSITY

This workshop presents a comprehensive exploration of machine learning (ML) techniques applied to functional verification, addressing the pressing need to automate and accelerate key stages of chip design verification. As verification consumes approximately 55% of ASIC/IC project costs and is a major bottleneck in chip design schedules, ML offers promising solutions to enhance productivity and reduce time-to-market. Our workshop aims to bridge the gap between cutting-edge research and practical industry applications, providing attendees with actionable insights and strategies to implement ML in their verification processes.

The workshop begins with a state-of-the-art survey of ML applications in verification, including recent advancements in using large language models (LLMs) for test bench generation and assertion insertion. We will discuss current limitations and challenges in applying ML to complex, large-scale designs, setting the stage for our exploration of novel solutions.

9:00–10:30

Introduction of IEEE 1801-2024 (UPF4.0) improvements for the specification and verification of low-power intent

Room: Fir

accellera SYSTEMS INITIATIVE

As advanced low-power architectures have become more pervasive in industry, the complexity of these architectures has driven new methodologies for the verification, implementation, and reuse of power intent specifications. Modern low-power designs place requirements that span from enabling more flexible IP design reuse to providing well defined interfaces between analog and digital components in simulation. The IEEE 1801-2024 (UPF 4.0) standard provides several key enhancements that are required to keep pace with these innovations in lowpower design. The workshop will provide an overview of the enhancements to the standard from both a conceptual and a command level. New concepts such as virtual supply nets, refinable macros, and UPF libraries will be introduced, as well as rearchitected features with respect to interfacing between analog and digital simulation and advanced state retention modeling. While the new IEEE 1801-2024 standard provides numerous detailed clarifications and enhancements to the previous version, this workshop will focus on the key changes that will impact most designers and changes that enable new functionality.

In the six years since IEEE 1801-2018 was introduced there have been a number of trends in design that required additional features in the standard to support. Key among these is an increasing need for co-verification of analog and mixed signal content. Another trend is that IP providers are providing pre-verified low-power IP to their customers, but struggle to provide a flexible IP for implementation in multiple design contexts while preserving the verification signoff on the blocks. To address these trends, IEEE 1801-2024 provides new features such as Value Conversion Methods (VCM) and HDL tunneling that help bridge the gap between the analog and digital designs, and the concept of a refinable macro to address the IP reuse requirements.

Real-world usage of the previous standard (IEEE 1801-2018) has prompted clarifications and enhancements that will have a significant impact on users of the standard. For example, the modeling of state retention has been entirely reworked to provide better modeling of the retention power intent and to more accurately define requirements on the retention control signals in each phase of state retention. The new standard also codifies some common design practices to make a clear, more consistent implementation across vendors. The new concept of virtual supplies is one such case. It removes the ambiguity that exists today when supplies are used to provide port constraints or to simplify power state definitions, but do not imply a physical supply net in implementation.

This workshop will introduce these new concepts and their associated commands and provide an overview of the major semantic and syntax changes introduced by IEEE 1801-2024. This understanding will help attendees transition to the new standard and improve the quality of advanced low-power architectures and design environments.

Authors:

- **John Decker,** IEEE P1801 Workgroup Chair
- **Daniel Cross,** Cadence
- **Amit Srivastava,** IEEE P1801 Workgroup Vice-Chair
- **Lakshmanan Balasubramanian,** IEEE P1801 Workgroup Secretary
- **Marcelo Glusman,** Cadence
- **Medaramitta Jeevan,** Siemens EDA
- **Gabriel Chidolue,** Siemens EDA
- **Rick Koster,** Siemens EDA
- **Raguvaran Easwaran,** Intel
- **Paul Bailey,** Nordic Semiconductor
- **Progyna Khondkar,** Cadence

10:30 – 11:00
Coffee Break
Room: Gateway Foyer

11:00 – 12:30
Moving Forward with IEEE 1800.2 UVM: Practical Insights and the Benefits of Migration
Room: Monterey Carmel

Presenter: **Justin Refice,** NVIDIA

As the IEEE 1800.2 UVM standard continues to evolve, Accellera's release of the latest reference implementation (2020.3.1) introduces significant enhancements for verification engineers. This workshop focuses on the practical aspects of adopting the new version, providing an overview of its performance and functional improvements, as well as guidance for a smooth transition.

We will examine the migration process from UVM 1.2, emphasizing how the challenges faced in earlier transitions have been addressed. Particular attention will be given to backward compatibility and resources now available, such as the public GitHub repository, which supports faster delivery of bug fixes and migration aids.

Participants will also gain an understanding of the performance benefits introduced and how these enhancements can accelerate verification workflows compared to legacy versions. The workshop will also provide an overview of functional improvements, including enhancements that reduce the need to maintain modified versions of the UVM library. Finally, we'll open the floor for discussion on potential future enhancements, including plans for reworking the Register Abstraction Layer (RAL).

11:00 – 12:30
Accelerating Design & Verification with AI Agents
Room: Oak

In this 90-minute session, participants will explore how AI-driven agents can revolutionize today's SoC design and verification workflows. We will discuss the latest breakthroughs in agentic AI algorithms for hardware modeling, constraint-solving, and automated test generation—showing how these AI agents not only expedite verification cycles but also enhance overall design quality. Using real-world use cases and practical demonstrations, attendees will gain actionable insights into integrating AI solutions for faster time to market, improved reliability, and lower development costs.

Introduction to ChipAgents and William Wang

ChipAgents is a pioneering semiconductor software company at the forefront of AI-driven automation in chip design and verification. By combining advanced AI algorithms with deep hardware expertise, ChipAgents delivers scalable solutions that help design teams catch bugs faster, optimize performance, and reduce project risk. The workshop organizer, William Wang, CEO and Founder of Alpha Design AI, is an industry thought leader recognized with the prestigious IEEE Laplace Award for his significant contributions in Artificial Intelligence. William has also been honored with "AI's 10 to Watch," the DARPA Young Faculty Award, the NSF CAREER Award, and the Karen Sparck Jones Award by the British Computer Society, underscoring his impact in applying machine intelligence to accelerate innovations.

Technical Program: Monday, February 24 (cont.)
Time Zone is PST

11:00 – 12:30
Emulation Driven Power Estimation for Real World Application
Room: Fir

Arti Dwivedi, Group Director, Product Engineering, Cadence Design Systems

Yash Bhagwat, Senior Emulation Verification Engineer at NVidia

Michael Young, Senior Product Management Group Director, Cadence Design Systems

Performance per watt is a key success criteria for complex billion gate SOCs. Optimizing for performance per watt requires power estimation for real application workloads early in the design flow.

Palladium Dynamic Power Analysis (DPA) offers novel technologies to estimate power of real-world scenarios spanning billions of cycles for billion gates designs in hours. Palladium's fast dynamic power analysis enables identification of power-hotspots in the design and provides insights into power efficiency of software-hardware interaction.

This workshop will present the power estimation methodologies for different types of emulation workloads to drive design power efficiency with fastest turnaround for long vectors. The presentation will include case studies on how Palladium users have drastically improved the turnaround of power estimation for long emulation vectors compared to traditional power methodologies. Presentation will also share how Palladium users have improved methodologies for IR drop analysis using DPA, enabling power integrity sign-off for real worst case power scenarios.

12:30 – 13:30
Lunch
Room: Pine Cedar

We invite you to join us for an engaging luncheon on Monday, February 24 as Accellera Chair Lu Dai provides an update on the latest advancements in standards development and offers a glimpse into exciting future initiatives. The luncheon will also honor a distinguished Accellera working group member with the prestigious Technical Excellence Award, celebrating their exceptional dedication and contributions to the ongoing evolution of our standards. Tom Fitzpatrick, Universal Verification Methodology Mixed-Signal (UVM-MS) Working Group Chair, will conclude the luncheon with an introduction to the upcoming UVM-MS 1.0 standard.

12:30 – 16:30
Exhibitor Set Up
Room: Bayshore Ballroom

13:30 – 15:00

PSS case studies in real-life projects

Room: Monterey Carmel

PSS (Portable Test and Stimulus Standard) was first released in 2018 to enable a single representation of stimulus and test scenarios that can be re-used across multiple verification and test engines and also provide the means for intelligent constrained random testing at the SoC level.

Six years later, PSS is adopted by many chip design companies in multiple use cases, verticals, and platforms!

In this workshop, we will review practical applications and real-life use cases of PSS adoption, focusing on the challenges that PSS was used to address, the way it was used to tackle them with Perspec™ System Verifier.

Workshop Highlights

During this workshop, you will have the opportunity to:

- Real-world applications: Discover how PSS is being used in real-world projects to improve productivity, enhance SoC-level coverage, and reduce time-to-market.
- Industry insights: Learn from industry leaders and pioneers who have successfully implemented Portable Stimulus in their projects and gain valuable insights into best practices and emerging trends.
- Gain in-depth knowledge: Our expert speakers will delve into the latest enhancements of the PSS standard and Cadence's System Verification libraries.

Who Should Attend?

This workshop is tailored for professionals in hardware and software design, verification, and testing. Whether you're a design engineer, verification engineer, or project manager overseeing system-on-chip development, this workshop is designed to enhance your understanding of Portable Stimulus and provide you with the knowledge and skills to apply it effectively in your projects.

13:30 – 15:00

Step Function Leaps in RTL Functional Verification Powered by AI/ML Innovations

Room: Oak

In the rapidly evolving landscape of semiconductor design, the complexity and scale of digital circuits continue to grow exponentially. Traditional methods of Register-Transfer Level (RTL) functional verification are increasingly challenged by these advancements, necessitating innovative approaches to ensure robust and efficient verification processes. This technical workshop aims to explore the integration of Artificial Intelligence (AI) and Machine Learning (ML) engines into RTL functional verification workflows, showcasing new products and methodologies that leverage these cutting-edge technologies.

The workshop will feature a comprehensive overview of the current state of RTL functional verification, highlighting the limitations and bottlenecks faced by verification engineers. We will introduce a suite of new AI/ML-powered tools designed to enhance verification efficiency, accuracy, and coverage. These tools employ advanced algorithms to automate pattern recognition, anomaly detection, and predictive analysis, significantly reducing the time and effort required for verification tasks.

Via the following presentations on "smart" automation for design and testbench creation, debug and regression analysis, engine optimizations, and muti-platform coverage merging and analysis, participants will be able to map their needs to these new AI/ML-accelerated flows:

13:30 – 15:00

Step Function Leaps in RTL Functional Verification Powered by AI/ML Innovations (cont.)

1. Introduction to AI/ML in RTL Verification: Understanding the basics of AI/ML and their applicability to RTL verification.
2. New AI/ML-Driven Verification Tools: Demonstrations of the latest products incorporating AI/ML engines, including their features, benefits, and use cases.
3. Case Studies and Real-World Applications: Insights from industry leaders on successful implementations of AI/ML in RTL verification, showcasing tangible improvements in verification outcomes.
4. Future Trends and Challenges: Exploring the future potential of AI/ML in verification and addressing the challenges associated with their adoption.

By the end of the workshop, attendees will have a deeper understanding of how AI/ML can transform their overall approach to RTL functional verification, driving innovation and efficiency in their verification processes.

Join us to stay ahead of the curve and harness the power of AI/ML to tackle the complexities of modern RTL D&V!

13:30 – 15:00

Moving Application-level Power Optimization to Pre-silicon with Advanced Hybrid Emulation and Power Exploration Technologies

Room: Fir

As the semiconductor industry is experiencing an explosion in design size and complexity, it is accompanied by a need to deliver software readiness when the silicon is back in the lab. One of the key targets for software readiness is the adherence to a power budget with real software applications stressing the hardware design. There are 2 key elements to validating power budgets in pre silicon – performance of the model and the ability to execute a full software stack. Combining a fast virtual prototype of the CPU sub-system with the RTL of the remaining SoC running on an emulator typically produces a 10x speed-up over fully-RTL emulation setups. Recent advances in both virtual prototyping and emulation now yield another leap in hybrid performance, which enables pre-silicon execution of entire software stack. Similarly, the power analysis engine needs to become efficient to be able to handle these large workloads and be able to address requirements of peak power, average power and leakage power. In this workshop, we will first review the latest state-of-the-art of hybrid emulation technologies and use-cases. We will then illustrate the application of hybrid emulation for pre-silicon power optimization.

15:00 – 15:30

Coffee Break

Room: Gateway Foyer

15:30 – 17:00

PSS Comes of Age: Runtime Behavioral Coverage, Methodology and More

Room: Monterey Carmel

With the release of the Portable Stimulus Standard (PSS) version 3.0, and additional work ongoing in the Accellera Portable Stimulus Working Group, the PSS language has taken the next steps to maturity.

Just as PSS has elevated the use of constrained-random verification from the transaction level in UVM to the scenario level, PSS 3.0 elevates the concept of runtime coverage from transaction-level data via covergroups, which PSS has supported for quite some time, to behavioral coverage to enable the tracking of sequential and concurrent behaviors to understand whether the scenarios generated from a PSS model execute the behaviors required to meet the intended deliverables. The first section of this technical Workshop will explain Runtime Behavioral Coverage in PSS and present examples to show how it is used to monitor and identify a variety of PSS behaviors as they are executed in the generated scenarios. We will also show how behavioral coverage statements may be combined with data coverage to understand the full usage and value of this new PSS feature.

The second section of the Workshop will provide an update on new and ongoing efforts in the Working Group, including a methodology library, similar to what UVM provides for SystemVerilog, to provide greater interoperability between PSS models, whether created in-house or sourced from third parties. This example-based approach will address solutions to common challenges faced in test creation and will underscore the necessity for an industry-wide PSS methodology library while showing the quality of PSS tests and the ease with which they can be created.

You will learn:

- How behavioral coverage can determine whether runtime concurrency matches test intent
- How to use key behavioral coverage operators and statements
- What new PSS features are coming
- How a PSS methodology library supports interoperability and simplifies scenario creation

Presenters include:

- Hillel Miller, Synopsys
- Prabhat Gupta, AMD

15:30 – 17:00

Complex Verification Example: RISC-V MMU Verification of Virtualization and Hypervisor Operation for CPU and SOC platforms

Room: Oak

The advent of RISC-V has presented verification teams with many new verification challenges. Complex interactions at the system level, that must be considered when developing a RISC-V core, include uncommon scenarios for block level verification teams. As we move towards more system-level verification in general, these types of scenarios will become commonplace. As such, RISC-V verification provides, among many other things, an interesting learning vehicle for general verification challenges to come.

This workshop will discuss a specific complex, but yet commonplace, verification challenge for any team working on a complex RISC-V core. We will consider the verification of a Memory Management Unit (MMU) that includes virtualization and hypervisor operation. These scenarios need to consider both Single- and Multi-core devices along with an Input Output Memory Management Unit (IOMMU) and uncore IP interaction.

Complex Verification Example: RISC-V MMU Verification of Virtualization and Hypervisor Operation for CPU and SOC platforms (cont.)

In this case, scenarios that will be considered will include a broad range of Page Table Entry (PTE) setup cases and page fault cases, with diMerentiated behavior at diMerent privilege levels. Many use cases for the MMU will be included from various data read and write operations and code fetches, up to issues such as self-modifying code. Complex interactions that include a range of Cache Coherency scenarios, RISC-V Weak Memory Ordering (RVWMO) that makes use of the fence instructions, Translation Lookaside BuMer (TLB) invalidation and sfence.vma cases, and many other situations.

As part of the workshop, a test place with a full range of scenarios will be discussed and considered, and eMicient tests will be shown that provide high coverage, even at the more complex system level. This workshop will be useful for anyone working on RISC-V cores or processor verification, but is also applicable for any verification engineer considering the development of more complex testbenches that extend into system interaction.

15:30 – 17:00

SIEMENS

Power Dynamics: Shaping the future of the data centric era

Room: Fir

From battery operated handhelds to datacenter servers, electronic devices are power consumers. Depending on the application area, total power consumption varies based on the semiconductor (SoC) content used, and the intended purpose for the device. One truth applies to every SoC, power analysis requires a holistic methodology from architectural exploration to tape-out to accurately addresses power concerns.

One of the key factors used to calculate power consumption is the dynamic power that has become increasingly important in technologies such as FinFET. Here the gate area has increased; hence, the load capacitance is larger and the impact of the switching power more pronounced.

In this workshop, join us in exploring the power dynamics shaping the future of the data centric era. We'll look at new methodologies for power profiling and analysis and their positive impact on meeting power requirements.

17:00 – 18:00

Welcome Reception

Room: Bayshore Ballroom

Technical Program: Tuesday, February 25
Time Zone is PST

8:30 – 9:00
Opening Session
Room: Oak

9:00 – 11:00
Session 1: Low Power UPF
Room: Monterey Carmel

Session Chair: **Progyna Khondkar**

[1082] Refinable Macros and Terminal Boundaries in UPF 4.0: Empowering Soft IPs of the Future
Amit Srivastava, Synopsys Inc; **John Decker,** Cadence Design Systems; **Lakshmanan Balasubramanian,** IEEE & ACM

[1127] Applications for UPF HDL Supply Tunneling in Mixed Signal Design
Daniel Cross, Cadence Design Systems

[1136] Future Proofing Power Intent Specification through Unified Power Format 4.0 for Evolving Advanced State Retention Strategies
Lakshmanan Balasubramanian, IEEE, ACM & Texas Instruments (India) Pvt. Ltd.; **Amit Srivastava,** Synopsys Inc.; **Raguvaran Easwaran,** Intel India Pvt. Ltd.; **John Decker,** Cadence Design Systems; **Rick Koster,** Siemens EDA; **Progyna Khondkar,** Cadence Design Systems; **Paul Bailey,** Nordic Seminconductors; **Barry Pangrle,** Abacus Semiconductor Corporation; **Shreedhar Ramachandra,** Synopsys Inc.; **Phil Giangarra,** Cadence Design Systems; J**ohn Biggs,** IEEE; David Cheng, Cadence Design Systems

[1034] What's New in IEEE 1801 and Why you Need to Know Now?
Progyna Khonkdar, Cadence Design Systems

9:00 – 11:00
Session 2: Functional Safety
Room: Oak

Session Chair: **Ann Keffer**

[1062] Lessons Learned Using Formal for Functional Safety
Doug Smith, Doulos

[1072] A Comprehensive Safety Verification Solution for SEooC Automotive SoC
Gaurav Kumar Yadav, Samsung Semiconductor India R&D; **Debasis Mishra,** Samsung Semiconductor India R&D; **PrashantKumar Shukranath Sonavane,** Samsung Semiconductor India R&D; **Aniruddha N Anavatti,** Samsung Semiconductor India R&D; **Pattan Farooq Khan,** Samsung Semiconductor India R&D; **Garima Srivastava,** Samsung Semiconductor India R&D

[1140] A Novel Approach for faster diagnostic coverage closure aided by STL of CPU Cores
Naveen Srivastava, Samsung Semiconductor India R & D; **Amresh Kumar Lenka,** Samsung Semicoductor India R&D; **Varun Kumar C,** Samsung Semiconductor India R & **D; Subramanian R,** Samsung Semiconductor India R & D; **Sekhar Dangudubiyyam,** Samsung Semiconductor India R & D

[1055] Automated Formal Verification of Area-Optimized Safety Registers in Automotive SoCs
Shuhang Zhang, Infineon Technologies AG; **Bryan Olmos,** Infineon Technologies AG

Technical Program: Tuesday, February 25(cont)

Time Zone is PST

9:00 – 11:00

Session 3: AI & ML in Verification

Room: Fir

Session Chair: **Paul Marriott**

[1005] Bridging the Verification Gap in DSP Designs A Case Study on LMS Adaptive Filter Datapath Cycle-Accurate Verification Using Generative AI and MATLAB DPIGEN

Kuan-Ting Chen, Silicon Labs

[1016] Towards Automated Verification IP Instantiation via LLMs

Ghaith Bany Hamad, Nvidia; Michael Marcotte, Nvidia; **Syed Suhaib,** Nvidia

[1048] Saarthi: The First AI Formal Verification Engineer

Aman Kumar, Infineon Technologies; **Deepak Narayan Gadde,** Infineon Technologies; **Keerthan Kopparam Radhakrishna,** Infineon Technologies; **Djones Lettnin,** Infineon Technologies

[1030] An Early Stage Coverage Measurement Methodology For Common Features Of System-On-Chip Verification, Using Design Metadata And Large Language Models

Myeongwhan Hyun, Samsung Electronics; **Jaehyeok Lee,** Samsung Electronics; **Jin Choi,** Samsung Electronics; **Dongjoo Kim,** Samsung Electronics; **Seonghee Yim,** Samsung Electronics; **Youngsik Kim,** Samsung Electronics; **Seonil Brian Choi,** Samsung Electronics

11:00 – 11:30

Coffee Break

Room: Gateway Foyer

11:00 – 12:30

Poster Session

Room: Gateway Foyer

[1004] A Survey of Predictor Implementation using High-Level Language Co-simulation

Sean Little, Verus Research

[1008] Automating Datapath Verification and Bug Correction via Equality Saturation

Emiliano Morini, Intel Corporation; **Samuel Coward,** Intel Corporation; **Theo Drane,** Intel Corporation; **Rafael Barbalho,** Intel Corporation; **George Constantinides,** Imperial College London

[1027] Technical Documents Version Management System Based on Large Language Models

Siarhei Zalivaka, SK Hynix

[1028] Continuous Integration in SoC Design: Challenges and Solutions

Wei Liu, sudoinfotech; Jianjun Li, sudoinfotech; Liangfeng Yang, sudoinfotech; Liang Li, sudoinfotech

[1031] Enhancing SDC Verification in SoCs: Heatmap Visualization and Machine Learning Approaches for Optimal Coverage Closure

Seungkyu Baek, Samsung Electronics; **Jaein Hong,** Samsung Electronics; **Moonki Jun,** Samsung Electronics; **Sungcheol Park,** Samsung Electronics

[1033] A Hybrid Verification Approach for Cache Coherent Systems: Functionality and Performance

Jiang-Tang Xiao, Mediatek; **Yung-Cheng Chen,** Cadence; **Harish Peta,** Cadence; **Osmond Yao,** Mediatek

[1035] An Effective Digital Logic Verification Methodology of High-Speed Interface IP Using a Configurable AFE Behavioral and C hannel Model

Kiyoon Shim, Samsung electronics; **Beomseok Kang,** Samsung electronics; **Seungsik Eom,** Samsung electronics

[1036] Breaking the Formal Verification Bottleneck: Faster and More Comprehensive Testing of Parameterized Modules

Menachem Rappaport, Veriest; **Ariel Ansbacher,** Veriest; **Elchanan Rappaport,** Veriest

Poster Session (cont.)

[1039] Time-travel Debugging for High-level Synthesis Code
Jonathan Bonsor-Matthews, LightBlue Logic Limited; **Greg Law,** Undo Limited

[1046] Static Structural Analysis and Formal Verification of SoC with Software Safety Mechanisms for Functional Safety
Hyunsun Ahn, Samsung Electronics Co., Ltd.; **Euisang Yoon,** Siemens EDA; **Namyul Cho,** Siemens EDA; **Arun Gogineni,** SIEMENS EDA; **Ann Keffer,** Siemens EDA; **Sungjin Park,** Siemens EDA; **Sungyun Yoo,** Siemens EDA; **Bumju Kim,** Samsung Electronics Co., Ltd.; **Junhyuk Park,** Samsung Electronics Co., Ltd.; **Youngsik Kim,** Samsung Electronics Co., Ltd.; **Seonil Brian Choi,** Samsung Electronics Co., Ltd.

[1069] Robust Verification of Clock Tree Network using "Clock Monitor" Integrated by ACRMG
Tejas Dipakkumar Dalal, Samsung Semiconductor India Research; **Giridhar S,** Samsung Semiconductor India Research; **Jeevan Nataraju,** Samsung Semiconductor India Research; **Garima Srivastava,** Samsung Semiconductor India Research

[1078] Real-time synchronization of C model with UVM Testbench
Kirtan Mehta, onsemi

[1084] Reset Sweep Verification for Elimination of Reset Domain Crossing Blind Spots in Design
Nitika Gupta, NXP Semiconductors; **Neha Srivastava,** NXP Semiconductors; **Vivek Yadav,** NXP Semiconductors

[1089] Register Access by Intent: Towards Generative RAL based Algorithms
Ahmed Allam, ICpedia

[1098] Achieving Full Liveness Proofs via a Systematic Assume-Guarantee Approach and Iterative Helper Generation
Stella Simic, Qualcomm; **Karthik Baddam,** Qualcomm

[1104] Formal and Simulation Methods Unite to Rescue the Damsel in Distress—Unclassified Faults
Siri Rajanedi, Analog Devices India pvt ltd; **Prashantkumar Ravindra,** Analog Devices India pvt ltd

[1112] Traversing the Abyss : Formal exploration of intricate state space
Sakthivel Ramaiah, Cadence Design System; **Tanishq Sharma,** Cadence Design System; **Craig Deaton,** Cadence Design System

[1134] Sleipnir: Bringing constraints and randomization to software defined data types
Nikhil Soraba, Microsoft; **Leon Cao,** Microsoft

12:30 – 13:30
Lunch
Room: Pine Cedar

SIEMENS

2024 Verification Trends Unveiled: Challenges, Surprises, and Siemens' Solutions

The verdict is in—our latest semi-annual verification survey reveals some startling trends, and the word to describe them is "alarming"! Join Harry Foster as he uncovers surprising insights that highlight the growing challenges in the verification world. Following his eye-opening overview, Siemens EDA experts Jean-Marie Brunet and Abhi Kolpekwar will share how Siemens is tackling these issues head-on with innovative flows and solutions. Don't miss this opportunity to learn how to navigate today's verification landscape and steer your projects toward success—all while enjoying lunch!

Presenters:
- Harry Foster, Chief Scientist Verification, Digital Verification Technology, Siemens EDA
- Jean-Marie Brunet, VP & GM, Hardware-Assisted Verification, Siemens EDA
- Abhi Kolpekwar, VP & GM, Digital Verification Technology, Siemens EDA

Organizers:
- Carole Dunn, Joe Hupcey III, Mathilde Karsenti (Siemens EDA)

Technical Program: Tuesday, February 25 (cont.)
Time Zone is PST

13:30 – 14:30

Industry Keynote: AI Factories Drive Re-invention of Chip Design, Verification, and Optimization
Room: Oak / Fir

Ravi Subramanian, Systems Design Group at Synopsys - Chief Product Management Officer
Artour Levin, AI Silicon Engineering at Microsoft Corporation - Vice President

Artificial Intelligence (AI) has transfixed the attention of the world and is infusing the electronics landscape from cloud-to-edge, including HPC, data center, PCs, smartphones, automotive, robots and many more devices. Architects and design teams are creatively producing AI engines that meet specific AI model and end-market application requirements. This new era of workload-specific AI accelerators necessitates new design, optimization, and verification strategies that must be performed in the context of the power and performance requirements of the end-market application. This new generation of customized chips driven by software workloads requires innovative, advanced and AI-assisted methodologies to ensure successful tapeouts in an increasingly complex, cost-driven, and fast time to value (TTV) environment. Hear from Synopsys and Microsoft how industry leaders are addressing these challenges from silicon to system and paving the way for further advancements in this new AI-driven era of pervasive intelligence.

13:30 – 18:00
Exhibit Hall Open
Room: Bayshore Ballroom

14:30 – 15:00
Coffee Break
Room: Gateway Foyer

15:00 – 17:00
Session 4: Portable Stimulus
Room: Monterey Carmel

Session Chair: **Santosh Kumar**

[1123] PSS and Protocol VIP: Like a Hand in a Glove
Bob Oden, Siemens EDA; **Tom Fitzpatrick,** Siemens EDA

[1085] Accelerating Device Sign-off through a Unified Environment for Design Verification, Silicon Validation and ATE with PSS
Maximilian Suckert, Advantest Europe GmbH; **Sergey Khaikin,** Cadence Design Systems, Inc.; **Arjun Ashok Vazhayil,** Qualcomm Technologies, Inc.; **Nandeep Devendra,** Qualcomm Technologies, Inc.; **Abhijeet Samudra,** Advantest America, Inc.; **Klaus-Dieter Hilliges,** Advantest Europe GmbH; **Moshik Rubin,** Cadence Design Systems

[1051] Performance verification for AI Heterogenous Multicore Systems using Portable Stimuli Standard
Pietro Locci, Synopsys; **Hillel Miller,** Synopsys

[1040] What Just Happened? Behavioral Coverage Tracking in PSS
Tom Fitzpatrick, Siemens EDA; **Wael Mahmoud,** Siemens EDA; **Mohamed Nafea,** Siemens EDA

Technical Program: Tuesday, February 25 (cont.)

Time Zone is PST

15:00 – 17:00

Session 5: AI & ML Coverage Closure

Room: Oak

Session Chair: **Kamel Belhous**

[1019] AFCML: Accelerating the Functional Coverage through Machine Learning within a UVM Framework

Syed Jawad Shah, National University of Science & Technology (NUST), Islamabad; **Majeed Ahmed,** National University of Science & Technology (NUST), Islamabad; **Muhammad Imran,** National University of Science & Technology (NUST), Islamabad; **Haroon Waris,** National University of Science & Technology (NUST), Islamabad; **Nasir Mohyuddin,** National University of Science & Technology (NUST), Islamabad; **Muhammad Mahboob Ur Rehman,** DreamBig Semiconductor

[1022] Reaching 100% Functional Coverage Using Machine Learning: A Journey of Persistent Efforts

Jaecheon Kim, Samsung Electronics Co., Ltd.; **Taewook Nam,** Samsung Electronics Co., Ltd.; **Wonil Cho,** Samsung Electronics Co., Ltd.

[1063] Stimulus Diversification and Coverage Closure of 3D NAND Flash with Artificial Intelligence

Goutham Pallela, Micron Technology, Inc.; **Peiyao Shi,** Micron Technology, Inc.; **Srinivas Deshmukh,** Micron Technology, Inc.; **Rohit Suvarna,** VerifAI Inc.; **Sandeep Srinivasan,** VerifAI Inc.; **Bill Hughes,** VerifAI Inc.; **Vaishnavi Venkatesh,** Micron Technology, Inc.

[1096] Functional Coverage Closure in SoC Interconnect Verification with Iterative Machine Learning

Jihye Kwon, Cadence Design Systems; **Sukwon Ha,** Samsung Electronics Co., Ltd.; **Youngsik Kim,** Samsung Electronics Co., Ltd.; **Seonil Choi,** Samsung Electronics Co., Ltd.; **Daeseo Cha,** Samsung Electronics Co., Ltd.; **Space Kim,** Samsung Electronics Co., Ltd.; **Kunhyuk Kang,** Samsung Electronics Co., Ltd.; **John Pierce,** Cadence Design Systems; **Amit Metodi,** Cadence Design Systems; **Saurabh Sharma,** Cadence Design Systems; **Heedo Jung,** Cadence Design Systems; **Yosinori Watanabe,** Cadence Design Systems

15:00 – 17:00

Session 6: Regression Management

Room: Fir

Session Chair: **Harish Patel**

[1065] A Scalable Gray-Box Instance-Based Reachability Predictor for Automated DV Regression Scheduling

Lorenzo Ferretti, Micron Technology; **Chinmaya Behera,** Micron Technology; **Surya Teja Bandlamudi,** Micron Technology; **Nihar Athreyas,** Micron Technology; **Vikram Narayan,** Micron Technology; **Samir Mittal,** Micron Technology

[1045] A Large Language Model-Based Framework for Enhancing Integrated Regression

Jin Choi, Samsung Electronics; **Noh Sangwoo,** Samsung Electronics

[1058] Automating Regression Triage in Design Verification Using AI-Based Random Forest Models

Lingkai Shi, AMD; Rohit Mathur, Amd

[1132] A Novel AI-ML Regression Flow for SoC verification

Sunil Shrirangrao Kashide, samsung semiconductor India(SSIR); **Narasimha Rao Chinni,** samsung semiconductor India(SSIR); **Garima Srivastava,** samsung semiconductor India(SSIR)

17:00 – 18:00

Reception

Room: Bayshore Ballroom

Technical Program: Wednesday, February 26
Time Zone is PST

9:00 – 10:00
Panel: Are AI Chips Harder to Verify?
Room: Oak / Fir

As AI chips evolve from specialized accelerators to complex heterogeneous systems, they present unique verification challenges: massive parallel computation units, dynamic data flow architectures, and intricate power management schemes. Additionally, verifying AI-specific features like numerical precision, training/inference modes, and complex memory hierarchies demands novel approaches.

This panel brings together verification experts from diverse industry segments to share their experiences and insights. Encompassing established semiconductor companies, Hyperscalers, innovative startups at different stages, and EDA technologists, our panellists will explore how different business models and market demands shape their verification strategies.

The panelists will debate key questions such as coverage metrics for AI workloads, verification reuse across multiple configurations, system-level aspects, and the balance between traditional verification methods –including functional verification, formal methods, virtual prototyping, and emulation - as well as the potential for AI-assisted approaches.

Panel Organizer and Moderator:

Moshe Zalcberg, CEO, Veriest Solutions

Panelists:

Harry Foster, Chief Scientist Verification, Siemens EDA (EDA)

Ahmad Ammar, Technical Lead, AIM (AI, Infrastructure, and Methodology), AMD

Stuart Lindsay, Principal HW EDA Methodology Engineer, Groq

Shahriar Seyedhosseini, Generalist Engineer, MatX

Shuqing Zhao, Formal Verification Lead, Meta

10:00 – 10:30
Coffee Break
Room: Gateway Foyer

10:30 – 12:00
Session 7: Formal Verification
Room: Monterey Carmel
Session Chair: **Vibarajan Viswanathan**

[1054] Automatic Test Pattern Generation Using Formal Verification and Fault Injection Methods
Jad Al Halabi, Infineon Technologies AG; **Endri Kaja,** Infineon Technologies AG; **Ecker Wolfgang,** Infineon Technologies AG

[1025] Hierarchical Formal Verification and Progress Checking of Network-On-Chip Design
Pritam Roy, NVIDIA; **Ping Yeung,** NVIDIA; **Joon Hong,** NVIDIA; **Abhishek Desai,** NVIDIA; **Aishwarya Raj,** NVIDIA; **Chirag Agarwal,** NVIDIA; **Dhruvin Patel,** NVIDIA

[1080] End-to-end Framework for Novel Datatype Arithmetic Verification
Qiuwen Lou, Amazon; **Bing Ji,** Amazon; **Stevo Bailey,** Amazon; **Deepak Shivaru,** ; **Nilabja Chattopadhyay,** Amazon.com LLC; **Sankalp Dayal**

Technical Program: Wednesday, February 26
Time Zone is PST

10:30 – 12:00
Session 8: UVM in Practice
Room: Oak
Session Chair: **Peter George**

[1086] Don't Go Changing: How to Code Immutable UVM Objects
William Moore, Paradigm Works

[1077] User Programmable Targeted UVM Debug Verbosity Escalation
Sam Mellor, Arm

[1119] Sequencer Containers - A Unified and Simple Technique to Execute Both Sequences and Virtual Sequences
Clifford Cummings, Paradigm Works, Inc.; **Mark Glasser,** Independent Consultant

10:30 – 12:00
Session 9: Coverage Modeling
Room: Fir
Session Chair: **Harry Foster**

[1083] Accelerating Pre-Silicon Verification Coverage with Transaction Sequence Modeling
Jayanth Raman, Micron, Inc.; **Jackson Wydra,** Micron, Inc.; **Ximin Shan,** Micron, Inc.; **Rahul Krishnamurthy,** Micron, Inc.; **Michael Yan,** Micron, Inc.; **Phyllis Hsia,** Micron, Inc.; **Vikram Narayan,** Micron, Inc.; **Samir Mittal,** Micron, Inc.

[1100] AI - accelerating coverage closure using intelligent stimulus generation
Jainender Kumar, Samsung Semiconductor India Research Bengaluru, India; **Ronak Bhatt,** Samsung Semiconductor India Research Bengaluru, India; **Garima Srivastava,** Samsung Semiconductor India Research Bengaluru, India; **Ashutosh Sinha,** Cadence Design Systems Pvt Ltd Noida, India; **Prashant Teotia,** Cadence Design Systems Pvt Ltd Noida, India

[1135] A Low-cost yet effective coverage model for fast functional coverage closure
Koushik Ramakrishnan, Nvidia corporation; **Roshan Paul,** Nvidia corporation; **Suresh M K,** Nvidia corporation; **Ajay Rupanagudi,** Nvidia corporation; **Tathagato Bose,** Nvidia corporation; **Guru Venkatesh,** guruv@nvidia.com; **Vaidyanathan Sambasivan,** Nvidia corporation; **Subodh Prabhu,** Nvidia corporation

12:00 – 13:00
Lunch & 2026 Announcement
Room: Pine Cedar

Technical Program: Wednesday, February 26 (cont.)

Time Zone is PST

13:00 – 14:00

Invited Keynote: The Role of EDA in U.S. Economic Security

Room: Oak / Fir

Robert Aitken, CHIPS R&D Office

CHIPS for America is a bipartisan program with the mission of strengthening America's economic and national security by revitalizing America's domestic semiconductor manufacturing and research and development ecosystem. U.S. leadership in chip design has made US companies dominant players in technologies ranging from smartphones to cloud computing to artificial intelligence. Underlying that success has been a strong and diverse electronic design automation (EDA) sector. This talk looks at the history of EDA and how it has enabled the semiconductor revolution, where it currently faces challenges, and how CHIPS for America and its CHIPS National Advanced Packaging Manufacturing Program is helping to address those challenges going forward.

13:00 – 18:30

Exhibit Hall Open

Room: Bayshore Ballroom

14:00 – 15:00

Poster Ninja Session

Room: Oak/Fir

15:00 - 15:30

Coffee Break

Room: Gateway Foyer

15:30 – 17:00

Session 10: Verification IP

Room: Monterey Carmel

Session Chair: **Bhaskar Vedula**

[1103] Expedite multi-die coherency verification through adaptive VIP subsystem

Jainender Kumar, Samsung Semiconductor India Research Bengaluru, India; **Sunil Shrirangrao Kashide,** Samsung Semiconductor India Research Bengaluru, India; **Garima Srivastava,** Samsung Semiconductor India Research Bengaluru, India; **Dimitry Pavlovsky,** Cadence Design Systems Pvt Ltd, USA; **Anunay Bajaj,** Cadence Design Systems Pvt Ltd Noida, India

[1120] Leverage Real USB Devices for USB Host DUT verification

Suchir Gupta, Synopsys Inc; **Amit Sharma,** Synopsys Inc

[1015] Design scheme for Emulator-friendly Memory Verification IP to Accelerate Simulation Performance

Sunghyeon Kang, SK Hynix; **Munsik Bae,** SK Hynix; **Jinsung Song,** SK Hynix; **Seokho Hong,** Siemens EDA; **Minsung Kang,** SK Hynix; **Sangkyoo Jeong,** SK Hynix

Technical Program: Wednesday, February 26 (cont.)

Time Zone is PST

15:30 – 17:00

Session 11: Testbench Generation
Room: Oak
Session Chair: **Cliff Cummings**

[1107] Guardians of the Chip: Mastering Next-Gen Security for SoCs and IPs

Sridevi Jagata, Cadence Design Systems; **Deep Mehta,** Cadence Design Systems; **Vishnu Prasad K V,** Cadence Design Systems

[1059] VerifLLMBench: An Open-Source Benchmark for Testbenches Generated with Large Language Models

Nishanth Somashekara Murthy, University of Minnesota, Twin Cities; **Eldon Nelson,** Synopsys; **Sachin Sapatnekar,** University of Minnesota, Twin Cities; **John Sartori,** University of Minnesota, Twin Cities

[1088] Test bench Framework for Fully Automated Register Tests of Numerous IPs in SoC

Wonyeong So, Samsung electronics; **Minje Kim,** Samsung electronics; **Jihye Lim,** Samsung electronics; **Sunil Roe,** Samsung electronics; **Youngsik Kim,** Samsung electronics; **Sunil Choi,** Samsung electronics

15:30 – 17:00

Session 12: Analog/Digital Mixed Signal
Room: Fir
Session Chair: **Jamie Ridgeway**

[1128] Catching the Elusive Voltage Spike with Analog/Mixed-Signal SVA/PSL Assertions

Charles Dancak, Betasoft Inc.

[1060] Addressing Advanced Mixed-Signal Verification Scenarios by Developing a UVM Framework for Analog Models

Simul Barua, Ulkasemi Inc.; **Henry Chang,** Designer's Guide Consulting, Inc.; **Shahriar Kabir,** Ulkasemi Inc.

[1057] Reuse of System-level Circuit Models in Mixed-Signal Verification

Bahaa Osman, Cirrus Logic; **Minghua Li,** Cirrus Logic; **Siddharth Maru,** Cirrus Logic; **Bhanu Singh,** Mathworks; **Eric Cigan,** Mathworks; **Suhas Belgal,** Mathworks

17:00 – 18:30

Reception & Best Paper Presentation
Room: Bayshore Ballroom

19:00 – 22:00

Exhibitor Clean Up
Room: Bayshore Ballroom

Technical Program: Thursday, February 27
Time Zone is PST

9:00 – 12:30
Next-Gen Verification Technologies for Processor-Based Systems
Room: Cascade

Today's complex processor-based systems enable technological advances in many market segments, such as AI, high performance computing, and automotive. However, verification of these systems introduces new challenges, spanning architectural verification of a custom RISC-V processor to memory coherency in a system containing thousands of Arm or RISC-V cores. As the complexity of the design increases, so does the need for new tools and methods beyond simulation and UVM testbenches.

In this tutorial, we will focus on RISC-V processors and present next-generation verification techniques that span the verification journey from a single RISC-V processor to complex systems with many RISC-V cores.

To accommodate the flexible and evolving nature of the RISC-V ISA, as well as privilege mode features, out-of-order pipelines, interrupts and debug mode, RISC-V processor verification requires innovation in stimulus generation, comparison, and checking. We will cover dynamic and formal approaches to verifying RISC-V cores, with topics including, but not limited to: ISA compliance verification and functional coverage, data path validation, functional verification of critical blocks, and security verification.

Multi-core designs introduce a new set of challenges, such as ensuring fair access to shared resources and cache and memory coherence. This tutorial will present solutions designed to address these issues and prevent costly bug escapes to silicon.

The size of multi-core designs and multi-processor SoCs means that a simulation-only verification strategy is impractical. Hardware-assisted verification becomes essential to ensuring correct operation in the multi-core designs of today and the future. This tutorial will demonstrate how Synopsys' next-generation processor verification tools and techniques combine with HAV platforms to create a powerful and effective solution.

Whether you are designers or verification engineers of these complex processor-based systems, you will walk away with new ideas on how to improve your verification flow by embracing these next generation solutions.

Ravindra Aneja, Synopsys Inc.

Xiaolin Chen, Synopsys Inc.

Aimee Sutton, Synopsys Inc.

Nilabja Chattopadhyay, Amazon.com LLC

Jevin Saju John, Synopsys Inc.

Bjoern Hartmann, Synopsys Inc.

(Will include presentations by Synopsys customers)

9:00 – 10:30

Beyond Integers and Floating Point – Designing and Verifying with Alternate Number Representations

Room: Donner

Speakers: **Russell Klein,** HLS Program Director, Siemens EDA

Many of the algorithms implemented in hardware have their foundations in mathematics and often have reference implementations in software programming languages. Mathematics generally uses real numbers (and sometimes imaginary numbers). Software and general-purpose computers typically use 32- or 64-bit integers and IEEE floating point representations. But for purpose-built hardware, supporting the full range and precision of these formats is not just unnecessary, it is wasteful in terms are area, power, and performance.

Examples of these types of algorithms can be found in image processing, audio processing, data communications including 5G and 6G, encryption, machine learning, data compression, and much more.

Algorithms are implemented in hardware, as opposed to simply being implemented in software and run on a general-purpose processor, specifically to improve their performance and power consumption. So as algorithms are implemented in hardware it is important to find an appropriate representation and understand the impact of that representation on the accuracy and precision of the algorithm, as well as the effect on the power, performance, and area (PPA) of the hardware implementation.

This workshop will cover a variety of numeric representations, including fixed point numbers, alternative floating-point formats like Google's "brain float," and exponential representations like "posits." It will examine rounding vs. truncation, overflow/underflow, and saturating math operations and their effects on the calculations. We will look at how to model algorithms using these alternate formats. And we will cover how to validate and verify both algorithmic implementations as well as Verilog or VHDL RTL, and how it fits into the overall verification process.

9:00 – 10:30

SoC development automation using IP-XACT 1685-2022 standard

Room: Siskiyou

Development of SoC is a flow involving several steps and many times there are multiple iterations to meet the design objectives and performance targets. This flow typically involves the following:

- Design intent definition by architects
- Handling CSR (Control and Status Registers), Memory Maps, Register banks, etc. Users usually define their register specifications in SystemRDL (an Accellera standard), spreadsheets, JSON, CSV, etc. Then they use EDA tools to convert these specifications into DV collaterals, firmware headers, documentation, etc., for the consumption of different teams in the SoC development flow.
- Design teams create RTLs for desired functionality manually from a feature specification. They also work on power specifications, clock synchronization, constraint analysis and timing closure. The same specification is used by other teams to create the verification testbench to verify the design, headers for firmware development, documentation for validation, etc. Any change in the specification during the process leads to iterations and sometimes rework.
- Reusing legacy IPs developed internally, mostly RTL, but also at other abstraction levels (TLM)

Using third party IPs (RTL and/or IP-XACT) from different vendors.

Different teams work on different aspects of SoC design dealing with different formats and a series of EDA tools. Finally, everything needs to be stitched together, integrated and assembled into the SoC which is then packaged and could be used in products inhouse or delivered to other product companies for further development and integration into a product.

Successful delivery of any SoC requires numerous exchanges of information and data (IPs) across inhouse teams of hundreds of engineers and vendors. It becomes important to standardize this exchange internally and externally for effective utilization of resources.

IP-XACT Workshop at DVCon US 2025 (cont.)

Standardized approach also creates scope for automation to further save upon development cycle time. IP-XACT, being an IEEE standard developed by Accellera, helps to standardize the SoC development flow. The latest version of IP-XACT (1685-2022) along with its rich set of TGI (Tight Generator Interface) API helps not only define standard structure of your design data but also allows programmability for automation using the TGI API.

10:30 – 11:00

Coffee Break
Room: Bayshore Foyer

11:00 – 12:30

Comprehensive Glitch Signoff – Learnings and experiences from industry use cases

Room: Donner

Vikas Sachdeva, Director of Product Strategy and Business Development at Real Intent

Introduction

Glitches are a common phenomenon in chip design, often deemed inconsequential due to their occurrence on synchronous paths, where Static Timing Analysis (STA) effectively mitigates them. However, specific scenarios within the chip design flow remain critically vulnerable to glitches, potentially causing catastrophic failures at the silicon level. These critical scenarios include clock domain crossing paths, interfaces between analog and digital domains, reset and clock paths, Design for Testability (DFT) paths, and paths spanning across power domains. Traditional methodologies struggle to detect and address glitches across such diverse scenarios comprehensively. This workshop introduces a holistic static methodology to achieve a thorough glitch signoff.

Summary of the content of the workshop

The session begins by delineating the glitch phenomenon, followed by a discussion on the existing chip design flow's limitations, which may overlook glitch issues, leading to silicon failures. The workshop will showcase actual glitch-induced design failures encountered by Real Intent's team, including:

- Glitches in asynchronous clock domain paths
- Glitches in reset paths
- Glitches in synchronous multi-cycle paths
- Glitches affecting DFT paths
- Glitches in power domain crossing paths and isolation signals
- Glitches at the digital-to-analog interfaces

We will provide a comprehensive analysis of these glitch types through detailed block diagrams, elucidating the identification, verification, and resolution processes for each glitch type. Drawing from these examples, we will develop a methodological framework that ensures a thorough glitch signoff.

Furthermore, the session will detail a signoff workflow that integrates static and formal analysis techniques to achieve a robust glitch pathway signoff.

Concluding with a compilation of Static Signoff best practices derived from industry insights and experiences, this workshop aims to empower participants to elevate verification practices within their organizations.

Intended Audience

This workshop is tailored for RTL Designers, Verification Engineers, SoC Designers, Chip Architects, and professionals involved in Clocks and Resets design and architecture, seeking to enhance their verification methodologies against glitches.

By attending, participants will gain invaluable insights into glitch analysis and signoff strategies, enriching the verification standards and practices in their respective fields.

11:00 – 12:30

CDC/RDC Interchange Format Standard

Room: Siskiyou

accellera SYSTEMS INITIATIVE

CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOC's having 2 trillion+ transistors and chiplet's having 7+ SOC's. Today CDC verification has become a multifaceted effort across the chips designed for clients, servers, mobile, automotives, memory, AI/ML, FPGA etc ... with focus on cleaning up of thousands of clocks and constraints, integrating the SV/\s for constraints in validation environment to check for correctness, looking for power domain and OFT logic induced crossings, finally signing off with netlist CDC to unearth any glitches and corrupted synchronizers during synthesis.

As the design sizes increased in every generation, the EDA tools could not handle running flat and the only way of handling design complexity was through hierarchical CDC-RDC analysis consuming abstracts. Also, hierarchical analysis helps to enable the analysis in parallel with teams across the globe. Even with all these significant progress in capabilities of EDA tools the major bottleneck in CDC-RDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools. Different vendor tool abstracts are seen because of multiple IP vendors, even in house teams might deliver abstracts generated with different vendors tools.

The Accellera CDC Working-Group aims to define a standard CDC-RDC IP-XACT model to be portable and reusable regardless of the involved verification tool.

As moving from monolithic designs to IP/SOC with IPs sourced from a small/select providers to sourcing IPs globally (to create differentiated products), the quality must be maintained as driving faster time-to-market. In areas where the standards (SystemVerilog, OVM/UVM, LP/UPF) are present, the integration is able to meet the above (quality, speed). However, in areas where standards (in this case, CDC-RDC) are not available, most options trade-off either quality, or time-to-market, or both :-(Creating a standard for inter-operable collateral addresses this gap.

This workshop aims to remind the definitions of CDC-RDC Basic Concepts and constraints, as well as the description of the reference verification flow, and addressing the goals, scope & deliverables of the Accellera CDC Working Group in order to elaborate a specification of the standard abstract model.

Presenters:

- **Bill Gascoyne,** Blue Pearl Software
- **Ping Yeung,** Nvidia
- **Chetan Choppali Sudarshan,** Marvell
- **Don Mills,** Microchip Technology
- **Anupam Bakshi,** Agnisys
- **Farhad Ahmed,** Siemens EDA
- **Iredamola Olopade,** Accellera