

Accellera, Standards, and Semiconductor Supply Chain

Lu Dai Accellera Chair



Lu Dai - Bio

Lu Dai is a Senior Director of Technical Standards at Qualcomm Technologies, Inc., spearheading semiconductor standards efforts and relationships with industry organizations.

Lu was previously Senior Director of Engineering and led Qualcomm's SOC design verification team and front-end methodologies and initiatives. He was also the Design Verification Lead responsible for multiple generations of premium tier platforms at Qualcomm, including the Snapdragon 8 series and products that power the Mars Perseverance rover and Ingenuity helicopter.

Prior to Qualcomm, Lu was the Design Verification Lead for Cisco's Gigabit Switching Business Unit where he worked on multiple generations of Cat4k ASICs.

Lu is the current Chair of Accellera, Chairman of the RISC-V International Board of Directors and serves on the Board of Directors at Si2.

Lu holds a Master's degree in Electrical Engineering from Cornell, and a Bachelor's in Electrical Engineering and Computer Science from UC Berkeley.







Accellera History

- Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry.
- Accellera supports a mix of user and vendor standards and open interfaces development in the area of electronic design automation (EDA) and intellectual property (IP).
- Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera are contributed to the IEEE for formal standardization and ongoing governance.

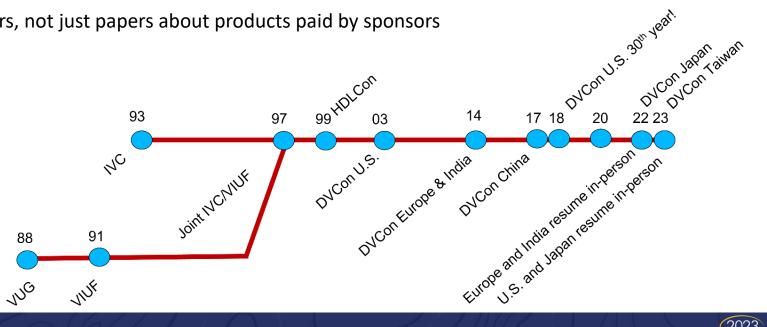
- 1991: Open Verilog International (OVI) and VHDL International (VI) founded separately
- 2000: OVI and VI merged to form Accellera Organization
- 2009: Accellera merged with The SPIRIT Consortium
- 2011: Accellera merged with Open SystemC Initiative (OSCI) and changed its name to Accellera Systems Initiative
- 2013: Accellera acquired Open Core Protocol (OCP) standard, the intellectual property of the OCP International Partnership (OCP-IP)





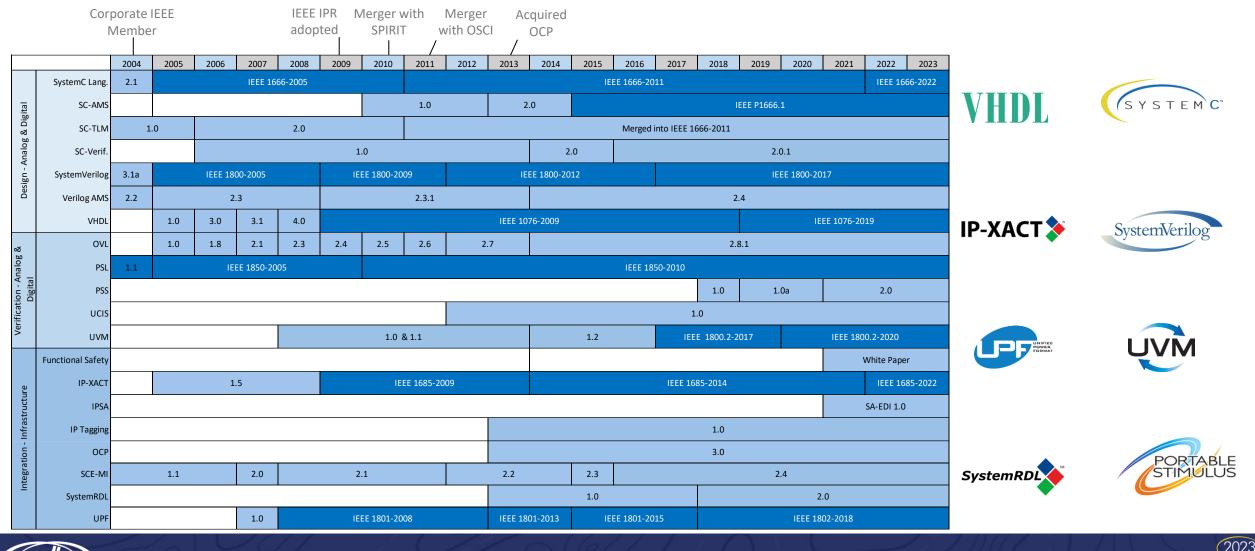
DVCon History

- Accellera has been successfully sponsoring Design & Verification Conference & Exhibition in the US for 35+ years
- Original events had different names and were tied to VHDL International and Open Verilog International ٠
- Eventually VHDL and Verilog-focused groups merged into a single conference and became DVCon in 2003 •
- Global expansion started in 2014: DVCon Europe, DVCon India, DVCon China, DVCon Japan, and DVCon Taiwan •
- Every DVCon has a similar "Look & Feel" with a focus on user contribution •
 - Papers written by and presented by users, not just papers about products paid by sponsors ٠
 - Panel sessions on current hot topics ٠
 - Tutorials related to relevant standards •





Accellera Standards



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CONFERENCE AND EXHIBITIC TAIWAN



2023/9/7

Accellera-IEEE Collaboration

IEEE

- <u>VHDL</u> or IEEE 1076 or IEC 61691-1-1
- <u>Verilog</u> or IEEE 1364 or IEC 61691-4
- Delay and Power Calculation System (DPCS/OLA: <u>Standard Parasitic</u> <u>Exchange Format</u>) or IEEE 1481
- Standard Delay Format (SDF) or IEEE 1497 or IEC 61523-3
- Open Model Interface (OMI) or IEEE 1499
- Open Compression Interface (OCI) or IEEE 1450.6.1
- Advanced Library Format (ALF) or IEEE 1603 or IEC 62265
- <u>SystemC</u> or IEEE 1666
- SystemC Analog/Mixed-Signal extensions or IEEE 1666.1
- <u>IP-XACT</u> or IEEE 1685
- <u>SystemVerilog</u> or IEEE 1800
- <u>Unified Power Format</u> (UPF) or IEEE 1801
- <u>Universal Verification Methodology</u> (UVM) or IEEE 1800.2
- <u>Property Specification Language</u> (PSL) or IEEE 1850 or IEC 62531

Accellera

- <u>IP Security Assurance</u> (Security Annotation for Electronic Design Integration (SA-EDI))
- <u>Open Core Protocol</u> (OCP)
- Open Verification Library (OVL)
- Portable Test & Stimulus Standard (PSS)
- <u>Standard Co-Emulation-Modeling Interface</u> (SCE-MI)
- <u>Soft IP Tagging</u>
- <u>SystemRDL</u> (System Register Description Language)
- <u>Unified Coverage Interoperability Standard</u> (UCIS)
- <u>Verilog-AMS</u> (Analog Mixed-Signal)





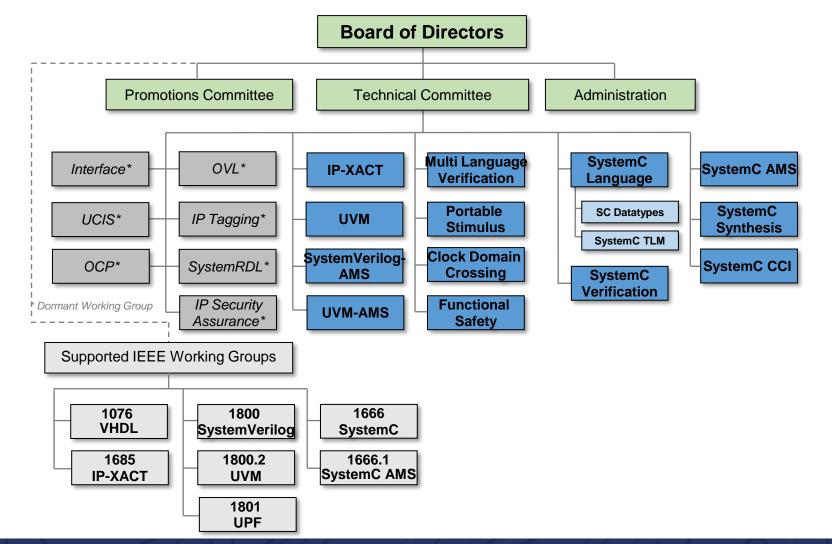


Accellera Members





Accellera Activities



| System/Design – | | Verifi | ation – | | |
|---|------------|------------------|----------|----------|--|
| Analog & Digital | | Analog & Digital | | | |
| SystemC | | UVN | A UVM-A | MS | |
| TLM/CCI/Synthesis | | | UVM-Sys | stemC | |
| SystemC-AMS | Working | | Portable | | |
| SystemVerilog | | Groups & | | Stimulus | |
| SV-AMS/V-AMS | Standards | | Multi-La | anguage | |
| | | | OVL | UCIS | |
| | | | 2. | | |
| Integratio | on – | | | | |
| Infrastruc | ture Clock | Comain C | Crossing | | |
| IP Security Assurance Functional Safety | | | | | |

IP-XACT SCE-MI IP Tagging OCP SystemRDL





Sy

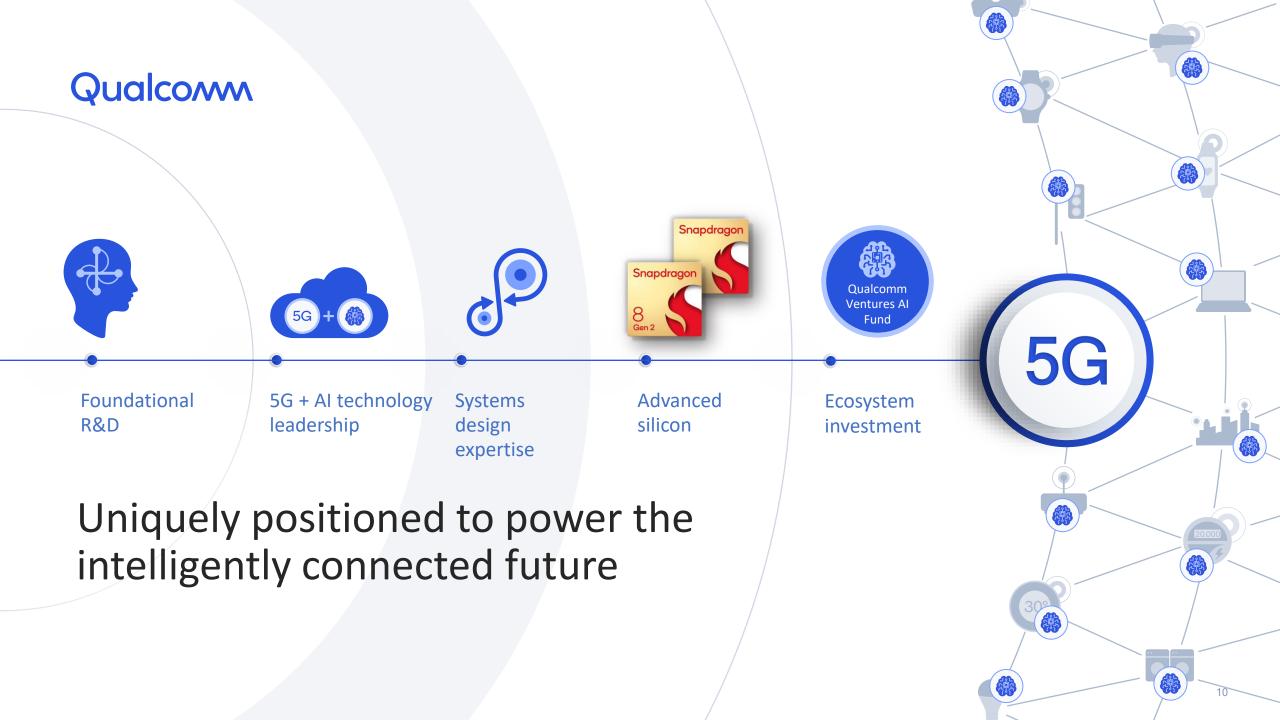
SV-

Years of driving the evolution of wireless

#1

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Fabless semiconductor company



We participate in

standards and industry organizations

Qualcom

What are standards?

- Regulations
 - "mandatory"
- Standards
 - Voluntary
 - In some parts of the world, developed by a formally recognized standards body
 - i.e., in Europe: CEN, CENELEC, or ETSI
 - In US, developed by an ANSI accredited standards body
- Specifications





Voluntary Consensus Standards

- Voluntary Consensus Standards Body US OMB A.119 Requirements
 - i. Openness
 - ii. Balance
 - iii. Due process
 - iv. Appeals process
 - v. Consensus

- OpenStand Principles
 - i. Due process
 - ii. Broad consensus
 - iii. Transparency
 - iv. Balance
 - v. Openness

- Adherence to these facilitates competition and reduces anti-trust concerns
- Similar rules are codified in the WTO (World Trade Organization) TBT (Technical Barriers to Trade) Agreements
 - "technical regulations", "conformity assessment procedures", and "standards" are not prepared, adopted or applied with a view to, or with the effect of, creating **unnecessary** obstacles to international trade.
 - However, allow some carve out for "inter alia: national security requirements; the prevention of deceptive practices; protection of human health or safety, animal or plant life or health, or the environment."



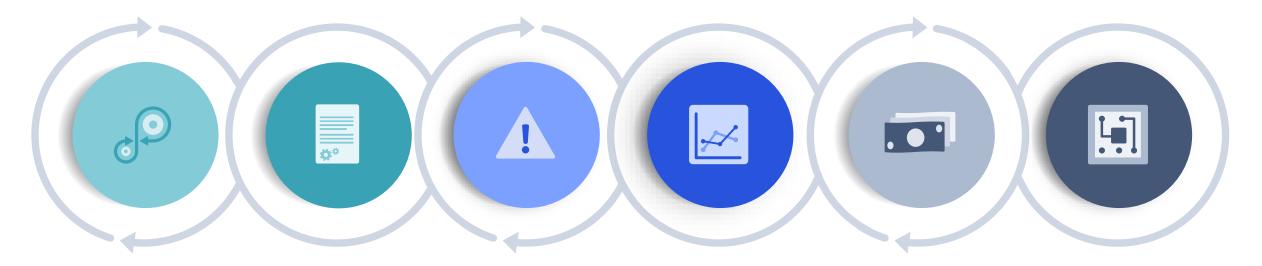
Patents: SEPs and FRAND

- SEP Standards Essential Patent
- FRAND (also RAND) Fair Reasonable and non-Discriminatory
- RF Royalty Free
- LoA Letter of Assurance
 - Letter of commitment to license SEPs under SDO IP policy
- Patent Declarations
 - Indicate SEPs
 - Often the terminology is considered interchangeable with LoA, but actual usage depends on the actual text used in the IP Policy itself





Our industry is based on technology standards



Ensuring system interoperability

while enabling product differentiation and spurring transparent industry competition

Meeting regulatory requirements

test and certification procedures are developed to aid in meeting obligations

Reducing market risk

especially in areas of large investments (e.g., 5G infra)

Creating new markets

and expanding addressable markets of existing products and technology

Lowering cost

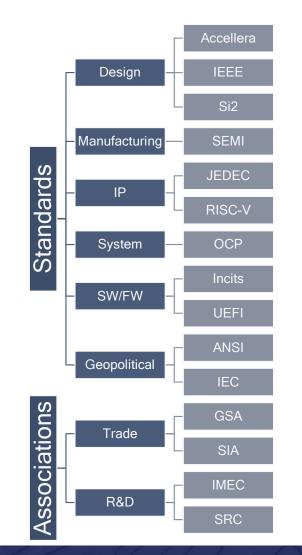
through economies of scale and multivendor sourcing

Improving technology

multiple companies participate, collaborate, compete – best prevails

Standards create significant value for the technology ecosystem

What are semiconductor standards







2023

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What is semiconductor supply chain

- [From Investopedia] A supply chain is a network of individuals and companies who are involved in creating a product and delivering it to the consumer. Links on the chain begin with the producers of the raw materials and end when the van delivers the finished product to the end user.
- Supply chain management is a crucial process because an optimized supply chain results in lower costs and a more efficient production cycle. Companies seek to improve their supply chains so they can reduce their costs and remain competitive.
- The semiconductor <u>supply chain</u> refers to the network of companies involved in their design, manufacturing, testing, packaging, and distribution. The supply chain is complex, involving the coordination of a number of different stages, from sourcing parts and materials to the sale to the final end user.





Supply Chain Challenges



What changed?

Covid Geopolitical events



How bad?

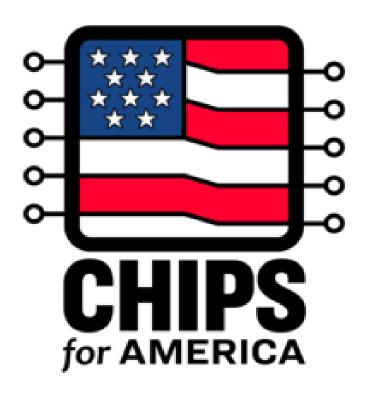
Supply chain constrain Supply chain disruption

- Supply chain rewire
 - Reliability (quality)
 - Security (safety)
 - Resiliency (risk management)
 - Diversity (options)
 - Sustainability (time)





CHIPS Act(s) and Rise of National Standards



- The CHIPS and Science Act of 2022 calls for a 5yr \$52.7B congressional funding to revitalize United States semiconductor industry
- There are international CHIPS Act in the work as well, including EU (€43B), South Korea (15-25% tax deduction), and Taiwan (NT\$6B), among others
- MIIT released a proposal to establish a new "National Integrated Circuit Standardization Technical Committee." The committee would research, develop, and revise standards for all types and components of semiconductors, including integrated circuit materials and equipment, semiconductors, integrated circuit module, integrated circuit chips, and microelectromechanical systems (MEMS)





A New Hope



While countries want disengagement for supply chain security, the world wants interdependency for preserving peace A semiconductor détente?

International standards help ensure interoperability of an interdependent ecosystem



Supply chain interdependency = a new foundation for world peace





Questions





