2024
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
JAPAN

August 29, 2024

CONFERENCE **PROCEEDINGS**

accellera
SYSTEMS INITIATIVE

DVCon Japan 2024
Steering Committee
updated 2024/8/12

目次

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DVCon Japan 2024 実行委員長
株式会社アドバンテスト 田中玄一

DVCon Japan 2024にようこそ！

DVConは米国では20年以上もの歴史を持つカンファレンスですが、昨年の対面形式での開催に続き今年も対面で開催できることとなりました。

DVConの歴史を紐解くと、1980年代に開催されていたVHDL User Groupや、その後のOpen Verilog Internationalにまで遡ります。当時も今も変わらず、言語仕様を学習することは大事ですが、それだけでは設計や検証を効果的に進めることはできません。さまざまな記述方法に起因する異なるメリットやデメリットについて、後工程も含めた評価と実践的な体得が不可欠です。それを業界として効率良く学ぶことを目的として発展してきたコミュニティから、2003年にDVCon - Design and Verification Conferenceが立ち上がりました。それまでのHDL設計だけでなく、極めて重要な課題である機能検証やその他多くの技術的な側面を取り上げたカンファレンスです。現在はIEEE標準であるSystemVerilogやUVM、UPF、フォーマルメソドロジ、Portable Stimulus、 IP-XACT、SystemC、機能安全、セキュリティ、AI/MLの適用など、議論する分野も多岐にわたります。そしてこれらは個別に議論されるのではなく、互いが複雑に絡み合うクロスドメインの課題として議論されています。

このような背景を持つDVConは米国はもとより、2014年にはヨーロッパ、インド、そして2017年には中国で開催される国際的なカンファレンスとして発展してきました。そして長く待たれていたDVCon Japanは2022年に始まり、今年で３回目の開催となります。

多くの技術者や管理者の方々が、さまざまな論文やチュートリアルによって多くのことが学べる場となるように、また技術者どうし、聴講者と講演者、Accelleraの代表らとの交流の場となるよう願っています。DVCon Japan 2024ではGoldスポンサー4社、Silverスポンサー7社、サポーター2社による多くのご支援を賜り、誠にありがとうございます。またアカデミアから協賛いただいております情報処理学会、IEEE CEDA AJJC、電子情報通信学会の方々にも、この場をお借りして厚く御礼申し上げます。

カンファレンスに加えて展示会も開催いたします。今年は日本、アメリカ、イギリス、フランス、アイルランド、ドイツ、インド、中国の各国から19社に出展いただいております。今年から展示会のみ無償で参加できる登録も追加いたしましたので、この機会をご利用ください。

また基調講演といたしまして、日本経済新聞社の太田泰彦様より「半導体が世界を回す～業界を取り巻く国際情勢と安全保障～」と題しましてご講演いただきます。

是非ともDVCon Japan 2024にご参加ください。皆さまとともに有意義なカンファレンス体験ができますことを楽しみにしております。

CONFERENCE SPONSOR

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Accelleraは幅広いメンバーで構成されており、偏りなくオープンです。世界中のエレクトロニクス産業に利益をもたらす技術標準を開発するための技術委員会の活動を全面的にサポートしています。

世界中の企業や半導体メーカーは、民生機器、モバイル機器、ワイヤレス機器、自動車機器、その他の「スマート」な電子機器を開発するために、幅広いプロジェクトや応用分野でIEEEの電子設計自動化（EDA: Electronics Design Automation）技術や知的財産（IP=Intellectual Property）標準を使用しています。AccelleraはIEEEとの継続的なパートナー関係にあり、Accelleraが開発した標準や技術的な実装がIEEEに寄贈されることで正式な標準化と継続的なガバナンスを実現しています。

Accellera Systems Initiativeのミッション

Accelleraのミッションは、エレクトロニクス製品の設計・検証の生産性を向上させるグローバルスタンダードを提供し、エレクトロニクス業界が協力してイノベーションを起こせるようなプラットフォームを提供することです。その目的とするところは次のとおりです。

- システム、半導体、IP、設計ツール企業が必要とする設計・検証標準を提供し、フロントエンドの設計自動化プロセスを強化する
- 企業、個人、組織のコミュニティと協力し、商用 IC、EDA 製品、組込みシステムソリューションの設計コストを低減し、世界中の設計者の生産性を向上させる標準を提供する
- システムレベル、RTレベル、ゲートレベルの設計フローを包含する次世代EDAとIP標準の利用可能性と採用を促進する
- 電子設計コミュニティと協力して設計者の生産性を向上させ、製品開発コストを低減させる標準を提供する
- SystemC、Universal Verification Methodology (UVM)、IP-XACTを含むAccellera Systems Initiativeユーザ・コミュニティの継続的な成長を可能にする仕組を提供する
- IEEEを通じてAccellera Systems Initiativeが開発した技術的な実装を標準化する

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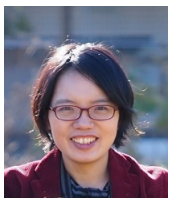

Shiho Hagiwara
TSMC Design
Technology Japan

Marketing Chair
Akio Mitsuhashi
EE Tech Focus

DVCon Japan 2024 Program

Time	Hall A
	General Sessions
8:50-9:00	DVCon Japan 2024 実行委員会委員長挨拶
9:00-9:30	Accellera Systems Initiative Overview / Technical Committee Update
9:30-10:30	Keynote:「半導体が世界を回す」~業界を取り巻く国際情勢と安全保証~

Time	Hall A	Conf E
	Tutorial Session	
10:30-11:20	T1 - Cadence Is AI the “magic bullet” for solving the growing IP and SoC verification challenges ?	T2 - Accellera CDC Working Group Standardizing CDC and RDC abstract models

Time	Hall A	Hall I
11:20-11:40	***Break for Lunch***	***Exhibition***
11:40-12:30	Siemens EDA Luncheon Session Verification methodologies for high-level synthesis, considering the contrast between RTL design and high-level design	

Time	Conf E	Conf F	Conf G	Conf H	Hall I
	Paper Presentation				***Exhibition***
12:30-13:00	PP1 Verification Technique	PP2 SystemVerilog / UVM	PP3 Automotive	PP4 Protocol Verification	
13:00-13:30					
13:30-14:00				PP5 New Language	
14:00-14:30	***Coffee Break***				

Time	Conf E	Conf F	Conf G	
	Paper Presentation			
14:30-15:00	PP6 DSP and HLS	PP7 Formal Verification & Security	PP8 Power & Performance	
15:00-15:30				
15:30-16:00	***Coffee Break***			***Exhibition***
	Tutorial Session			
16:00-16:50	T3 - Steering Committee Portable Stimulus Standard Update	T4 - Siemens EDA Introducing Smart Verification Unleashing the Potential of AI Within Functional Verification	T5 - Steering Committee SA-EDI Update	
16:50-17:40	T6 - Art-Graphics A Subjective Review on IEEE Std 1800-2023	T7 - Synopsys Low Power Verification Using Formal Technology	T8 - Codasip The way we walk around RISC-V	
	Networking and Exhibition			
17:40-20:20				***Networking & Exhibition***

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2024 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION JAPAN

General Session

9:00-9:30 / Hall A

Accellera Systems Initiative Overview Technical Committee Update

Accellera Systemc Initiative Chairman, Lu Dai
Technical Committee Chair, Martin Barnasconi

Accellera Systems Initiative は、世界中のエレクトロニクス業界が使用するシステムレベル設計やモデリング、および検証のための標準規格を開発、サポート、推進し、さらに促進させるための独立した非営利組織です。このセッションではチェアマンを務めるLu Daiからのオーバービュー、そしてテクニカルコミッティーのチェアを務めるMartin Barmasconiから、チュートリアルでは扱っていない標準化活動を中心に最新情報をお伝えします。

9:30-10:30 / Hall A

基調講演
半導体が世界を回す
～業界を取り巻く国際情勢と安全保障～

日本経済新聞社
太田 泰彦

米中両大国の対立が深まり、半導体は国家安全保障のカギを握る戦略物質となった。米国が中国の技術進歩を阻止しようと強力な対中輸出規制を打ち出す一方、中国は製造から設計、素材、製造装置に至るまで関連するあらゆる製品の国産化を急ぐ。台湾有事が視野に入る中で、米国、中国、欧州、台湾、韓国、日本は、それぞれサプライチェーンの要所を支配下に置く国家戦略を競い始めた。日本の政府、企業、エンジニアが進むべき道を、地政学的な観点から考察する。

Tutorial Session

Tutorial T1 10:30-11:20 / Hall A

Is AI the “magic bullet” for solving the growing IP and SoC verification challenges ?
(AIは増大するIPおよびSoC検証の課題を解決する「特効薬」なのか？）

Cadence Design Systems
System Verification Group, Nick Heaton

IP and SoC Verification challenges continue to grow with complexity and multi-chiplet systems, explores the need for HW and SW solutions for the range of use-cases and explains the challenges and introduces solutions focusing on how AI may or may not help.
IP および SoC 検証の課題は、複雑性とマルチチップレット システムの拡大とともに増加し続けており、さまざまなユース ケースに対する HW および SW ソリューションの必要性を探り、課題を説明し、AI がどのように役立つか、または役立たないかに焦点を当てたソリューションを紹介します。

Tutorial T2 10:30-11:20 / Conf E

Standardizing CDC and RDC abstract models
（CDCとRDCの抽象モデルの標準化）

Accellera Systems Initiative - CDC Working Group
Agnisys CEO, Anupam Bakshi

This session will provide a basic understanding of CDC and RDC issues, and will cover the CDC verification possible at RTL, as well as assertion-based verification in CDC. We will also discuss the concept of hierarchical flow in CDC and RDC, the need for it, and ideas for its implementation, as well as the activities of the various subgroups that are currently working on it, and milestones towards the final LRM.
このセッションではCDCやRDCの問題について基本を理解し、そしてRTLで可能なCDC検証、またCDCにおけるアサーションベース検証について解説します。またCDCとRDCにおける階層的なフローの概念とその必要性、実現アイデアについても触れ、それに対して現在活動が行われているさまざまなサブグループのアクティビティ、最終LRMに向けてのマイルストーンなどについてお伝えしようと思います。

Luncheon Session

11:40-12:30 / Hall A

RTL設計と高位設計の対比から考察する高位合成向けの検証手法
(Verification methodologies for high-level synthesis, considering the contrast between RTL design and high-level design)

Siemens EDA
山本修作

今年は、1994年に初の商用高位合成ツールが発表されてから30年目の節目の年に当たります。日本の大手各社では、その10年後に世界に先駆けて高位合成ツールの導入が始まり、更にその10年後には欧米でも同様の動きがありました。
つまり、高位合成の導入からは既に10-20年が経とうとしているわけですが、検証についてはRTL設計時代からどのように推移してきたでしょうか。
このセッションでは、はじめに従来のRTL設計時と対比しながら、高位合成フローの検証を整理します。次に一例として、Siemens EDAが提供するCatapult High Level Design Platformにおける検証手法とツールの機能を紹介したうえで、高位設計時の検証効率化に向けた今後の方向性について皆さんといっしょに考えてゆきたいと思います。

This year marks the 30th anniversary of the first commercial high-level synthesis tool in 1994. Ten years later, major Japanese companies began to introduce high-level synthesis tools ahead of the rest of the world, a further decade later, similar developments took place in Europe and the USA.In other words, 10-20 years have already passed since the introduction of high-level synthesis.How has verification evolved since the era of RTL design?
In this session, firstly, the verification of high-level synthesis flow will be organized in comparison with the conventional RTL design.
Next, as an example, we will introduce the verification methods and tool functions of the Catapult High Level Design Platform provided by Siemens EDA, and discuss the future direction to improve verification efficiency in high-level design flow with you.

Thank you to the Luncheon Sponsor

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ICをはじめとしたシリコンシステムと電子システムの設計開発に携わるすべての技術者のためのテクニカルイベント

よりスマートな未来をエンジニアリング。シーメンスEDAとともに

Siemens EDA Tech Forum 2024 Japan

Siemens EDA Tech Forumは、品質、安全性、信頼性の要件に応えつつ、進化を続けるテクノロジ、デザインの高密度化や複雑化、その他さまざまな設計課題に取り組む、シリコンシステムや電子システムの設計／開発に携わるすべての皆様と、最新の技術動向や事例、課題解決策を共有し合い、持続可能なビジネスの実現に向けた知見とネットワークを深めていくことを目指すテクニカル・イベントです。

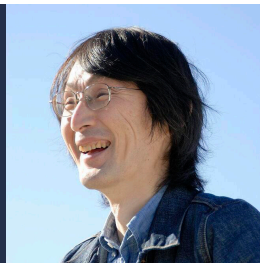
3D IC、チップレット、AIやML（機械学習）用チップ、ICパッケージングといった先端分野の設計技術や手法から、プリント基板（PCB）を基軸とする電子システムの設計、解析、エレメカ連携などのマルチドメインでの協調開発、デジタルスレッドを活用した社内外におけるエコシステム構築まで、幅広い分野を取り上げます。ぜひ、ご参加ください！

Siemens EDA Tech Forum 2024 Japan
2024年9月6日（金）10:00 - 20:00（受付: 9:30 ～） | 東京コンファレンスセンター・品川
プログラムの詳細と参加登録はこちらから: https://go.sw.siemens.com/rYxVejOL

新たな価値創出を提言するジェネラルセッション

基調講演: 夢を形に - システム設計新時代の幕開け
マイク エロー（Mike Ellow）
CEO, シーメンスEDA シリコンシステムズ, シーメンスデジタルインダストリーズソフトウェア

特別講演: Preferred Networksにおけるプロセッサー開発
牧野 淳一郎氏
VP コンピュータアーキテクチャ担当 CTO, 株式会社Preferred Networks



業界エキスパートによる事例紹介

- 株式会社Preferred Networks
- Rapidus株式会社
- アルプスアルパイン株式会社
- キヤノン株式会社
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- 三菱電機株式会社
- ルネサスエレクトロニクス株式会社
- シーメンスデジタルインダストリーズソフトウェア　（順不同）

最新技術と顧客事例を織り交ぜた3つのテクニカルトラック

- IC（集積回路）を含むシリコン設計、検証、製造
- PCB（プリント基板）を基軸とした電子システムの設計と製造
- 3D IC / チップレット / ICパッケージング設計

情報交換と交流の場

シリコン設計から電子システム設計に携わるエンジニアやマネージャーがそれぞれの知見を交換できる交流の場をご用意。レセプションでは、素敵なプレゼントが当たる抽選会も！

※ プログラムの内容は予告なく一部変更になる場合がございます。
あらかじめご了承ください。

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Paper Presentation - 1

PP1 : Verification Technique | 12:30-14:00 @Conf E
Session Chair : Yoshinari Ojima, Toshiba Electronoic Device & Storage

PP1.1 (12:30-13:00)

Quality Driven Analysis of Clock Tree Network using "Accelerated Clock Reference Model Generator"

Tejas Dipakkumar Dalal, Giridhar S, Jeevan Nataraju, Garima Srivastava
Samsung Semiconductor India Research

Clock tree network (CTN) is one of the complex design structures in SOC that controls clock supply for all the synchronized logic on the chip. It constitutes numerous clock component instances to employ Dynamic Voltage Frequency Scaling (DVFS) and Clock Gating (CG) schemes, effectively contributing to overall performance and power optimization. Ensuring verification of such a network with legacy methodology is demanding, inconsistent and mostly restricted. This paper presents a holistic verification strategy for CTN with clock reference model (CRM) that encompasses all the clock components of the network under verification. The CRM generation is automated using "Accelerated clock reference model generator" (ACRMG). It is an in-house developed tool, modelled with a custom algorithm to trace clock tree path for each IP in SOC and generate the CRM. It is a single click solution that makes it adaptable for frequent design changes during the chip development cycle. The proposed solution is validated with mobile and automotive SOCs having multi-die/chiplet-based architecture. With ACRMG, the overall TB environment setup time is reduced from 2 days to less than 1 day resulting in faster bug resolution.

PP1.2 (13:00-13:30)

Data integrity checker for Coherency Verification

Priyanshu Somvanshi, Shubhanshu Jain, Vaibhav Ashtikar
Google

Coherency verification is a crucial aspect of chip verification. It involves checking data integrity across various components such as caches, buffers, interconnects etc. The variety of transaction protocols and protocol conversions across multiple interfaces presents new challenges for data integrity checks.
This paper proposes a novel approach for data integrity verification using interface monitors (trackers) and a post-processing tool. The approach validates data integrity at every stage of execution. The tool aids in debugging data consistency issues by pinpointing the exact time when inconsistencies occurred. Memory models are built on each interface using this approach, enabling the verification of memory signatures across different verification environments, such as emulation versus SoC verification and across projects.
Post-processing reduces the simulation time consumed for verification runs and facilitates statistical analysis in regressions. The data integrity checker can be an integral part of any verification methodology, spanning subsystem, SoC level, and emulation.

PP1.3 (13:30-14:00)

Hardware/Software co-design and co-verification of embedded systems

Mayank Nigam, Nikita Gulliya
Agnisys Technologies Pvt. Ltd, India

As hardware chip complexity continues to increase, these chips are frequently utilized as targets in Initiator-Target Architectures, where the targets are commonly referred to as custom peripheral IPs. The initiator can write to and read from these peripherals. While silicon companies provide functionality and register information in their datasheets, they often overlook validation from the programmer's perspective—the ones who develop software to control these IPs. In embedded systems, programmers write software into the processor's program memory to interface with external devices and manage peripheral hardware pins, tailored to real-world applications. Therefore, it is crucial for silicon vendors to adopt a comprehensive approach to design, verify, and validate these peripheral IPs. This paper presents methodologies for the co-design, verification, and validation of hardware and software. Entire process will be demonstrated through detailed examples.

Paper Presentation - 2

PP2 : SystemVerilog / UVM | 12:30-14:00 @Conf F
Session Chair : Takahide Yoshikawa, Fujitsu

PP2.1 (12:30-13:00)

Solving Memory Configurations Challenge with SV-Rand Verification Flow

Kaushal Vala, Krunal Kapadiya, Joseph Bauer, Shyam Sharma,
Dharini SubashChandran, Ritesh Desai, Pooja Patel, Vatsal Patel
Cadence Design Systems, Ahmedabad, India

Cadence Memory Models use configuration files to uniquely describe the characterization attributes of every legal and real memory device described in protocol standards and vendor data sheet. The Memory Model performs timing checks and protocol responses according to the combination of attribute settings in each device file. As the number of these memory device configurations increases per memory type, a significant challenge arises for the EDA provider and for the design verification engineers using them. Memory part offerings even within one protocol have increased into the tens of thousands while the number of characterization attributes describing a memory and the dependencies between them increases with each protocol generation. Moreover, the set of memory part offerings and attributes evolves over many version updates of the protocol standard and vendor data sheets during user's product development. The EDA provider is challenged to provide and maintain accurate updates for all the evolving real part configurations. In conjunction, the user's challenge is to validate that their SoC's memory sub-system is compatible across the applicable memory part variations their SoC can externally connect to. To ensure compatibility as evolving updates are taken at regular intervals, the user has had to repeat their process steps to manage their repository snapshot of configurations while incorporating them into their test environment's part selection and coverage tracking.
A new widely adopted solution is available that represents all parts as one class file while simplifying the selection and coverage scoping to the right level of memory differentiating attributes aligned to the specification, vendor, and application. This "SystemVerilog constraint random configuration (SV-Rand)" flexible solution represents all valid parts in a single SystemVerilog class of constraints which resolves evenly across user's application scope of required configurations, while simultaneously providing compatibility coverage for closure over that same scoped set of parts. This constraints class, representing the relational intersection of all configuration settings relative to these memory differentiating attributes, is auto generated from a human friendly form for ease maintaining specification alignment. Additionally, Auto-Config layer in memory subsystem is an automated and scalable solution to reduce verification efforts, achieve faster time to market with no silicon escape.

PP2.2 (13:00-13:30)

Having Your Cake and Eating It Too - Programming UVM Sequences with DPI-C

Rich Edelman, Tomoki Watanabe
Siemens EDA

Blending SystemVerilog UVM and SystemVerilog DPI-C is a powerful way to create or reuse pre-existing verification environments. This paper describes the mechanisms and methods and syntax needed, including writing tasks and functions in both the SystemVerilog interface and the UVM sequences.

PP2.3 (13:30-14:00)

Maximizing Verification Productivity Using UVM and Dynamic Test Loading

Masayuki Masuda
Renesas Electronics Corporation

Verification engineers involved in debugging tests are always interested in improving verification productivity. To achieve this, UVM enables verification interoperability within companies and throughout the electronics industry. In addition, Dynamic Test Loading (DTL), including Save/Restore (S/R), reduces compile and run time.
In order to maximize verification productivity, we have established a simplified and standardized architecture for applying UVM and DTL. The results demonstrate that our solutions can reduce compile time by more than 90% across all designs and run time by up to 99% for some tests where S/R is available.

Paper Presentation - 3

PP3 : Automotive | 12:30-14:00 @Conf G
Session Chair : Motoki Higashida, Verification Technology

PP3.1 (12:30-13:00)

Exploring Software-Defined Vehicles through Digital Twin Simulation with Extensible Prototyping FPGA: A Tool Perspective

Tasneem A. Awaad, Mohamed Ellethy, Mohamed AbdElSalam
Siemens EDA Egypt

In this paper, we present our compositional simulation interconnect framework for exploring Software-defined Vehicle implementations from cloud to edge. The framework enables heterogeneous clients' connections to create digital twins of Electronic Control Units (ECUs) of a Vehicle at different abstraction levels connected to real traffic scenario simulators, sensor models and mechatronic systems. The design methodology behind the framework is based on three enabling pillars: the gateway concept, Digital Twin Description Language (DTDL), and automation flow. An adaptive cruise control application is used as a demonstration of the interconnect framework.

PP3.2 (13:00-13:30)

Profiling and Optimization of Level 4 vECU Performance for faster ISO26262 Testing

Lukas Jünger,
MachineWare GmbH
Hitoshi Hamao, Megumi Yoshinaga, Koichi Sato
Renesas Electronics Corporation

The complexity of HW/SW systems has surged in recent decades, with even small embedded systems now running huge software stacks comprising millions of lines of code. This complexity is particularly critical in safety- and security-critical domains like automotive and aerospace, where thorough testing and verification are essential, often prerequisites for certifications such as ISO26262. Moreover, software issues can lead to substantial consequences, including accidents, damage to brand image, delayed product launches, and costly product recalls, underscoring the paramount importance of software quality. However, the limited availability, scalability and flexibility of physical hardware prototypes pose significant challenges during software development and verification. To address these challenges, testing strategies leveraging full system simulations executing unmodified target software, commonly referred to as Virtual Platforms (VPs) or Level 4 virtual Electronic Control Units (L4 vECUs), have emerged as a recommended and established practice. Unfortunately, the execution performance of L4 vECUs is frequently subpar, introducing scalability limitations. Additionally, identifying performance bottlenecks within these virtual environments can be challenging. In this paper, we propose a novel approach to construct fast, scalable, and flexible L4 vECUs utilizing the popular open-source simulator QEMU and the SystemC TLM standard. Leveraging SystemC TLM allows for seamless integration of existing simulation models and facilitates profiling of simulation execution to pinpoint bottlenecks accurately. We demonstrate our approach through a representative case study involving the construction, profiling, and optimization of a L4 vECU for a gateway ECU. By identifying and addressing simulation performance bottlenecks, we achieve a speedup of 1000x for the test scenario. This underscores the effectiveness of our methodology in enhancing the performance and scalability of L4 vECUs, offering significant benefits for the development and testing of complex HW/SW systems in safety-critical domains.

PP3.3 (13:30-14:00)

New Serial NAND Flash Octal Double Data Rate Feature Its Verification Challenges and Solution for the Automotive Application Space

Vishal Gulati, NXP Semiconductors India
Anil Gupta, Winbond Electronics
Sharvil Tushar Jani, Jaykumar Domadia, Durlov Khan
Cadence Design Systems

To meet the increasing bandwidth needs of the automotive industry, Serial NAND Flash memories have evolved from a 1-bit slow clock SPI interface to fast clock speeds over 2-bit and 4-bit derived SPI interfaces. Recently memory vendors added the Octal SPI interface to the Serial NAND Flash devices that enables 8-bit wide high bandwidth synchronous data transfers at manageable clock speeds. In several cases, the Octal SPI interface is combined with double data rate capabilities. The changes in device architecture and design have presented SoC validators with few options for rapid and effective verification of the feature within the high-demand and high-volume automotive application space. Automotive SoC and Flash Controller Silicon IP require a proven and reliable solution for the recent Octal DDR update to their controller. Cadence in partnership with suppliers of Octal Serial NAND including Winbond crafted a solution to add Octal DDR Verification support. The new Octal Serial NAND devices with Double Data Rate capability from Winbond offer up to 240MB/s continuous read data transfer rates at 120MHz clock speeds. This paper delves into the challenges faced by design validators and the implementation and usage details of the verification solution and demonstrates methods to verify Octal Serial NAND capabilities using a highly configurable user interface and Memory Model Advanced Verification (MMAV).

Paper Presentation - 4

PP4 : Protocol Verification | 12:30-13:30 @Conf H
Session Chair : Yukihiro Sasagawa, Socionext

PP4.1 (12:30-13:00)

Conquering UCIe 1.1 Multi-die System Verification Challenges

Hiromasa Terasawa, Mohit Bhardwaj
Synopsys

The Universal Chiplet Interconnect Express (UCIe) v1.0 standard was introduced in March of 2022 and v1.1 was published in July 2023. There is a huge demand for an open chiplet ecosystem that will unleash innovation across the compute continuum which in turn increases the demand for power efficient and cost-efficient solutions. UCIe 1.1 addresses four broad areas that encourage a thriving open chiplet ecosystem. These include enhancements like automotive segment, streaming protocol usages, cost optimization for advanced packages, and compliance testing. This session focuses on key design considerations to bring forward the verification requirements and an overview of verification solution to enable UCIe 1.1 complex designs.

PP4.2 (13:00-13:15)

[Short] Ensuring DRAM Compliance: Novel Verification Techniques for Refresh and Refresh Management in Modern Dram Architecture

Dharini SubashChandran, Shyam Sharma, Gruhesh Patel
Cadence Design Systems

DRAM data integrity is a core requirement for any of the modern SoCs NoC and PCBs where DRAM memories are used anywhere in the system. It is also one of the most difficult problems to verify in today's complex memory subsystems. Beyond the basic Refresh, Row Hammer and PRHT (Per Row Hammer Tracking) is increasing becoming an important consideration for the DRAM based systems. In the latest generation of DRAMs like DDR5 and Lpddr5, Refresh Management features are added to help designers tackle the Row Hammer challenges. This presentation talks about the innovative tools and solutions we have come up to help IP and SoC verification engineers, ensuring they can not only achieve their verification goals for the Refresh requirement that DRAMs have but also test the different aspects of Refresh Management and quantify their verification completeness by getting measurement of what all has been tested with intuitive Refresh/RFM related functional coverage.

PP4.3 (13:15-13:30)

[Short] Enhancing PHY Design Verification: A Tailored VIP Solution for PIPE Interface-Based Designs

Nehal Patel, Mrunal Pancholi, Nirav Toliya
Cadence Design Systems

Customers have been verifying their PCIe, DP, USB, USB4 PIPE PHY designs using protocol VIPs or custom traffic generators, which introduced an overhead to the verification in the form of protocol specific rules that were outside the scope of the PHY. Also, there was no PHY monitor solution which can observe both serial and parallel interface of the PHY DUT. Identifying this gap, Cadence developed a solution to address standalone PHY DUT Design verification.

Paper Presentation - 5

PP5 : New Language | 13:30-14:00 @Conf H
Session Chair : Yukihiro Sasagawa, Socionext

PP5.1 (13:30-14:00)

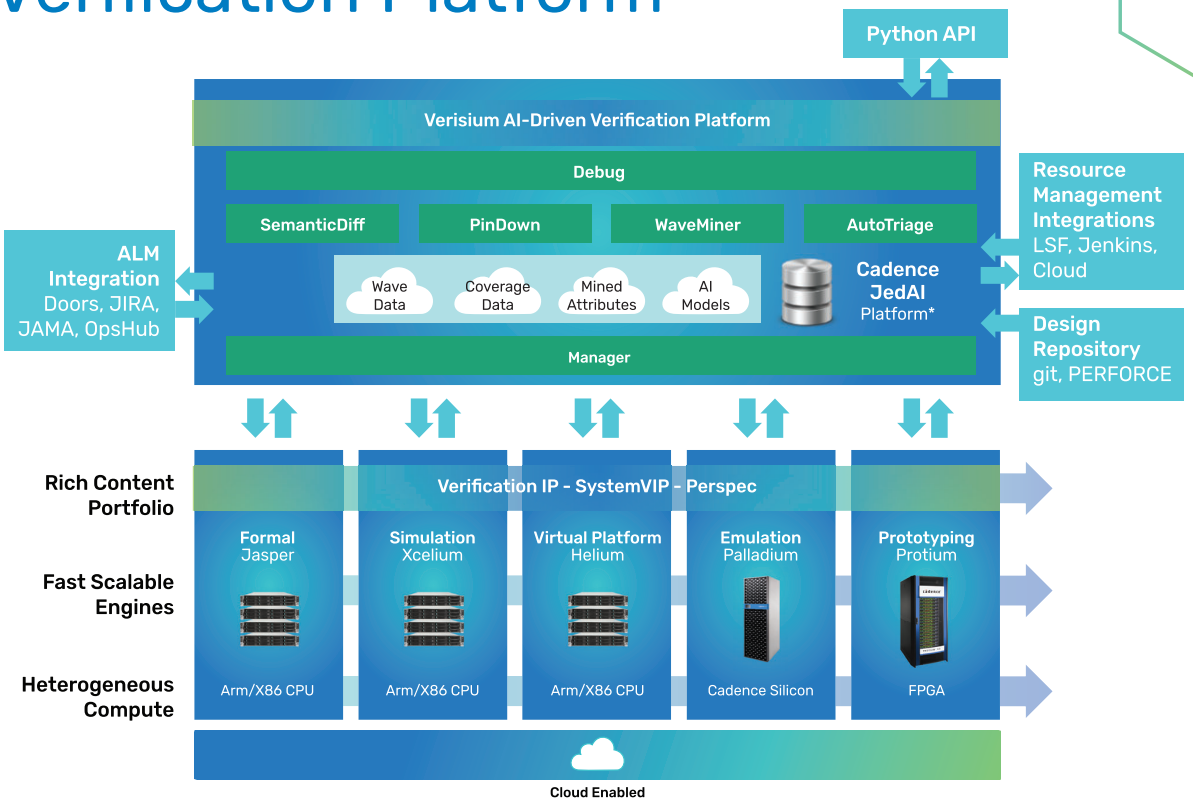
Veryl: A New Hardware Description Language as an Alternative to SystemVerilog

Naoya Hatta, Taichi Ishitani
PEZY Computing
Ryota Shioya
The University of Tokyo

Veryl, a hardware description language based on SystemVerilog, offers optimized syntax tailored for logic design, ensuring synthesizability and simplifying common constructs. It prioritizes interoperability with SystemVerilog, allowing for smooth integration with existing projects while maintaining high readability. Additionally, Veryl includes a comprehensive set of development support tools, such as package managers and real-time checkers, to boost productivity and streamline the design process. These features empower designers to conduct high-quality hardware design efficiently.

cadence®

Cadence Verisium AI-Driven Verification Platform



Verisium Manager	検証プラニング、ジョブスケジューリング、マルチエンジンカバレッジ等の機能を提供する統合管理環境。AIドリブンのテスト実行最適化により、コンピュートファーム/クラウド環境の効率を向上。ブラウザベースのコンソールによる簡単な操作でVerisiumプラットフォームの有効化が可能
Verisium Debug	基本デバッグ機能(波形、回路表示、ドライバトレース)および、SmartLog技術を活用しインタラクティブデバッグ、ポストデバッグを高速に実現するデバッグフローを提供。テストのパス・フェイル情報の自動比較によるAIドリブンのRoot Cause解析が可能な総合デバッグソリューション
Verisium AutoTriage	人手によるエラー選別(トリアージ)を学習し、自動化を支援するAI App
Verisium CodeMiner	異なるリビジョン間の構造的な差分を比較し、バグ混入リスクのある変更点のランク付けをAIで支援するApp
Verisium WaveMiner	複数の波形を比較し、フェイルの根本原因に関係する可能性が高い信号、タイミングを推定しデバッグ作業を効率化するAI App
Verisium PinDown	ソースコードの変更履歴情報から、バグを混入させた可能性が高いソースコード更新を推定するApp

Paper Presentation - 6

PP6 : DSP & HLS | 14:30-15:30 @Conf E
Session Chair : Shiho Hagiwara, TSMC Design Technology Japan

PP6.1 (14:30-15:00)

Quantization Methodology based on Value Range Analysis

Shigetaka Nata, Petri Solanti
Siemens EDA

Algorithm developers are usually using double precision data types to be able to focus on the mathematical functionality of the algorithm. When this algorithm is implemented as a hardware module, the data accuracy must be reduced to minimum number of bits that still fulfills the system performance requirements. The process of converting the floating-point algorithm to bit-level optimized model is complicated and requires special knowledge. This paper introduces a simple, easy, and robust quantization methodology based on value range analysis.

PP6.2 (15:00-15:30)

Impact of a 64-bit Vedic Multiplier on Processor, Multi-Core, and DSP Performance

Lakshya Miglani, Gopi Srinivas Deepala
Silicon Interfaces

The Urdhva Tiryagbhyam sutra-based algorithm revolutionizes multiplication by significantly reducing computational steps and enhancing Power, Timing, and Area (PTA) metrics. This paper introduces a 64-bit multiplier design that leverages the optimized Urdhva Tiryagbhyam algorithm for binary numbers, demonstrating improved efficiency and performance over traditional methods. Essential for Arithmetic Logic Units in processors, multi-core systems, and Digital Signal Processors (DSPs), rigorous testing has confirmed faster speeds and superior PTA metrics. Our Vedic multiplier deviates from conventional approaches by focusing on concatenation as the key operation for creating partial products. This method efficiently merges binary digits or bit strings crosswise, generating partial products that are then concatenated. An addition operation follows, producing a final 128-bit multiplication result. This innovative approach simplifies the multiplication process and reduces computational complexity, leading to better PTA outcomes. The paper showcases significant improvements in size, area, and power consumption, enhancing computational efficiency and resource utilization. This development represents a significant leap in multiplier design, paving the way for progress in various fields. Its integration into computing systems heralds a new era of digital computation, offering unmatched efficiency and leading to new levels of performance and power efficiency.

Paper Presentation - 7

PP7 : Formal Verification & Security | 14:30-15:30 @Conf F
Session Chair : Takehisa Hashimoto, SONY Semiconductor Solutions

PP7.1 (14:30-15:00)

Noise Reduction in Coverage-Based FV

Gilboa Alin, Emilia Katz
Intel Israel

Formal-Verification (FV) plays a crucial role in the verification methodology of chip design. Establishing a robust signoff methodology is essential for FV to become a mainstream validation approach. The primary challenges/risks in FV include being overly constrained by assumptions, and assertions that do not cover the entire design . FV tools can create automatic cover points and attempt to verify that they are reachable and checked by at least one assertion. However, the number of cover points can reach hundreds of thousands and many of them can be unreachable or remain unchecked. Indicating which of them are hiding bugs is the main challenge in FV sign-off. In this paper, we explore this topic and propose a solution for efficiently and reliably cleaning violation reports to facilitate sign-off.

PP7.2 (15:00-15:30)

Introduction of CHERI and how it works

Shigehiko Ito
Codasip

In recent years, the number of memory vulnerabilities discovered has been on the rise, and the cost of addressing them has been increasing. In addition, a huge amount of legacy C/C++ code is at risk of memory vulnerabilities. To solve this problem, a new technology called CHERI (Capability Hardware Enhanced RISC Instructions) has been developed. This is processor hardware that enables software to implement robust memory access mechanisms. In this presentation, we will explain what is CHERI and demonstrate CHERI.

Paper Presentation - 8

PP8 : Power & Performance | 14:30-15:30 @Conf G
Session Chair : Hiroshi Hosokawa, Canon USA

PP8.1 (14:30-15:00)

Optimizing UPF Integration Efficiency through Enabling Automation with UPVM for Unified Power Verification

Gopi Srinivas Deepala, Lakshya Miglaini, Sastry Puranapanda
Silicon Interfaces

This paper presents an innovative approach to enhancing UPF integration efficiency by leveraging automated enablement with UPVM for unified power verification (UPV). We introduce a Python-based automation tool designed to seamlessly integrate UPF power strategies with UPVM class libraries. UPVM, a burgeoning open-source standard for Unified Power Verification Methodology™, serves as the vital link between UVM and UPF. The automation tool streamlines the process from RTL to GLS and GDSII stages for Design under Test (DUTs), emphasizing low-power functionalities. It simplifies complex tasks such as power domain management, hierarchical organization, supply port creation, interconnection, state transition handling, and comprehensive power strategy implementation. By bridging the gap between UPF and UVM methodologies, the tool effectively addresses challenges related to power management during verification. Furthermore, it ensures strict compliance with low-power criteria by facilitating the seamless translation of power objectives from RTL to GLS/GDSII. Through its holistic and integrated approach, this tool aims to revolutionize low-power semiconductor design practices, leading to heightened power efficiency, error reduction, and smoother transitions across diverse design development stages.

PP8.2 (15:00-15:30)

High-Speed Emulation Framework for Performance Analysis of GenAI SoC design

Saksham Mehra, Kalyan Kar, Abhishek Saksena
Google

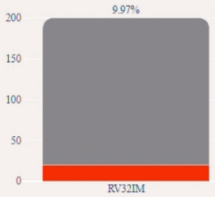
Addressing the challenges of thorough performance testing for GenAI and other complex usecases on System-on-Chip (SOC) designs within constrained timeframes is paramount. This paper proposes a novel approach leveraging emulation platforms and synthesizable traffic generators, which provides easier stimulus control and cycle accuracy for testing synthetic patterns. Our solution is cost-effective and explores the availability of the platform much earlier in the project cycle, which aids in giving feedback to the architects before the design freeze. In addition, the user friendly nature of the platform makes it ideal for conducting architectural studies such as MMU and cache sizing on actual SoC RTL designs.

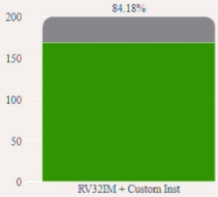
RISC-V は皆同じではありません

Custom Compute で差別化を

CBI で検証労力も激減

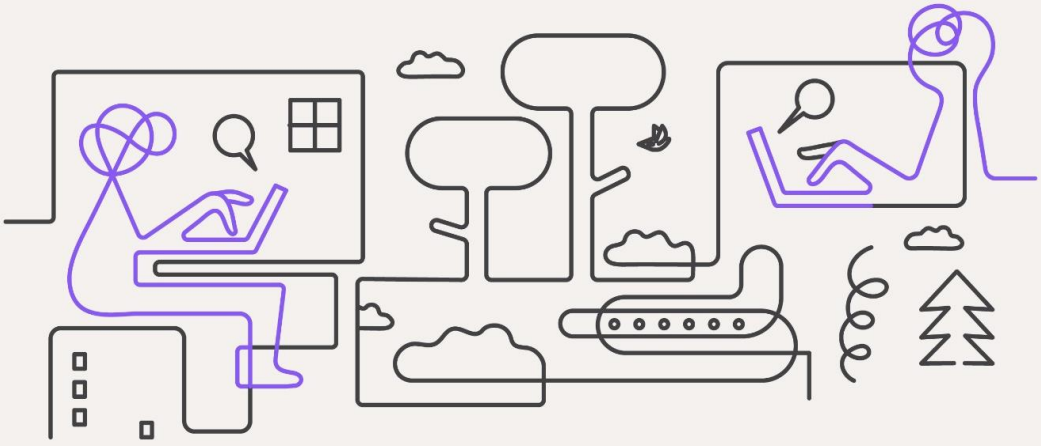
RV32IM (80MHz)		RV32IM + カスタム命令 (20MHz)
1.03	AI モデルのスループット [推定量/秒]	1.27
77.91M	サイクル数 [サイクル/推定]	15.77M
1.64	消費電力 [mJ/推定]	0.23





メモリ安全対策は CHERI で

Codasip



RISC-V

Tutorial Session

Tutorial T3 16:00-16:50 / Conf E

Portable Stimulus Standard Update

Steering Committee
Hiroshi Hosokawa, Canon USA

SoCをリセット状態から動作状態にするには、数百から数千のIPレジスタを設定して、サブシステムとIPをコンフィギュレーションする必要があります。動作のモードでは、さらに多くのレジスタを設定する必要があります。ブロックの設計チーム、検証チーム、サブシステムとSoC検証チームなどのステークホルダーはレジスタの正確な設定するシーケンスに早期にアクセスできる必要があります。UVMやCコードで実装されるレジスタ設定をPSSで制御することで、ブロックレベルからSoCレベルへとスムーズにテスト資産が受け渡されます。このチュートリアルでは、PSS 3.0で開発中のPSS機能も含め、ワーキンググループの現在の取組みについてアップデートします。

Tutorial T4 16:00-16:50 / Conf F

Introducing Smart Verification, Unleashing the Potential of AI Within Functional Verification

(スマート検証の紹介 - AIを検証の世界に活用しより生産性を高めるアイデア)

Siemens EDA Japan
Front end Verification, AE Manager, Taiki Ando

エンジニアの確保が大変難しい時代になってきました。エンジニアの生産性を高めるために、AI・MLを採用し日々の業務を効率化することが重要になってきています。データドリブン検証環境は、検証で生成されるデータをAI・MLで学習し、リグレッションやカバレッジ解析を効率化するソリューションのご提案をいたします。
It has become very difficult to secure engineers. In order to increase the productivity of engineers, AI/ML is becoming increasingly important to improve the efficiency of day-to-day work. Data-driven verification environment is a solution that uses AI/ML to learn the data generated by verification, and to improve the efficiency of regression and coverage analysis. We propose solutions to streamline regression and coverage analysis.

Tutorial T5 16:00-16:50 / Conf G

SA-EDI Update

Steering Committee
Akio Mitsuhashi, EE Tech Focus

AccelleraのSA-EDI(Security Annotation for Electronic Design Integration)はIEEEに寄贈され P3164として標準化が進んでいます。SA-EDIの適用効果はIPに存在するアセットを正確に特定することに大きく依存します。また特定するだけでなく正確な分類も不可欠です。しかしこの作業は思っているほど簡単ではありません。アセットの特定には、セキュリティ要件、ユースケース、周辺のIPなどIPの統合に関する一連の情報が必要になることが多いからです。結果として設計プロセスのかなり後になって定義されることが多いのです。このセッションではSA-EDIそのものの基本的な情報に加え、セキュリティ実務の経験が浅いIP所有者でも適用可能な、メソドロジに基づいたアプローチを紹介します。

Tutorial T6 16:50-17:40 / Conf E

A Subjective Review on IEEE Std 1800-2023

(IEEE Std 1800-2023の要約)

Kazuya Shinozuka
Art Graphics

2024年2月28日にSystemVerilogが改訂されて IEEE Std 1800-2023として公開されました。しかし、その重要性にもかかわらず改訂版が公開されている事は広く普及していません。そこで、本チュートリアルでは最新のSystemVerilogを要約しどのような新機能が使用可能であるかを解説します。この改訂版には、前仕様における誤りの訂正、曖昧な仕様の明確化、新規に追加された機能の解説が含まれています。誤りの訂正に関しては、正誤表等を参照する事により解決します。一方、仕様の明確化に関しては、単なる補足説明で済むものもあれば、詳細な解説が必要な仕様もあります。然し、幸いにも、昨年のDVConにおいてDave Rich氏がそれらを明確にする努力をされていたので、敢えて解説をここで繰り返す必要はないと思えます。したがって、本チュートリアルでは、改訂版IEEE Std 1800-2023で使用可能となった新機能を中心に解説をします。

IEEE Std 1800-2023 was published on February 28 this year and has replaced the previous revision IEEE Std 1800-2017. Despite the significance of the release, its availability appears not to be pervasive. The purpose of this tutorial is to provide an overview and summary of this new revision as part of propaganda for the latest SystemVerilog. The new revision includes corrections and clarifications in the aspect of the language definition in the previous one. It has also introduced enhancements that ease design and improve verification. As for corrections, checking for errata will suffice. While some clarifications are simply informative and require no further explanations, others deserve special comments. Fortunately, however, many of important clarifications were already presented and discussed in depth at DVCon last year by Dave Rich, and we feel that repetitive effort is unnecessary. Therefore, this tutorial intends to summarize the enhanced language features of the new revision, including how to use them.

Tutorial T7 16:50-17:40 / Conf F

Low Power Verification Using Formal Technology
(フォーマル技術によるローパワー検証)

Jun Ueda
Synopsys Inc.

生成AIが多くの関心を集めるようになり、私たちの生活は想像を絶する変化を遂げつつあります。GPT-3の機能と1750億のパラメータを処理するAIチップ1つで、推定1280メガワット/時を消費し、これは約120台のガソリン車が1年間走れるエネルギー量、約550トンの二酸化炭素排出に相当します。生成AIや、他の類似アプリケーションは半導体デバイス上で稼働するため、デバイスの消費電力をできるだけ削減することが不可欠です。

省電力の最も一般的な手法は、クロックゲーティング、パワードメインと電圧アイランドの分離、リテンション・セルの活用、効率的な電源管理ユニットの設計などです。これらのローパワー・エレメントの採用によって、デザインに回路が追加されることになり、デザイン動作に影響を与える可能性があります。こうしたローパワー構造を考慮しつつデザインの機能的意図を検証することは非常に重要です。

本チュートリアルでは、リテンション充足度のチェックなど、デザイン内のローパワー・エレメントを考慮したフォーマル・コネクティビティ・チェックとプロパティの検証手法を中心に、消費電力/性能/面積（PPA）を改善するローパワー検証手法をご紹介します。(例: 仕様と UPF 間のIsolationの不一致、PG ピンのコネクティビティ・チェック、Isolation信号伝播チェックなど)

Generative AI created a lot of interest recently and is poised to change our lives in many unimaginable ways. One significant change we already know is the huge amount of power it consumes: an AI chip with the functionality of GPT-3 and 175 billion parameters would require an estimated 1280 megawatt-hours, which is equivalent to about 120 gasoline powered cars operating for one year and creating around 550 tons carbon emissions. Generative AI and other similar applications leverage semiconductor devices, so it is imperative that such devices consume as little power as possible.

The most common power saving schemes are clock gating, separating power domains and voltage islands, installing retention cells, and designing efficient power management units. These low-power instruments add circuitry to the design and potentially impact design behavior. Verifying the functional intent of the design in the presence of the low-power constructs is critical.

This tutorial topics include: Formal connectivity checking and property verification in the presence of low-power elements in the design, including checking retention sufficiency to help improve PPA. (e.g., Isolation mismatch between spec and UPF, PG pin connectivity checks and Isolation signal propagation checks)

Tutorial T8 16:50-17:40 / Conf G

RISC-Vの歩き方

(The way we walk around RISC-V)

Takaaki Akashi
Codasip GmbH

RISC-Vが市場に浸透しつつあります.特に組込み市場では成長し始めています.理由幾つか挙げてみると、a) 命令セットがオープンだから、b) オープンソースIPがあるから、c) ARMより安価で導入できそうだから、d) 自作できるから、e) カスタムできるから、等々です.RISC-Vは、これまでの特定企業が寡占していた命令セットと異なり、様々な面で自由度が高いため、これまでの「IPを購入する」意外にも、先のように幾つもの導入方法があります.これらのメリットとデメリットについてご紹介しコダシップのソリューションがどの局面でどのように有用かご紹介したいと思います.

RISC-V is spreading into the market. Especially in the embedded market, it is starting to grow. The some major reasons are: a) open instruction set, b) available open source IP , c) maybe cheaper than ARM, d) homebrew, e) customizable, etc. Unlike instruction sets that have been dominated by particular companies, RISC-V has a lot of freedom in various aspects. Therefore, there are several ways to adopt RISC-V other than "just buying IP" as described above. We would like to introduce the advantages and disadvantages of these options and how Codasip's solutions can be useful in each situation.

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