DVCON EUROPE 2025

CONFERENCE PROCEEDINGS

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2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

DVCon Europe 2025

Welcome Message from DVCon Europe General Chair,

Mark Burton
General Chair - Qualcomm

Dear Colleagues and Friends,

Welcome to DVCon Europe 2025!

This year, we gather at a pivotal moment in so many ways. In 2025, we focused on the growing impact of Artificial Intelligence, and I think we can all agree, the pace of change has been nothing short of extraordinary. AI is now embedded in our daily lives, for better or worse.

Personally, I worry about what this means for the next generation of engineers. We must ensure that AI enhances, not replaces, the brilliance, creativity, and curiosity of human talent. That's a challenge for all of us, especially as we struggle to comprehend what's coming next. In some ways, we may not even be worthy of calculating the simplest parameters of the future ahead.

Yet DVCon Europe has always stood for progress, especially in automation. And in 2025, that means embracing AI, not passively, but actively shaping how it fits into our workflows and our values. One thing is already clear: to truly benefit from AI, we must also benefit more from each other. The future lies in open, collaborative ecosystems—wider, more inclusive, and more transparent.

That brings me to our two outstanding keynotes this year.

First, we're honoured to welcome Amanda Brock, CEO of OpenUK. Amanda will delve into what open ecosystems really mean—not as an abstract idea, but grounded in legal, technical, and societal realities. If you haven't heard her speak before, you're in for a treat. Her insight into Open Source is as sharp as it is necessary, and I suspect her talk may challenge a few assumptions (in the best possible way).

Second, those of you who have been attending DVCon Europe for a while may remember the memorable keynote from Berthold Hellenthal, then Head of the Progressive Semiconductor Program at Audi AG, back in 2017. It has gone down in our history as one of the most attentively listened to and influential keynotes we've ever hosted. A clear challenge was issued: to provide Virtual Platforms for Automotive. So, you may be forgiven for wondering, what happened?

To answer that, we've invited Ralf Schleifer to return and give us an update on the state of virtualization in automotive, from Audi's perspective. I'm not just excited, I'm also waiting with some trepidation to hear what he has to say! But that's the spirit of DVCon Europe: we ask the hard questions and welcome the honest answers.

On the social side, I'm delighted to announce the return of the off-site dinner at the beer hall, a clear favorite from DVCon Europe's 10th anniversary in 2023.

It's a fantastic opportunity to relax, reconnect, enjoy surprise entertainment, and engage in the kind of informal conversations that so often spark great ideas.

As always, I'd like to extend my heartfelt thanks to our sponsors, exhibitors, technical committees, and volunteers. Your time, energy, and commitment are what make DVCon Europe possible and successful.

Of course, DVCon Europe would not exist without the invaluable contributions of all those who have spent the time to write engineering papers, research papers, and tutorials. I know how much time and effort it takes! As ever quality increases every year (and I must say, the gramma is remarkably good this year, I wonder why?)

So, as we kick off this year's conference, I invite you to get involved. Challenge assumptions. Share insights. Be curious. And most of all, help shape the conversations that will define our industry for years to come.

Thank you for being part of DVCon Europe 2025 and for making a difference.

Warmest regards,

Mark Burton
General Chair, DVCon Europe 2025

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Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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Technical Program Grid - Day 1 - Tutorials - October 14

	Forum 4	Forum 5	Forum 6	Forum 7	Forum 8	Großer Saal
8:00 - 8:15 AM	**Opening Session** (Ballsaal)					
8:15 - 9:15 AM	**Keynote Speaker: Amanda Brock** (Ballsaal)					
9:15 - 9:45 AM	**Attendee Coffee Break & Expo Hours** (Großer Saal)					**Exhibit Hall Open**
9:45 - 11:15 AM	1A: Liberating Functional Verification from Boolean Shackles REAL INTENT	1B: Cybersecurity: A Model-Based Systems Engineering Approach to Risk Analysis and Mitigation (hands-on) MathWorks	1C: Cadence Verisium - Optimizing Regressions and Debug with AI cadence	1D: Data-Driven Approach to Accelerate Coverage Closure on Highly Configurable ASIC Designs SIEMENS	1E: Pre-Silicon Performance Benchmarking with Emulation Hybrids SYNOPSYS	
11:15 - 11:30 AM	**Break**					
11:30 - 1:00 PM	2A: CDC-RDC Standardization: Concepts & Status	2B: Efficient SoC Modeling, Architectural Exploration, and Result Analysis using TLM2 based IPs	2C: Creating a Co-Simulation Environment for Questa Simulator Using QEMU	2D: Tackling the cyber-physical system design challenges with MBSE and SystemC	2E: Cocotb and PyUVM tests powered with pytest	
1:00 - 3:00 PM	**Lunch & Expo Hours** (Großer Saal)					
3:00 - 4:30 PM	3A: Unleashing the Potential of AI Within Functional Verification SIEMENS	3B: Property Generator: simple generation of Formal Assertion IP LUBIS EDA	3C: Next-Gen Verification Technologies for Processor-Based Systems SYNOPSYS	3D: Will it Blend? - Verifying the Hardware / Software Interface of complex SoCs ARTERIS IP	3E: Scalable Virtual Platforms for Automotive and Beyond MACHINEWARE	
4:30 – 5:15 PM	**Break**					
5:15-6:45 PM	4A: Tutorial on the Improvement introduced by IEEE 1801-2024 (UPF4.0) Standard for the Specifications, Implementation and Verification of Low Power intent	4B: Expediting Coverage Closure in Digital Verification with the Portable Stimulus Standard (PSS)	4C: Introduction to the Apheleia Verification Library	4D: Teaching Analog CMOS Chip Design using Open Source Tools	4E: Standardization of Multi-Physics Interfaces and Model Exchange Mechanisms	
6:45-7:30 PM	**Break**					
7:30-10:30 PM	**Conference Dinner (Hofbräukeller - Innere Wiener Straße 19 - 81667 München)** sponsored by: AMIQ					

Technical Program Grid - Day 2 - October 15

	Forum 4	Forum 5	Forum 6	Forum 7	Forum 8	Großer Saal
8:15-8:30 AM	**Opening Session** (Ballsaal)					
8:30-9:30 AM	**Keynote Speaker: Ralph Schleifer** (Ballsaal)					
9:30-10:00 AM	**Attendee Coffee Break & Expo Hours** (Großer Saal)					**Exhibit Hall Open**
10:00-12:00 PM	Session 5A: AI and Machine Learning for Verification & Coverage	Session 5B: Formal & Symbolic Approaches to Digital Verification	Session 5C: Mixed-Signal and Power-Aware Verification	Session 5D: Virtual Prototyping and System-Level Simulation	Session 5E: Functional Safety and Security	
12:00-1:00 PM	**Lunch & Expo Hours** (Großer Saal)					
1:00-2:00 PM	**Panel** (Ballsaal)					
2:00-2:15 PM	**Break**					
2:15-3:45 PM	Session 6A: Next Generation UVM Testbenches	Session 6B: Innovative and Reusable Verification Methodologies	Session 6C: Advances in Virtual Platform Integration	Session 6D: Debugging and Formal Methods in Verification	Session 6E: AI and Automation in Verification Workflows	
3:45-4:15 PM	**Attendee Coffee Break & Expo Hours** (Großer Saal)					
4:15-5:45 PM	Session 7A: Scalable Verification through Automation and Formal Methods	Session 7B: Coverage Reuse and Model Based UVM	Session 7C: Mixed Signal Verification and Automation	Session 7D: Virtual Prototyping and Digital Twin Applications	Session 7E: AI and Infrastructure	
5:45-6:15 PM	**Closing Session & Best Paper Award** (Großer Saal Foyer)					

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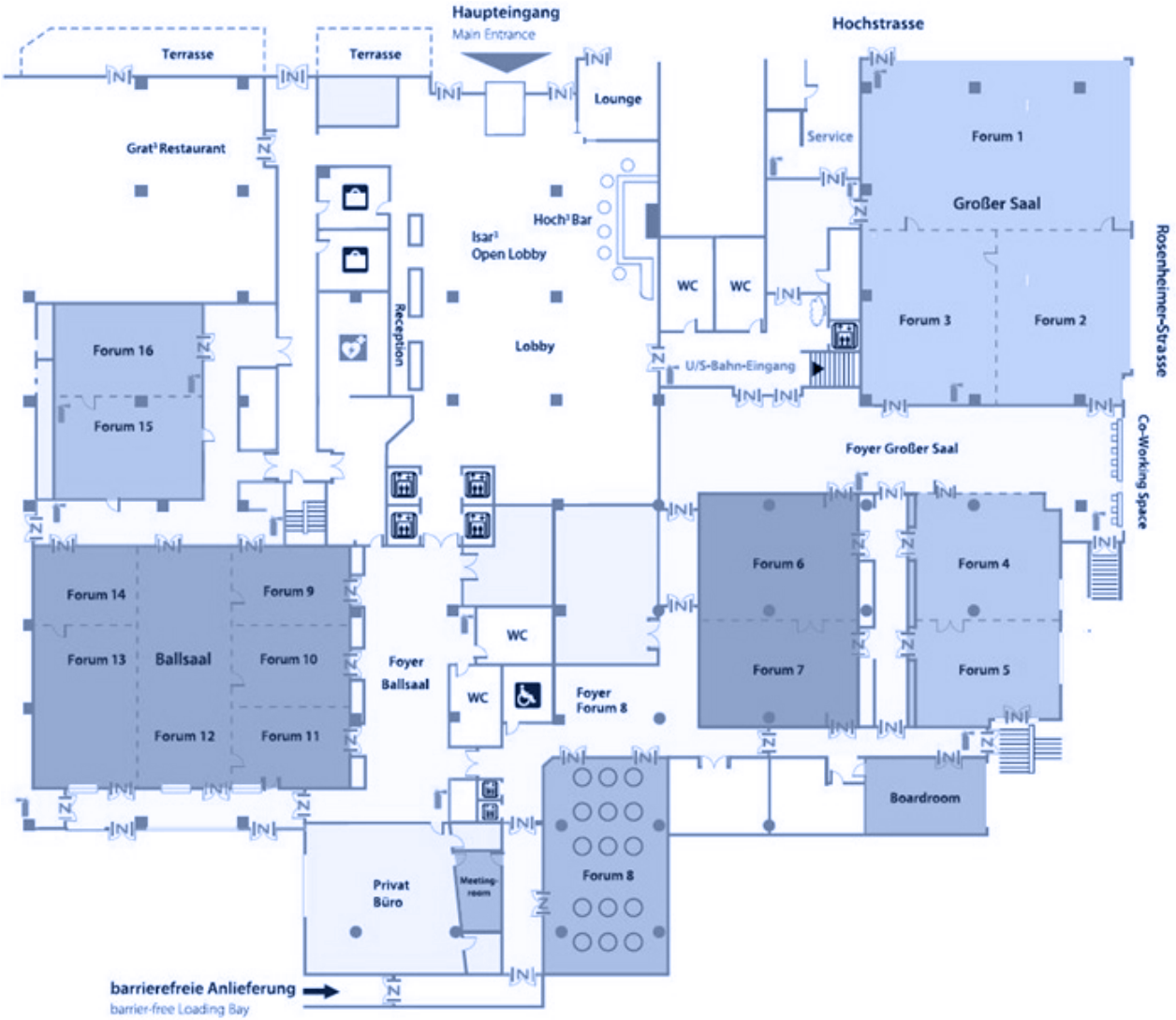
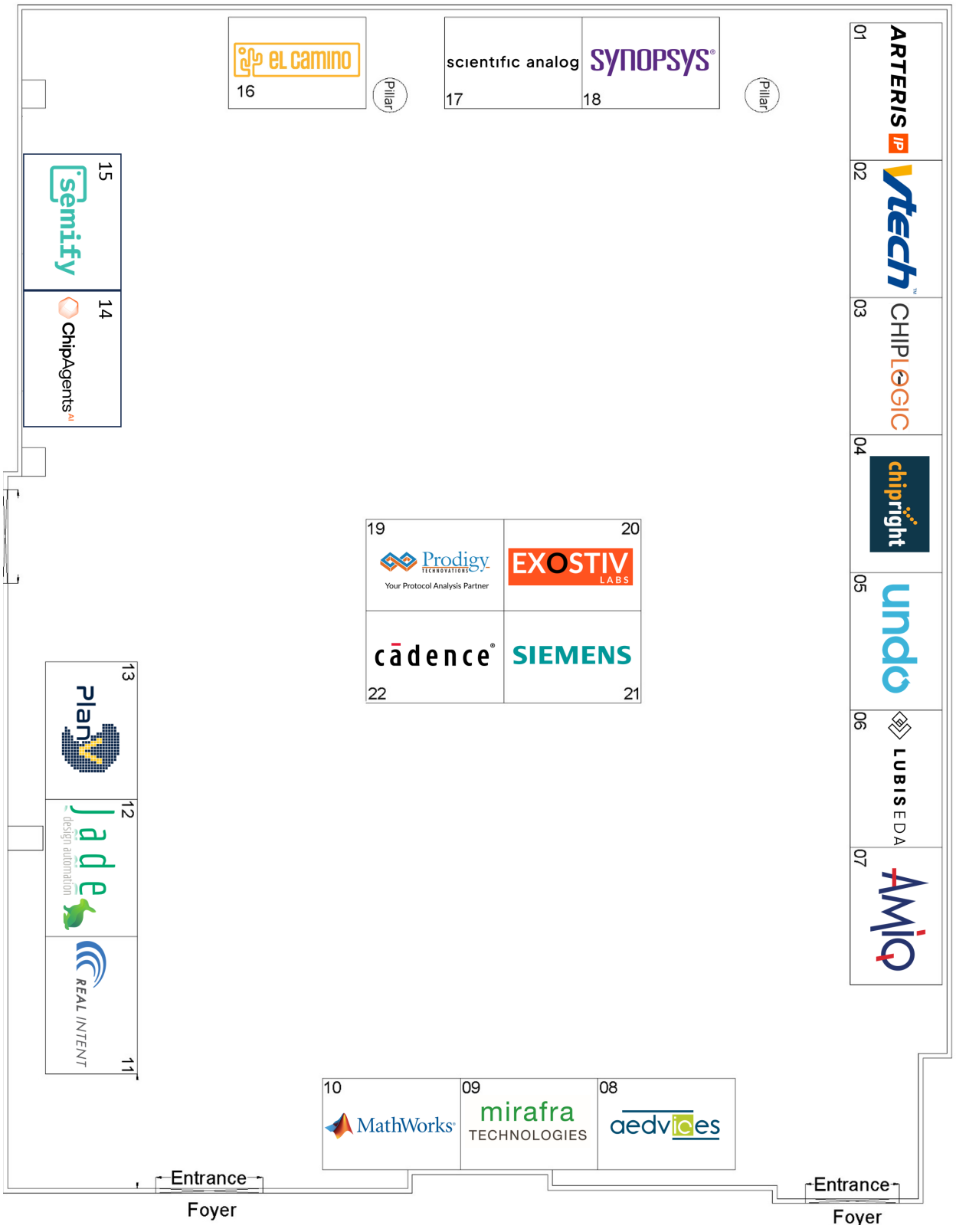
DVCon Europe 2025 Venue - Holiday Inn Munich City Centre

Hochstraße 3, 81669 München, Germany

The hotel is directly above Rosenheimer Platz S-Bahn station for fast, frequent connections across the city. It's a 10-minute train ride to Munich Hauptbahnhof and 35 minutes to Munich Airport (MUC). Families love the science and tech exhibits at the vast Deutsches Museum, a short walk away, while shoppers delight at the stores lining pedestrianised Kaufingerstrasse in the Old Town. The hotel has 18 meeting rooms offering space for up to 550 guests, and its convenient location makes it an ideal venue for events.



DVCon Europe 2025 Exhibit Hall - Großer Saal



DVCon Europe SystemC Modeling Challenge

Estimate Power with SystemC – Win a High-End Laptop, Travel Grants & More!

Put your skills to the test in the DVCon Europe Challenge 2025. Create a SystemC model that uses power measurements and data from a known scenario to estimate power consumption in an unknown scenario. This challenge is open to advanced students and professionals interested in SystemC modeling and low-power design. A short introductory workshop will be provided, along with a video recording for those who cannot attend live.

Learn More: **https://dvconchallenge.de/**

Tutorial Program: Tuesday, October 14th

Opening Session
8:00 AM - 8:15 AM
Ballsaal

Keynote Speaker: Amanda Brock, OpenUK CEO
8:15 AM - 9:15 AM
Ballsaal

We Didn't Start the Fire…Open Source Software in 2025

Abstract: In this session Amanda will guide the audience through a refresher on the meaning of open source software to build a base understanding of the shift in digital infrastructure over the last 10 years where the pace of adoption of open source has not been met with a pace in understanding.

As she peels the layers of our digitalisation back it will reveal the underbelly of our tech sector, what makes tech tick today and why it's driving in the directions it is. From geopolitics, to tariffs and calls for sovereignty she will explore the stories we all know to build deeper understanding of policy bathed in a technical context. Embracing software infrastructure deep tech and AI, this story is one of the technical and social evolution of the last 30 years, driven by a world of open source and global collaboration.

Biography: OpenUK CEO, Amanda Brock has built one of open source's most recognised and impactful organisations. Executive Producer of State of Open Con (2023- 2025), Amanda's a globally sought-after keynote speaker.

A lawyer with 25 years' experience, 5 as GC of Canonical, she's been instrumental in shaping open source's legal frameworks, as she was internet law during the early 2000's.

Regularly contributing to tech press, she edited "Open Source: Law, Policy and Practice", 2nd edition (2022).

Recognition: Computer Weekly 50 Most Influential Women in UK Tech (2023, 2024) listed as #20 in 2024; Computing IT Leaders 100 (2023, 2024); Lifetime Achievement Award WIPL (2022); Women Who Will Changemaker (2023); INvolve Heroes (2022, 2023); Novi Awards (2024); and Ambassador, Open Charge Alliance.

Advisory Board Appointments: UK Cabinet Office Open Standards Board; UKRI Digital Research Infrastructure; UKRI Exascale; KDE; commercial boards – Mimoto, Scarf, FerretDB and Space Aye; and Fellow, Open Forum Academy; Distinguished Fellow, Rust Foundation; and European Representative, OIN and Board Member Mojaloop Foundation.

Attendee Coffee Break & Expo Hours
9:15 AM – 9:45 AM
Großer Saal

Exhibit Hall Open
9:15 AM – 6:30 PM
Großer Saal

Tutorial Program: Tuesday, October 14th (cont.)

1A: Liberating Functional Verification from Boolean Shackles

9:45 – 11:15 AM
Forum 4
Speakers:
Vikas Sachdeva

Functional verification remains a major resource-intensive task in modern semiconductor design. According to industry studies, verification engineers dedicate their entire focus to ensuring functional correctness, with clock-related issues and logic bugs being leading causes of silicon re-spins. As designs grow in complexity—particularly in clocking, power management, and resets—static and formal verification methods have become indispensable.

This tutorial explores the paradigm shift in functional verification, emphasizing the role of static signoff in enabling early defect detection, improved design quality, faster time-to-market, and cost reduction. The session covers:

- Early Functional Verification Tools that generate signoff-quality results even before traditional simulation or formal methods.
- Core Requirements for RTL Signoff, including speed, capacity, and comprehensive coverage.
- Comparison of Static, Dynamic, and Formal Verification, highlighting how static signoff overcomes Boolean limitations, achieving results that are 10-100x faster and scalable to billions of gates.

Real-world case studies will demonstrate how static signoff effectively resolves design re-spin issues, including logic bugs, clocking challenges, and reset failures. Key static signoff categories covered include:

- Established RTL Static Signoff – Early bug detection via linting and multi-policy checks.
- Enhanced RTL Static Signoff – Advanced DFT, glitch detection, and other verification pain points.
- Expanded RTL Static Signoff – Addressing NoC validation, connectivity verification, and hardware security assessments.

The tutorial concludes with best practices for static signoff, equipping RTL designers, verification engineers, SoC architects, and chip designers with the tools to implement a shift-left verification approach. Attendees will gain practical insights into optimizing functional verification, reducing rework, and accelerating design cycles.

1B: Cybersecurity: A Model-Based Systems Engineering Approach to Risk Analysis and Mitigation (hands-on)

9:45 – 11:15 AM
Forum 5
Speakers:
Marco Bimbi and Cristian Macario

Hands-on session, attendees can bring their own laptop and go through the presented examples. Cyberattacks are on the rise, targeting electronic systems

across various industries. For example, vulnerabilities in several car brands have allowed anything from remotely controlling the brakes during driving to theft of a vehicle within 30 seconds. Semiconductor devices often play a critical role in these attack scenarios, emphasizing the need for robust cybersecurity measures. Consequently, many industries have established cybersecurity standards such as ISO/SAE 21434, IEC 62443, DO-356, and the Cyber Resilience Act. These standards require a structured security risk analysis to anticipate weaknesses during early development and define security features that protect these systems from attacks.

1B: Cybersecurity: A Model-Based Systems Engineering Approach to Risk Analysis and Mitigation (hands-on)(cont.)

A wealth of metadata including threats, attack vectors, and impact rating must be captured, analyzed to deduce risk factors, and kept consistent throughout the development phase. This data must also be updated over the whole product life cycle in response to security incidents after production.

This hands-on tutorial walks the attendees through a full workflow that manages security risks efficiently and consistently with Model-Based Approach. Participants will learn:

- Fundamentals of Model-Based Design in the context of security risk analysis
- Asset and threat identification (STRIDE method)
- Feasibility estimation (attack potential method)
- Severity assessment (attack simulation method)
- Integration with safety data such as FHA and FMEA
- Countermeasure definition, goal allocation, and residual risk calculation
- Verification and validation of security goals
- Change analysis to track design changes and keep risk data consistent

Participants are encouraged to bring their laptops. We will provide access to the necessary tools to ensure a practical, hands-on experience.

1C: Cadence Verisium - Optimizing Regressions and Debug with AI

9:45 – 11:15 AM

Forum 6

Speaker:
Moshik Rubin

While Agentic AI promises to revolutionize the ways in which chips are designed and verified, the fundamental building blocks, AI Agents, are available today to optimize regressions and shorten total debug. In this session we will highlight how the Verisium platform's industry-leading verification planning, management and debug capabilities have been upleveled and enhanced with AI agents offering automation for everything from regression optimization to failure root cause analysis. Topics will include automation and optimization for regression orchestration, testcase selection, verification planning, coverage closure, failure triage, bug prediction and waveform analysis, all enhanced with AI.

1D: Data-Driven Approach to Accelerate Coverage Closure on Highly Configurable ASIC Designs

9:45 – 11:15 AM

Forum 7

Speakers:
Tulio Pereira Bitencourt, Rasadhi Attale, Samuel Man-Shun Wong, Po-Shao Cheng and Anton Tschank

During the last few decades, the semiconductor industry has experienced an ever-growing complexity in integrated circuit (IC) designs. The requirements for chips have risen and with more tasks now being allocated into devices that must be area efficient, low power and operate at high frequencies, it becomes challenging to ensure that those marvels of technology work flawlessly before they go into production.

As the industry moves towards Intellectual Property (IP)-based approaches, where independent parts of chips are purchased and embedded to compose more robust and application-specific integrated circuit (ASIC) designs, Verification Engineers must now cope with increased complexity of highly configurable ICs while ensuring acceptable time-to-market. Moreover, relying on robust and straightforward Electronic Design Automation (EDA) tools and effective data-driven methodologies ensure that coverage targets can be met even in the most complex scenarios.

1D: Data-Driven Approach to Accelerate Coverage Closure on Highly Configurable ASIC Designs(cont.)

This tutorial aims to propose a novel data-driven approach to accelerate coverage closure on highly configurable ASIC designs. During the tutorial, the following topics will be covered:

Challenges of working with highly configurable IPs: Discusses the different aspects of verifying fully parameterized ASIC designs that leverage randomized parameters in thoroughly compatible testbenches and coverage metrics.

Requirement management and verification planning: Showcases the need for well-defined, mappable and machine-readable specifications, the creation of parameter-based verification plans, and the importance of end-to-end traceability for data-driven verification.

Early bug detection: Focuses on the importance of continuously monitoring metrics to identify gaps or issues early in the process. Introduces live simulations and alternatives to track historical regression data for optimized debugging.

Traffic light system & Unreachability: Presents the application of a traffic light system (i.e., green, amber and red waivers) for assessing coverage reachability under highly configurable environments.

Structure for effective regressions: Introduces a powerful and well-defined regression system capable of randomizing parameters, generating data (e.g., coverage, failures, etc.) and collecting failure signatures.

Accumulated coverage structure: Proposes a robust and straightforward procedure to generate and accumulate coverage metrics across all supported and randomized configurations.

Real-time and interactive dashboards: Highlights the value of real-time and interactive dashboards for acquiring an overall view of design/verification health and regression performance. Its advantages become clear when there is a need for scalable and efficient identification of issues in large permutations of IP configurations.

Powerful tools to enhance time-to-market: Wraps up the presented methodology and describes how to effectively use a mix of graphic, analytic and artificial intelligence/machine learning (AI/ML) options to accelerate Coverage Closure.

Therefore, the herein presented data-driven approach aims at effectively accelerating the coverage closure process of highly configurable ASIC designs by leveraging the presented state-of-the-art methodology and robust EDA options. The tutorial is structured to showcase a new methodology to cope with very complex real-world scenarios when dealing with highly configurable designs, as well as to present thorough details on how one can reproduce it.

1E: Pre-Silicon Performance Benchmarking with Emulation Hybrids

9:45 – 11:15 AM

Forum 8

Speaker:

Leonard Drucker

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As the semiconductor industry is experiencing an explosion in design size and complexity, it is accompanied by a need to deliver software readiness when the silicon is back in the lab. One of the key targets for software readiness is achieving targeted performance specifications with real software applications stressing the hardware design. There are 2 key elements to validating performance pre-silicon – speed of model execution and the ability to execute a full software stack. Combining a fast virtual prototype of the CPU sub-system with the RTL of the remaining SoC running on an emulator typically produces a 10x speed-up over fully-RTL emulation setups. Recent advances in both virtual prototyping and emulation now yield another leap in hybrid performance, which enables pre-silicon execution of entire software stack. Similarly, dynamic metrics collection need to be efficient enough to handle these large workloads and be able to address industry and custom KPI's. In this workshop, we will first review the latest state-of-the-art of hybrid emulation technologies and use-cases. We will then illustrate the application of hybrid emulation for pre-silicon benchmarking execution and optimization.

Break
11:15 AM – 11:30 AM

2A: CDC-RDC Standardization: Concepts & Status
11:30 AM – 1:00 PM
Forum 4
Speaker:
Jean-Christophe Brignone

CDC-RDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOCs having 2 trillion+ transistors and chiplets having 7+ SOCs. Today CDC verification has become a multifaceted effort across the chips designed for clients, servers, mobile, automotives, memory, AI/ML, FPGA, etc., with focus on cleaning up thousands of clocks and constraints, integrating the SVAs for constraints in validation environment to check for correctness, looking for power domain and DFT logic induced crossings, finally signing off with netlist CDC to unearth any glitches and corrupted synchronizers during synthesis.

As the design sizes increased in every generation, the EDA tools could not handle running flatly and the only way of handling design complexity was through hierarchical CDC-RDC analysis consuming abstracts. Also, hierarchical analysis helps to enable the analysis in parallel with teams across the globe. Even with all these significant progress in capabilities of EDA tools, the major bottleneck in CDC-RDC analysis of complex SOCs and Chiplets is consuming abstracts generated by different vendor tools. Different vendor tool abstracts are seen because of multiple IP vendors; even in-house teams might deliver abstracts generated with different vendor tools.

The Accellera CDC Working Group aims to define a standard CDC-RDC IP-XACT / TCL model to be portable and reusable regardless of the involved verification tool.

As moving from monolithic designs to IP/SOC with IPs sourced from small/select providers to sourcing IPs globally (to create differentiated products), the quality must be maintained as driving faster time-to-market. In areas where the standards (SystemVerilog, OVM/UVM, LP/UPF) are present, the integration is able to meet the above (quality, speed). However, in areas where standards (in this case, CDC-RDC) are not available, most options trade-off either quality, or time-to-market, or both :-(Creating a standard for interoperable collateral addresses this gap.

This tutorial aims to remind the definitions of CDC-RDC Basic Concepts and constraints, as well as the description of the reference verification flow, and addressing the goals, scope, structure & deliverables of the Accellera CDC Working Group in order to elaborate a specification of the standard abstract model.

A status related to the last LRM version open to public review by Q2 will be presented.

2B: Efficient SoC Modeling, Architectural Exploration, and Result Analysis using TLM2 based IPs
11:30 AM – 1:00 PM
Forum 5
Speakers:
Rocco Jonack, Matthias Jung and Jean-Blaise Pierrès

The advancement of semiconductor technology, characterized by shrinking feature sizes and the increasing viability of die-to-die and chip-to-chip interconnects, continues to drive the integration of complex electronic systems onto a single chip, giving rise to the paradigm of System-on-Chip (SoC) design. The ability to model the behavior of these intricate systems before committing to physical implementation is paramount. This tutorial addresses the critical need for efficient modeling, comprehensive architectural exploration, and insightful result analysis within the constraints of typical project lifecycles.

The increasing availability and maturity of pre-verified Intellectual Property (IP) blocks, such as CPUs, DRAM controllers, and interconnect fabrics, present an opportunity to shift the focus from low-level component modeling to system integration. By leveraging these readily available IPs, designers can concentrate on the critical aspects of system architecture, inter-component communication, and overall system behavior.

2B: Efficient SoC Modeling, Architectural Exploration, and Result Analysis using TLM2 based IPs (cont.)

This tutorial aims to bridge the gap between theoretical modeling techniques and practical SoC design workflows. We will explore strategies for accelerating the initial model generation process, enabling designers to rapidly prototype and evaluate different architectural configurations.

A key aspect of this tutorial is the usage of architectural exploration techniques. This will involve the use of simulation-based techniques to evaluate the impact of different architectural choices, such as the number and type of key initiators like CPUs, video processing units or accelerators, the memory hierarchy configuration, and the interconnect topology.

Generating tangible and actionable results from model simulations is crucial for both internal design optimization and effective customer communication. This tutorial will provide practical guidance on how to extract meaningful insights from simulation data, including performance metrics, power consumption profiles, and resource utilization statistics specifically in an open-source environment. We will explore techniques for visualizing and analyzing simulation results, enabling designers to identify bottlenecks, optimize resource allocation, and validate system performance. We will also discuss strategies for generating flexible reports that can be tailored to the specific needs of different stakeholders, including internal design teams, management, and customers.

The tutorial will be structured around a series of practical examples and case studies. We will begin by discussing the requirements for common system components, such as CPUs, DRAM controllers, and interconnects. We will then explore techniques for integrating these components into a unified platform, focusing on the challenges of inter-component communication and synchronization. We will present several illustrative platform examples, showcasing different SoC architectures and their associated use models. Finally, we will delve into the analysis of results from model simulations, demonstrating how to extract meaningful insights and generate actionable reports.

By attending this tutorial, participants will gain a comprehensive understanding of the challenges and opportunities associated with SoC modeling, architectural exploration, and result analysis. They will acquire practical skills and knowledge that can be immediately applied to their own SoC design projects, enabling them to accelerate development cycles, enhance product quality, and reduce time-to-market.

2C: Creating a Co-Simulation Environment for Questa Simulator Using QEMU
11:30 AM – 1:00 PM
Forum 6
Speakers:
Telat Işık, Faruk Karaahmet and Melike Karabalkan

This document gives information and step-by-step details on creating a co-simulation environment using QEMU for Questa Advanced Simulator.

2D: Tackling the cyber-physical system design challenges with MBSE and SystemC
11:30 AM – 1:00 PM
Forum 7
Speakers:
Karsten Einwich, Rolf Meyer and Petri Solanti

Mastering the interdisciplinary complexity of cyber-physical systems requires a holistic design methodology that can handle the specific needs of all implementation domains involved. Model-based systems engineering methodology backed by a versatile simulation technology provided by SystemC can tackle the design and verification challenges of cyber-physical systems. This tutorial demonstrates a holistic methodology for cyber-physical systems design.

2E: Cocotb and PyUVM tests powered with pytest
11:30 AM – 1:00 PM
Forum 8
Speakers:
Tymoteusz Blazejczyk, Abhiroop Bhowmik, Ronahi Halitoglu and Shrinivas Naik

Audience target: RTL verification engineers who are currently using or want to start using Cocotb, optionally with PyUVM. This tutorial is for those looking for significant improvements in their current Way-of-Working (WoW), especially with discovering, managing, and running a large number of tests.

Cocotb and PyUVM already provide significant Quality-of-Life (QoL), workflow, ecosystem, and productivity improvements to the RTL verification landscape. They overcome limitations and flaws from classic approaches like using SystemVerilog + UVM and in-house tooling and flows.

Currently, Cocotb encourages using pytest, the most popular Python testing framework, to manage, build, and run HDL simulations with Cocotb using Python. This is an alternative to custom in-house solutions, mostly based on Makefiles, TCL, or shell scripts.

Pytest is a very popular and powerful testing framework available in Python. It allows you to easily discover, introspect, and manage a large number of tests. Pytest's built-in plugin facility allows you to extend pytest and verification environment capabilities by creating new plugins or using existing ones. These can range from generating HTML reports to CI integration with custom or external flows. It also extends test re-usability and provides a clean setup/teardown context solution for tests by introducing a modern approach with fixtures. Pytest parametrization eliminates duplicate code for testing multiple sets of input and output. Rewritten assert statements provide detailed output for causes of failure.

Unfortunately, current documented Cocotb examples show pytest usage in a very narrow, specific use case: to only build and run HDL simulations without using all available pytest capabilities directly in Cocotb or PyUVM tests to extend the overall verification experience.

At Qblox, we strive to use tools to their fullest to boost our development productivity and deliver top-class, high-quality products to our customers in the quantum field, which are constrained by tight requirements and high expectations. We want to share our experience with the industry and verification community on how to achieve that by leveraging Python + Cocotb + PyUVM + pytest together.

1:00 PM - 3:00 PM
Lunch & Expo Hours
Room: Großer Saal

3A: Unleashing the Potential of AI Within Functional Verification
3:00 PM - 4:30 pm
Forum 4
Speakers:
Darron May and Joseph Hupcey

SIEMENS

FIn the rapidly evolving landscape of semiconductor design, the complexity and scale of digital circuits continue to grow exponentially. Traditional methods of Register-Transfer Level (RTL) functional verification are increasingly challenged by these advancements, necessitating innovative approaches to ensure robust and efficient verification processes. This technical workshop aims to explore the integration of Artificial Intelligence (AI) and Machine Learning (ML) into RTL functional verification workflows, showcasing new products and methodologies that leverage these cutting-edge technologies.

The workshop will feature a comprehensive overview of the current state of RTL functional verification, highlighting the limitations and bottlenecks faced by verification engineers. We will introduce a suite of new AI/ML-powered tools designed to enhance verification efficiency, accuracy, and coverage. These tools employ analytical, predictive, and generative AI to automate pattern recognition, detect anomalies, generate "right by construction" artifacts like code and assertions, significantly reducing the time and effort required for verification tasks.

3A: Unleashing the Potential of AI Within Functional Verification (cont.)

Via the following presentations on "smart" automation for design and testbench creation, debug and regression acceleration, engine optimizations, and collaborative coverage analysis, participants will be able to map their needs to these new AI/ML-accelerated flows using faster engines, enabling faster engineers and optimizing resources with fewer workloads:

1. Introduction to AI/ML in RTL Verification: Understanding the basics of AI/ML and their applicability to RTL verification.
2. New AI/ML-Driven Verification Tools: Demonstrations of the latest products incorporating AI/ML engines, including their features, benefits, and use cases.
3. Case Studies and Real-World Applications: Insights from industry leaders on successful implementations of AI/ML in RTL verification, showcasing tangible improvements in verification outcomes.
4. Future Trends and Challenges: Exploring the future potential of AI/ML in verification and addressing the challenges associated with their adoption.

By the end of the workshop, attendees will have a deeper understanding of how AI/ML can transform their overall approach to RTL functional verification, driving innovation and efficiency in their verification processes.

Join us to stay ahead of the curve and harness the power of AI/ML to tackle the complexities of modern RTL D&V!

3B: Property Generator: simple generation of Formal Assertion IP
3:00 PM - 4:30 pm
Forum 5
Speakers:
Tobias Ludwig and Osama Ayoub

LUBIS EDA

The Property Generator is a proprietary tool developed by LUBIS EDA to simplify and accelerate formal verification. It results in correct-by-construction assertions, which are human-readable and remove the need for assertion review.

The verification journey begins with writing a SystemC model that expresses functional intent. This model can be simulated using standard C++ and SystemC techniques, helping designers and verification engineers validate functionality early. The Property Generator then analyzes the model to auto-generate assertions that comprehensively describe the expected behavior.

After generation, the assertions are loaded together with the design into your formal tool of choice or a simulator. In a typical setup, these assertions must be manually bound to RTL design signals—a process that is time-consuming and error-prone. To address this, the Property Generator integrates an AI-Refinement add-on, powered by Large Language Models (LLMs). These models can interpret both the abstract model and RTL structure, performing the refinement step with high accuracy and minimal user intervention.

What makes our generations special is that we generate assertions to ease proof complexity by generating a large number of simple, focused properties, rather than a few complex ones. These simpler properties are easier to prove individually. Once the design is verified, only the abstract model needs review, significantly reducing sign-off time.

By using our tool, we enable more people to use formal verification and kick-start their formal journey.

3C: Next-Gen Verification Technologies for Processor-Based Systems

3:00 PM - 4:30 pm

Forum 6

Speakers:

Bjoern Hartmann, Synopsys Inc.; Oguzhan Turk, Synopsys Inc.

Today's complex processor-based systems enable technological advances in many market segments, such as AI, high performance computing, and automotive. However, verification of these systems introduces new challenges. In this tutorial, we will focus on RISC-V processors and present next-generation verification techniques that accommodate the flexible and evolving nature of the RISC-V ISA, as well as privilege mode features, out-of-order pipelines, interrupts and debug mode. We will cover dynamic and formal approaches to verify RISC-V cores, with topics including, but not limited to: ISA compliance verification and functional coverage, data path validation, functional verification of critical blocks, and security verification. This tutorial provides a comprehensive verification walkthrough of a RISC-V example core to illustrate these concepts. Whether you are designers or verification engineers of these complex processor-based systems, you will walk away with new ideas on how to improve your verification flow by embracing these next generation solutions.

3D: Will it Blend? - Verifying the Hardware / Software Interface of complex SoCs

3:00 PM - 4:30 pm

Forum 7

Speakers:

Tim Schneider, Insaf Meliane and Alvin Santos

Verification of modern System on Chip (SoC) designs involve many components. Hardware Description Languages (VHDL, System Verilog), Unified Power Format (UPF), Software Languages (C#/C++), Interconnect standards (IP-XACT, AMBA), and specialty purpose-built layers such as the Universal Verification Methodology (UVM) and System Verilog Assertions (SVA). This tutorial explores using Arteris SoC Integration technologies to "blend" these components together by proposing a more efficient methodology to increase productivity and help ensure first-time SoC project success.

3E: Scalable Virtual Platforms for Automotive and Beyond

3:00 PM - 4:30 pm

Forum 8

Speakers :

Lukas Jünger, Matthias Berthold and Nils Bosbach Nils Bosbach

The shift toward software-defined vehicles demands a radical rethinking of how automotive software is developed and tested. Virtual Platforms (VPs) – or Level 4 Virtual Electronic Control Units (L4 vECUs) – have emerged as a key enabler in this transformation, offering scalable, flexible, and hardware-independent environments for early and continuous software validation. This tutorial explores the practical and technical foundations of using VPs in automotive software testing, highlighting their role in accelerating development cycles, improving test coverage, and reducing reliance on physical prototypes. Participants will gain insights into building VPs using open-source technologies, integrating them with modern testing and automation toolchains, and leveraging detailed simulation models to represent complex SoCs and IP components. Furthermore, the tutorial delves into performance optimization strategies, drawing from both industry practices and academic research to address the challenges of simulation speed and scalability. By bridging the gap between hardware abstraction and software validation, VPs are reshaping the automotive development landscape. This session equips engineers, researchers, and toolchain architects with the knowledge to effectively deploy and scale virtual testing environments in real-world automotive workflows.

Attendee Coffee Break & Expo Hours

4:30 PM - 5:15 PM

Room: Großer Saal

4A: Tutorial on the Improvement introduced by IEEE 1801-2024 (UPF4.0) Standard for the Specifications, Implementation and Verification of Low Power intent

5:15 PM - 6:45 PM

Forum 4

Speakers:

Joshua Ong, Nathalie Meloux, Gabriel Chidolue and Shaun Durnan

As advanced low-power architectures have become more pervasive in industry, the complexity of these architectures has driven new methodologies for the verification, implementation, and reuse of power intent specifications. Modern low-power designs place requirements that span from enabling more flexible IP design reuse to providing well-defined interfaces between analog and digital components in simulation. The IEEE 1801-2024 (UPF 4.0) standard provides several key enhancements that are required to keep pace with these innovations in low-power design. The tutorial is based on the DVCON 2025 US Workshop titled "Introduction of IEEE 1801-2024 (UPF4.0) Improvements for the Specification, Implementation and Verification of Low-Power Intent". The tutorial will provide an overview of the enhancements to the standard from both conceptual and command levels. New concepts such as virtual supply nets, refinable macros, and UPF libraries will be introduced, as well as re-architected features with respect to interfacing between analog and digital simulation and advanced state retention modeling for enhanced semantics. While the new IEEE 1801-2024 standard provides numerous detailed clarifications and enhancements to the previous version, this workshop will focus on the key changes that will impact most designers and changes that enable new functionality.

4B: Expediting Coverage Closure in Digital Verification with the Portable Stimulus Standard (PSS)

5:15 PM - 6:45 PM

Forum 5

Speakers:

Tulio Pereira Bitencourt, Nikolaos Ilioudis, Ahmed Abd-Allah, Daniel Waszczak, Anton Tschank and Tom Fitzpatrick

The semiconductor industry is in an ever-growing and evolving process, where complexity is increasing to cope with the necessity for optimized integrated circuits (IC) that are more robust and reliable. Among many requirements, the need for systems that can execute different tasks and interconnect with multiple other devices emerges as critical, which compromises testing capabilities as one shall now deal with complicated designs.

Portable Stimulus Standard (PSS) from Accellera tackles this complexity by allowing test cases to be executed at different levels of abstraction, such as during the verification procedure using SystemVerilog and UVM (Universal Verification Methodology) or when prototyping a Register-Transfer Level (RTL) circuit in a field-programmable gate array (FPGA). PSS was released by Accellera in 2018 and has been added into Electronic Design Automation (EDA) tools ever since, with a rising number of companies using it. Specifically for the digital verification phase for application-specific integrated circuits (ASICs), PSS can be used on top of UVM to enhance its capabilities and allow for dynamic test cases, the so-called scenarios, to be randomly created prior to simulations. PSS relies on a task-based system where independent operations can be defined as either UVM sequences or virtual sequences, and a PSS-compatible tool generates scenarios based upon rules described in a PSS model file. Using PSS combined with UVM allows for many test cases to be effortlessly randomized solely based upon three critical files: PSS test, PSS model, and list of tasks. This approach significantly optimizes bug finding and coverage closure times, as random scenarios can swiftly create a wide range of stimuli to RTL designs.

4C: Introduction to the Apheleia Verification Library

5:15 PM - 6:45 PM

Forum 6

Speakers:

Andy Bond

In the 20 years since UVM was introduced, bringing a common structure and methodology to re-usable verification environments, much has changed in both the designs under verification and the technology available. AVL (Apheleia Verification Library) is an open-source Python library focusing on the user experience and efficiency, while retaining the scalability and re-use mentality of UVM.

This tutorial will walk participants through their first AVL test-bench, introducing the features, key differences and potential efficiency gains vs. UVM. In addition, the tutorial can be run on any mid-level laptop, with no requirement for commercial tools or licenses demonstrating the potential benefits to students, hobbyists and early-stage innovators who wish to focus on innovation without requiring significant up-front investment.

4D: Teaching Analog CMOS Chip Design using Open-Source Tools

5:15 PM - 6:45 PM

Forum 7

Speakers:

Ted Johansson

Microelectronics are essential for all products with just a little bit of technology inside. The COVID-19 pandemic exposed vulnerabilities in global supply chains, particularly in the automotive sector, which faced production disruptions due to a shortage of critical chips, mainly produced in Asia. EU and USA Chips Act programs have regained the focus on fabrication of semiconductors, new devices, circuit design, and the supply chains. In the next couple of years, huge amounts of money, shared between government and industry, will be spent on rebuilding the semiconductor industry in Europe and USA.

However, during the last 25 years, this area has not attracted students. We need to educate a new generation of engineers and researchers on semiconductors and circuit design. To meet the foreseen need of education and training, Uppsala University is developing new courses in electronics, semiconductors, circuit and chip design, and manufacturing technology. These courses will range from continuing education to engineering programs and doctoral studies.

In the tutorial, I will describe how we created a PhD course (which will also be offered to master programs in 2025/26) on analog IC design, addressing the design chain, tools, and everything you need to know to design and have chips fabricated at a foundry using only open-source tools and PDKs.

4E: Standardization of Multi-Physics Interfaces and Model Exchange Mechanisms

5:15 PM - 6:45 PM

Forum 8

Speakers:

Sumit Adhikari, Heiko Schick and Daniel Hedberg

The increasing prevalence of tightly-coupled, multi-physics systems across domains such as electronics, electromagnetics, thermal, mechanical, and fluidic design necessitates standardized methods for model interchange and tool interoperability. Current industrial workflows rely on heterogeneous, proprietary interfaces and loosely defined integration schemes, leading to inefficiencies in co-simulation fidelity, model portability, and system verification. To address this gap, we propose a workshop to define the scope and objectives of a prospective Accellera Working Group dedicated to the standardization of interface definitions and model exchange formats for multi-physics design environments. The workshop will convene stakeholders from industry, academia, and tool vendors to: 1) Identify core interoperability challenges in multi-physics workflows; 2) Examine existing solutions (e.g., FMI, Modelica, SystemC, SystemC-AMS) and their limitations in heterogeneous domain coupling;

4E: Standardization of Multi-Physics Interfaces and Model Exchange Mechanisms (cont.)

3) Delineate candidate requirements for a unified interface abstraction supporting cross-domain semantics, co-simulation control, and metadata exchange; 4) Formulate initial charter language, use case classes, and a phase-wise deliverable roadmap for the proposed working group; 5) Assess opportunities for alignment with existing Accellera standards and external consortia.

Break
6:45 PM - 7:30 PM

Conference Dinner
7:30 PM - 10:30 PM
Location: Hofbräukeller - Innere Wiener Straße 19 - 81667 München

Sponsored by: AMIQ

Program: Wednesday, October 15th

Opening Session
8:15 AM - 8:30 AM
Ballsaal

Keynote Speaker: Ralph Schleifer, CARIAD Management
8:30 AM - 9:30 AM
Ballsaal

Driving Forward: The Evolution of Virtual Development in the Automotive Industry

Abstract: We will explore the transformative journey of virtual development within the automotive industry over the past years, delve into expectations set a few years back, examining the ambitious goals and visions. Through a detailed analysis, we will highlight advancements achieved, including innovation in simulation technologies, digital twins, and virtual testing environments. Additionally, we will address the challenges faced and the lessons learned along the way. This speech aims to provide an overview of how virtual development has evolved in the industry. Join us as we reflect on the past, celebrate the present, and envision the future of virtual development in automotive engineering.

Biography: Ralph Schleifer, CARIAD SE, is heading Virtual ECUs and Simulation at CARIAD. Before joining the automotive industry in 2015, Ralph has been active in different fields of mobile communication at Ericsson in SW development, speech processing research, system engineering, DSP sub systems and Virtual Prototypes. Ralph holds a M.Sc. degree in Electrical Engineering. He has established virtual development methodology on different abstraction levels along the automotive supply chain first within Audi and now at CARIAD. He has been active in various areas of Virtual Development for more than 15 years.

Exhibit Hall Open
9:30 AM - 4:30 PM
Großer Saal

Attendee Coffee Break & Expo Hours
9:30 AM - 10:00 AM
Großer Saal

Session 5A: AI and Machine Learning for Verification & Coverage
10:00 AM - 12:00 PM
Forum 4
Session Chair: Martin Ruhwandl

#144 AI-Powered Hardware Verification: Your Non-Human Friend in Action (Engineering Paper)
Sreedevi Sreekaladevi, Deepak Narayan Gadde, Aman Kumar, Johannes Grinschgl, Linus Maurer and Georg Pelz

#170 LLM-based Functional Coverage Generation and Auto-Evaluation Framework (Research Paper)
Ján Labuda, Marcela Zachariášová and Zdeněk Matěj

#129 Fast, Flexible, Timing-accurate and Open Source Performance Modeling Method for Compute Accelerators (Engineering Paper)
Vishal Chovatiya, Andrew Stevens and Snehith Shenoy

#130 Accelerating Coverage Closure with Reinforcement Learning: A Case Study on FSM Verification (Engineering Paper)
Tijana Misic

Session 5B: Formal & Symbolic Approaches to Digital Verification
10:00 AM - 12:00 PM
Forum 5
Session Chair: Bryan Daniel Olmos Suquillo

#100 Accelerate Verification of Complex Hardware Algorithms using MATLAB based SystemVerilog DPIs (Engineering Paper)
Samuele Candido

#158 Transformation-Aided Verification of MAC Designs using Symbolic Computer Algebra (Research Paper)
Lennart Weingarten, Kamalika Datta and Rolf Drechsler

#107 Advancing Open-Source Verification: Enabling Full Randomization in Verilator (Engineering Paper)
Yilou Wang

#95 FPGA Firmware Verification: a common approach for simulation and hardware tests (Engineering Paper)
Stefano Pavinato, Stephane Gabourin and Emmanuel D'Costa

Session 5C: Mixed-Signal and Power-Aware Verification
10:00 AM - 12:00 PM
Forum 6
Session Chair: Clemens Süßmuth

#110 Early Chip-Level Power Estimation using Digital Mixed-Signal Simulations (Engineering Paper)
Ricardo Dantas, Akib Zaidi and Gabriela Alecu

#154 Performance Evaluation of a Phase-Locked Loop using Variation-Aware Behavioral Models (Research Paper)
Neha Chavan, Jan Rödel, Carna Zivkovic and Christoph Grimm

#102 Implementing Functional Coverage for Analog IPs in Mixed-Signal Verification Environments (Engineering Paper)
Akib Mohammad Azam Zaidi and Ana-Maria Radu

#131 Real Number Voltage aware behavioral modeling and verification of SRAM subsystem with Unified Power Format (UPF) (Engineering Paper)
Isha Sharma and Amit Singh

Session 5D: Virtual Prototyping and System-Level Simulation
10:00 AM - 12:00 PM
Forum 7
Session Chair: Thorsten Dworzak

#108 Cloud-Enabled Virtual Prototypes (Engineering Paper)
Tim Kraus, Axel Sauer and Ingo Feldner

#126 Simulation Time Federation using the Zenoh framework between SystemC's and QEMU (Engineering Paper)
Mark Burton, Mahmoud Kamel and Alwalid Salama

#151 Automated Flow to Maintaining Consistency in Parallel Design Representations Using Cross-Level Verification (Engineering Paper)
Javier Castillo, Mohammad Badawi and Jan-Hendrik Oetjens

#125 Offloading Complex Mathematical Computations in System Verilog Testbenches - Asyncronous verification of ethernet Reed-Solomon forward error correction using third-party Python packages (Engineering Paper)
Simon Coulter

Session 5E: Functional Safety and Security
10:00 AM - 12:00 PM
Forum 8
Session Chair: Asheque Mohammad Zaidi

#94 A pragmatic Approach to apply HEAVENS Threat-Level for Attack Feasibility Determination as per ISO/SAE 21434 Recommendations RC-15-11 and RC-15-12 (Engineering Paper)
Clemens Röttgermann, Tanja Schülting and Frauke Blossey

#163 Pre-Silicon Verification of Software Safety Mechanisms: A Hybrid Approach with SPI and NVDLA Case Studies (Engineering Paper)
Moustafa Nabil, Ahmed Makram, Mohamed Nasser, Ahmed Saied and Sherif Khourshed

#172 Minimally Intrusive Safety and Security Verification of Rust RTIC Applications (Research Paper)
Pawel Dzialo, Ivar Jönsson, Malte Munch, Erik Serrander, Johan Eriksson and Per Lindgren

#133 A Generic Functional Safety Vector UVC (Engineering Paper)
Kilaru Vamsikrishna, Siril Roy, Raghav Sharma and Sushrut B Veerapur

Lunch & Expo Hours
12:00 PM - 1:00 PM
Großer Saal

Panel
1:00 PM - 2:00 PM
Ballsaal

Beyond the Chip: How Ecosystems Are Shaping the Future of System Design
Moderator: Axel Jahnke, Nokia

Panelists:

- Moussa Belkhiter, STMicroelectronics
- Andrew Dellow, Qualcomm/RISC-V Ambassador
- Ralph Schleifer, CARIAD Management
- Sara Vinco, Politecnico di Torino

In today's rapidly evolving technological landscape, the development of system(-of-systems) solutions plays a critical role in driving innovation across various industries. The ecosystems that support these developments are fundamental to this process, providing the necessary tools, resources, and collaborative environments to enable efficient and effective design and implementation.

In this panel, we explore the multifaceted world of ecosystems and their broader implications for system design as a whole.

Our conversation will cover the following key areas:

- Open or proprietary development Ecosystems: Understanding the various ecosystems that support SoC development, including open-source and proprietary platforms, and how they contribute to innovation and efficiency.
- Integration with System Design: Exploring how ecosystems extend beyond chip-level design to influence overall system architecture, performance, and scalability.
- Tools and Methodologies: Discussing the tools, methodologies, and best practices to sustain broader system design, ensuring seamless integration and optimized performance.
- Challenges and Solutions: Identifying the challenges faced in system-level design and exploring strategies to address these challenges effectively.

Future Trends: Envisioning the future of system design, including emerging technologies, trends, and their potential impact on various industries: what about Artificial Intelligence and Machine Learning, Edge Computing, Security and Privacy, and Sustainability?

Program: Wednesday, October 15th (cont.)

Break
2:00 PM - 2:15 PM

Session 6A: Next Generation UVM Testbenches
2:15 PM - 3:45 PM
Forum 4
Session Chair: Uwe Simm

#132 Unified UVM Testbench: Integrating Random, Directed and Pseudo-Random Verification Capabilities (Engineering Paper)
Kilaru Vamsikrishna, Shaikh Salehabibi, Amitav Mitra and Sushrut B Veerapur

#116 Evaluating the Usability of pyuvm with cocotb for UART Verification (Engineering Paper)
Mihir Ashvinbhai Donga, Eyck Jentzsch and Juergen Mottok

#101 A Novel Configurable UVM Architecture To Unlock 1.6T Ethernet Verification (Engineering Paper)
Sameh El-Ashry

Session 6B: Innovative and Reusable Verification Methodologies
2:15 PM - 3:45 PM
Forum 5
Session Chair: Andrei Vintila

#139 Out of the Box Techniques for Data Path Verification (Engineering Paper)
Atharva Kakde, Ketki Gosavi, Pradeep Bagavathiappan and Anshul Singhal

#124 Reduce, Reuse, Reverify: A green approach in formal verification from PCIe Gen6 to Gen7 Environment (Engineering Paper)
Md Zahid Fazal, Moola Jeevan Chaitanya Goud, Hamish Hendry and Sakthivel Ramaiah

#127 Comprehensive & Configurable Ethernet IP Verification Strategy (Engineering Paper)
Tom O'Connor, Sameh El-Ashry, Atif Ansari, Vinaykumar Kori, Simon Coulter, Afroz Alam and Paul Drum

Session 6C: Advances in Virtual Platform Integration
2:15 PM - 3:45 PM
Forum 6
Session Chair: Daniele Ludovici

#160 Integrating SystemC TLM into FMI 3.0 Co-Simulation with an Open-Source Approach (Research Paper)
Andrei Mihai Albu, Giovanni Pollo, Alessio Burrello, Daniele Jahier Pagliari, Cristian Tesconi, Loris Panaro, Dario Soldi, Fabio Autieri and Sara Vinco

#123 Federated Simulation of Virtual Platforms using the Open-Source SIL Kit Library (Engineering Paper)
Jakob Engblom

#120 Improving Flexibility in Hardware-Software Co-Development with Remote Virtual Prototypes (Engineering Paper)
Przemysław Mikluszka and Patryk Górniak

Session 6D: Debugging and Formal Methods in Verification
2:15 PM - 3:45 PM
Forum 7
Session Chair: Rafal Baranowski

#98 Time-Travel Debugging for HLS Code (Engineering Paper)
Jonathan Bonsor-Matthews, Greg Law, Chirag Goyal and Mark Williamson

#166 DRAMPyML: A Formal Description of DRAM Protocols with Timed Petri Nets (Research Paper)
Derek Christ, Thomas Zimmermann, Philippe Barbie, Dmitri Saberi, Yao Yin and Matthias Jung

#165 Advanced State Space Tunneling: Debug Your Formal Complexity Using Waveforms (Engineering Paper)
Diego Hernandez, Erik Seligman, Lars Lundgren, Mariane Goncalves, Gustavo Junqueira, Tulio Leao, Gabriela Bahia, Hakan Hjort, Craig Deaton and Varun Ramesh

Session 6E: AI and Automation in Verification Workflows
2:15 PM - 3:45 PM
Forum 8
Session Chair: Vikas Sachdeva

#118 Fully Automated Verification Framework for Configurable IPs: From Requirements to Results (Engineering Paper)
Shuhang Zhang, Jelena Radulovic and Thorsten Dworzak

#134 ChipDesign DevOps – from sometimes working to almost never broken (Engineering Paper)
Johannes Koesters, Udo Krautz, Jeff Brownscheidle and Lou Schmidt

#169 GAIL-V: Generative AI Leveraged - Verification : A systematic framework for leveraging generative AI in verification (Engineering Paper)
Sriram Madavswamy and Daniel Larkin

Attendee Coffee Break & Expo Hours
3:45 PM - 4:15 PM
Großer Saal

Session 7A: Scalable Verification through Automation and Formal Methods
4:15 PM - 5:45 PM
Forum 4
Session Chair: Thomas Klotz

#105 The Test Bench Factory: Building Verification Environments Faster, Better, Smarter (Engineering Paper)
Thorsten Dworzak and Johannes Grinschgl

#164 Exploring the Limits of Vertical Reuse Automation in PSS-Driven SoC Verification (Engineering Paper)
Petr Bardonek, Alessandra Dolmeta, Marcela Zachariášová and Guido Masera

#115 ACT with Confidence: Formal Verification of Packet Based Designs using Array Centric Tracking (Engineering Paper)
Anka Babu Appikatla and Sakthivel Ramaiah

Session 7B: Coverage Reuse and Model Based UVM
4:15 PM - 5:45 PM
Forum 5
Session Chair: Johannes Grinschgl

#152 Efficient Coverage Optimization with Formal-Guided Testcase Generation in UVM Verification (Research Paper)
Yu-Shien Shen, Yean-Ru Chen, Yu-Tung Chen and En-Hsiang Lin

#143 Vertical Reuse of Reference Models in UVM (Engineering Paper)
Joachim Geishauser, Ciro Ceissler and Leo Tran

#135 A Graph-Based UVM Generation Framework for Complex State Machine Verification (Engineering Paper)
Francois Cerisier, Philippe Ledent and Eric Hargous

Program: Wednesday, October 15th (cont.)

Session 7C: Mixed Signal Verification and Automation
4:15 PM - 5:45 PM
Forum 6
Session Chair: Karsten Einwich

#140 Automated PDF Reporting in MSV Workflow (Engineering Paper)
Kostiantyn Barabanov and Clemens Suessmuth

#104 DMS Verification Environment for Gyroscope System (Engineering Paper)
Thierry Nouguier, Ajay G Nayak and Fabrice Boissieres

#136 A UVM Testbench for Exploring Design Margins of Analog/Mixed-Signal Circuits: A PCI-Express Receiver Detection Circuit Example (Engineering Paper)
Jaeha Kim

Session 7D: Virtual Prototyping and Digital Twin Applications
4:15 PM - 5:45 PM
Forum 7
Session Chair: Sara Vinco

#167 Leveraging RISC-V for Flexible and Adaptive Real-Time Radar Sequencing (Research Paper)
Michael Atzmüller, Rainer Findenig, Bernhard Greslehner-Nimmervoll, Wolfgang Ecker and Daniel Grosse

#121 Harnessing a Digital Twin for Personalized Type-1 Diabetes Care: A Model for Glucose Control and Insulin Administration (Engineering Paper)
Ammar Abdelghany, Mohamed Hamed, Asmaa Khaled, Nada Alfowey, Tamer Basha, Loai Ali and Mohamed Abdelsalam

#128 A Framework for Reusability of Virtual Realtime Systems (Engineering Paper)
Sacha Loitz, Torsten Hermann and Martin Hruschka

Session 7E: AI and Infrastructure
4:15 PM - 5:45 PM
Forum 8
Session Chair: Francois Cerisier

#142 AI Pair or Despair Programming, Using Aider to build a VIP with UVM-SV and PyUVM (Engineering Paper)
André Winkelmann and Damir Ahmetovic Ignjic

#112 GAP: A Generic Agent Pattern for Reusable Testbenches (Engineering Paper)
Omar Younis and Peter Gad

#137 How Docker containers can make chip development more productive (Engineering Paper)
Philipp Wagner, Holger Horbach, Martijn Berkers, Udo Krautz and Johannes Kösters

Closing Session & Best Paper Award
5:45 PM – 6:15 PM
Großer Saal Foyer

SYSTEMC EVOLUTION DAY 2025

SystemC Evolution Day events are an opportunity for the whole SystemC community to come together. The days are intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community, tool providers and the Accellera Working Groups to advance SystemC standards.

SystemC Evolution Day events are full-day, in person events, divided into several in-depth sessions. Selected current and future standardization topics around SystemC are discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day events are co-located with DVCon Europe, on the day after the main conference.


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