2024
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DVCON
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EUROPE
MUNICH, GERMANY
OCTOBER 15-16, 2024

DVCON EUROPE 2024
CONFERENCE PROGRAM

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Welcome Message from DVCon Europe General Chair,

Mark Burton
General Chair - Qualcomm

Dear Colleagues and Friends,

Welcome to DVCon Europe 2024!

I have been at every DVCon Europe since it's conception over a decade ago, and now I am absolutely honored to play my part as the General Chair, continuing to foster and grow what has become an institution in our industry. This year, I'm really pleased to announce that we are introducing a new SystemC competition, which I know will be a highlight of the conference. So, I'm thrilled to gather once again in this dynamic forum, where innovation, collaboration, and knowledge sharing drive the advancements in the design and verification community.

Our industry is at the forefront of technological transformation, and DVCon Europe stands as a beacon for professionals dedicated to pushing the boundaries of what is possible in Electronic Design Automation (EDA), verification, and embedded systems. This year, we have curated an exciting program that encompasses a diverse range of technical sessions, insightful keynotes, and interactive panel discussions. DVCon Europe has a history of pivotal keynote speakers and this year will be no exception as we welcome two keynote speakers that we're extremely lucky to have as they are at the forefront of the AI and Automotive industries.

As always, this year's conference will feature cutting-edge paper presentations and tutorials from leading experts, offering deep dives into the latest methodologies, tools, and techniques. Whether you are a seasoned veteran or new to the field, you will find sessions tailored to your interests and expertise. One of our core missions is to foster an environment where engineers, researchers, and industry leaders can connect and exchange ideas. The research track was a great success last year, and I'm please to say that it has further expanded this year.

For the first time, we will be hosting the DVCon Europe SystemC Modeling Challenge, designed to showcase the skills of our talented attendees. This competition promises to be thrilling, providing participants with an opportunity to demonstrate their expertise and creativity in SystemC. Additionally, we have extended our reception to offer even more opportunities for networking and collaboration providing the perfect setting to connect with peers, discuss ideas, and forge new professional relationships in a relaxed and engaging atmosphere.

There will be additional opportunities for more spontaneous interactions in our exhibition hall which will showcase the latest products and services from top companies in the industry. And finally, our social events are designed to help you build and strengthen professional relationships while having a little fun.

I would like to extend my heartfelt thanks to our sponsors, exhibitors, and the DVCon Europe organizing committee, as well as the technical program committees and reviewers, who are all volunteers. Your unwavering dedication make this event possible, and your support this year has been, as ever, invaluable.

As we embark on this exciting journey over the next few days, I encourage you to immerse yourself fully in the experience. Engage with the speakers, participate in discussions, and explore the innovative solutions on display. Together, we can drive the future of design and verification.

Thank you for being a part of DVCon Europe 2024. Let's make this an unforgettable event!

Warmest regards,

Mark Burton,
DVCon Europe 2024 General Chair

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Accellera Systems Initiative is an independent, not-for profit organization dedicated to create, support, promote, and advance system-level design, modeling, and verification standards for use by the worldwide electronics industry. We are composed of a broad range of members that fully support the work of our technical committee to develop technology standards that are balanced, open, and benefit the worldwide electronics industry. Leading companies and semiconductor manufacturers around the world are using our electronic design automation (EDA) and intellectual property (IP) standards in a wide range of projects in numerous application areas to develop consumer, mobile, wireless, automotive, and other "smart" electronic devices. Through an ongoing

partnership with the IEEE, standards and technical implementations developed by Accellera Systems Initiative are contributed to the IEEE for formal standardization and ongoing governance.

Our Mission

At Accellera our mission is to provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

The purposes of the organization include:

- Provide design and verification standards required by systems, semiconductor, IP, and design tool companies to enhance a front-end design automation process.
- Collaborate with our community of companies, individuals, and organizations to deliver standards that lower the cost of designing commercial IC and EDA products and embedded system solutions, as well as increase the productivity of designers worldwide.
- Encourage availability and adoption of next-generation EDA and IP standards that encompass system-level, RT-level, and gate-level design flows.
- Collaborate with the electronic design community to deliver standards that increase designer productivity and lower the cost of product development.
- Provide mechanisms that enable the continued growth of the Accellera Systems Initiative user community including SystemC, Universal Verification Methodology (UVM), and IP-XACT.
- Standardize technical implementations developed by Accellera Systems Initiative through the IEEE.

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Program Grid - Day 1 - Tutorials - October 15

	Forum 4	Forum 5	Forum 6	Forum 7	Großer Saal
8:00 - 8:15 AM	**Opening Session** (Ballsaal)				
8:15 - 9:15 AM	**Keynote Speaker: Thomas Boehm** (Ballsaal)				
9:15 - 9:45 AM	**Attendee Coffee Break** (Großer Saal)				**Exhibit Hall Open**
9:45 - 11:15 AM	**T1.1** G-QED for Pre-Silicon Verification	**T2.1** Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model	**T3.1** Unleash the Full Potential of Your Waveforms: From Extra-functional Analysis to Functional Debug via Programs on Waveforms	**T4.1** A detailed tour of IEEE standard P3164	
11:15 - 11:30 AM	**Break**				
11:30 - 1:00 PM	**T1.2** Calling All Engines – Faster Coverage Closure with Simulation, Formal, and Emulation SIEMENS	**T2.2** Modernizing the Hardware / Software Interface - Life beyond spreadsheets. How to bring your SoC register design into the 21st Century ARTERIS IP	**T3.2** Developing Complex Systems using Model-Based Cybertronic Systems Engineering Methodology SIEMENS	**T4.2** USF-based FMEDA-driven Functional Safety Verification cadence	
1:00 - 2:00 PM	**Lunch** (Großer Saal)				
2:00 - 3:30 PM	**T1.3** cocotb 2.0: How to get the best out of the new major version of the Python-based testbench framework	**T2.3** QEMU and SystemC (QBox) tutorial	**T3.3** Scalable HW Performance Assessment	**T4.3** Novel Approach to Verification and Validation (V&V) for Multi-die Systems	
3:30 - 4:00 PM	**Attendee Coffee Break** (Großer Saal)				
4:00 - 5:30 PM	**T1.4** A Holistic Approach to RISC-V Processor Verification SYNOPSYS	**T2.4** Comprehensive Glitch Signoff – Learnings and experiences from industry use cases REAL INTENT	**T3.4** Efficient AI: Mastering Shallow Neural Networks from Training to RTL Implementation MathWorks	**T4.4** Exploring the Next-Generation of Debugging with Verification Management and Integrated Development Environment SYNOPSYS	
5:30 - 7:30 PM	**Reception** (Großer Saal)				

Program Grid - Day 2 - October 16

	Forum 4	Forum 5	Forum 6	Forum 7	Forum 8	Großer Saal
8:15 - 8:30 AM	**Opening Session** (Ballsaal)					
8:30 - 9:30 AM	**Keynote Speaker: Erik Norden** (Ballsaal)					
9:30 - 10:00 AM	**Attendee Coffee Break** (Großer Saal)					**Exhibit Hall Open**
10:00 - 11:00 AM	**Session 1A**	**Session 1B**	**Session 1C**	**Session 1D**	**Session 1E**	
11:00 - 11:15 AM	**Break**					
11:15 - 12:00 PM	**Session 2A**	**Session 2B**	**Session 2C**	**Session 2D**	**Session 2E**	
12:00 - 1:00 PM	**Lunch** (Großer Saal)					
1:00 - 2:00 PM	**Panel** (Ballsaal)					
2:00 - 2:15 PM	**Break**					
2:15 - 3:45 PM	**Session 3A**	**Session 3B**	**Session 3C**	**Session 3D**	**Session 3E**	
3:45 - 4:15 PM	**Attendee Coffee Break** (Großer Saal)					
4:15 - 5:45 PM	**Session 4A**	**Session 4B**	**Session 4C**	**Session 4D**	**Session 4E**	
5:45 - 6:15 PM	**Closing Session & Best Paper Award** (Ballsaal)					

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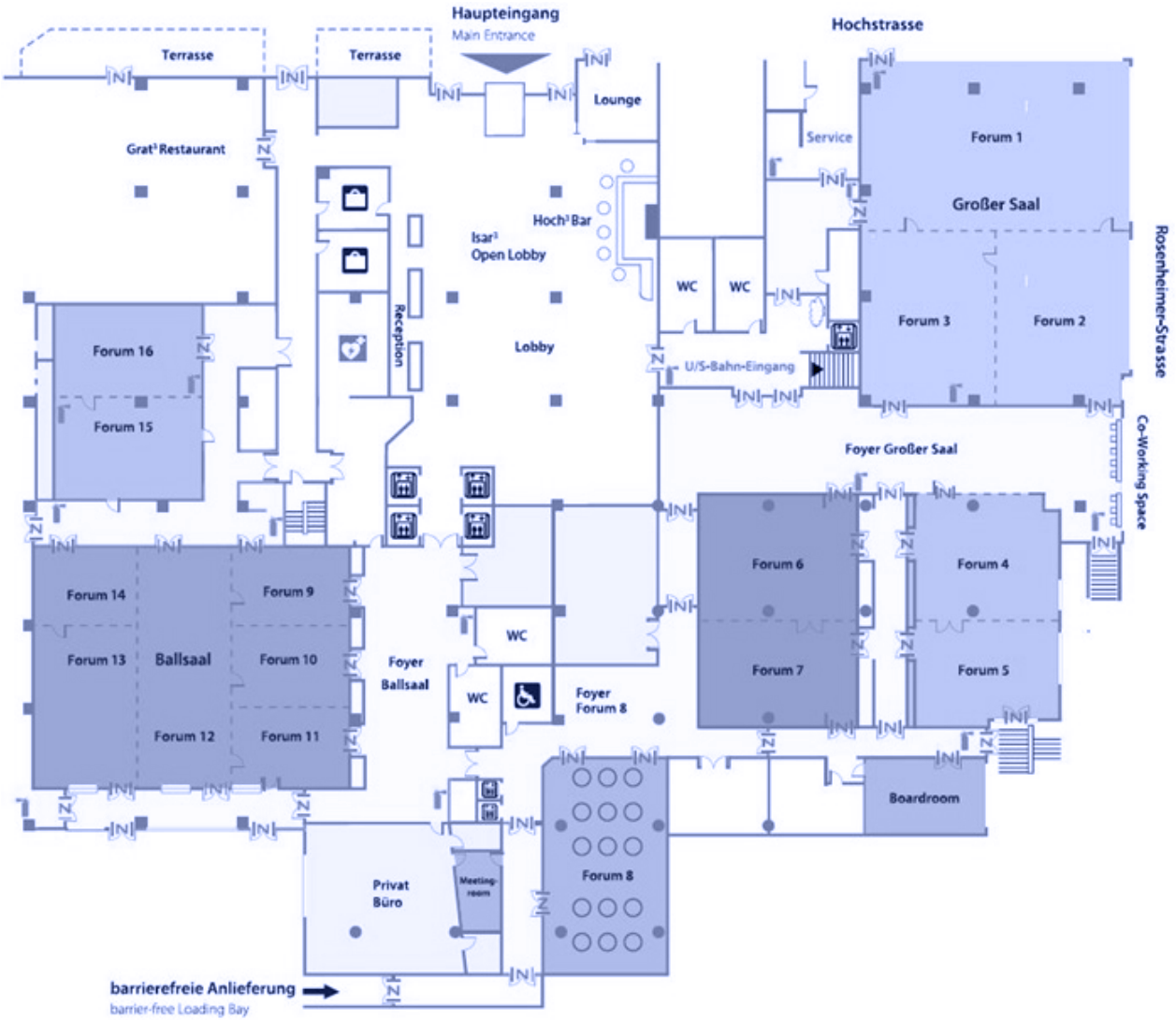
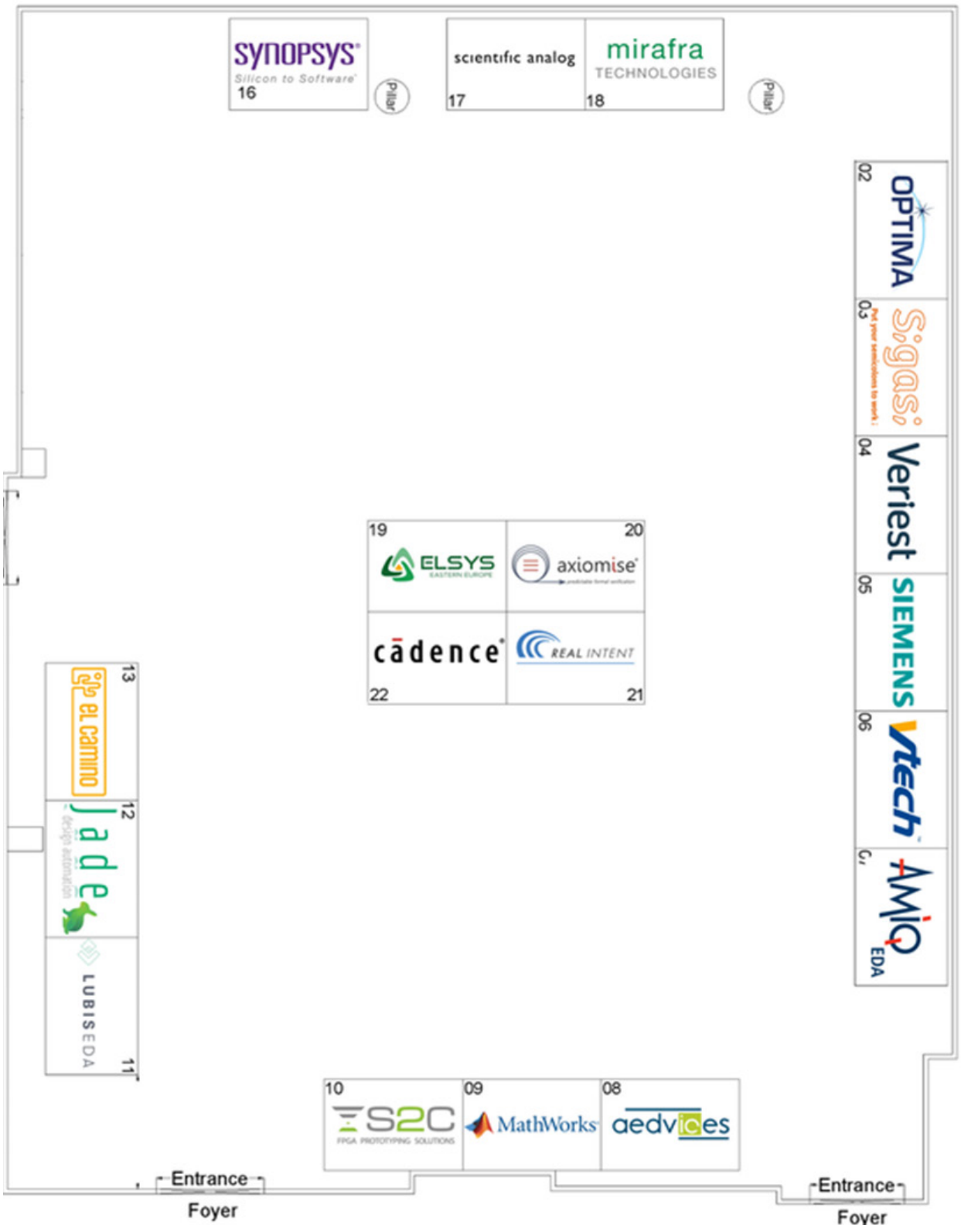
DVCon Europe 2024 Venue - Holiday Inn Munich City Centre

Hochstraße 3, 81669 München, Germany

The hotel is directly above Rosenheimer Platz S-Bahn station for fast, frequent connections across the city. It's a 10-minute train ride to Munich Hauptbahnhof and 35 minutes to Munich Airport (MUC). Families love the science and tech exhibits at the vast Deutsches Museum, a short walk away, while shoppers delight at the stores lining pedestrianised Kaufingerstrasse in the Old Town. The hotel has 18 meeting rooms offering space for up to 550 guests, and its convenient location makes it an ideal venue for events.



DVCon Europe 2024 Exhibit Hall - Großer Saal



DVCon Europe SystemC Modeling Challenge

DVCon Europe 2024 offers for the first time a SystemC Modeling Challenge -- with a have a vast set of great prizes and also traveling grants (kindly sponsored by Huawei).

How accurate can you estimate power/energy consumption of embedded HW/SW systems?

Bring your power estimation methods to DVCon Europe community!

Find more information please register on **https://dvconchallenge.de** – we will provide you

- a SystemC template: fill in your method for power estimation
- a measured power consumption data set: use it to create your power estimation method – calibration, machine learning, whatever, be creative!
- a test bench: it will be used to expose your power estimation method to an unknown scenario for evaluation.

Students and participants from developing countries can apply for travel grants.

Learn More: **https://dvconchallenge.de/**

Tutorial Program: Tuesday, October 15th

Opening Session
8:00 AM - 8:15 AM
Ballsaal

Keynote Speaker: Thomas Boehm (Infineon Technologies)
8:15 AM - 9:15 AM
Ballsaal

Dependable microcontroller architectures – challenges and opportunities in a fast changing automotive market

The automotive industry is undergoing a profound transformation driven by advances in semiconductor and microcontroller technologies, which are crucial for next generation vehicle architectures.

The presentation explores success factors for modern controller designs, major market trends and challenges for the industry. Key issues include increasing complexity and integration of electronic control systems, stringent requirements for dependability, upcoming AI technologies and scalability to meet the cost targets of affordable cars.

In this presentation we will analyse innovation drivers for modern multi-core microcontrollers in the last decade. On this basis we will showcase how the AURIX™ controller architecture addresses the main challenges of the industry and offers solutions for megatrends such as vehicle electrification and E/E architecture change. The presentation will also offer insights into the relevance of open source technologies for future hardware and software designs.

Attendee Coffee Break
9:15 AM – 9:45 AM
Großer Saal

Exhibit Hall Open
9:15 AM – 7:30 PM
Großer Saal

T1.1: G-QED for Pre-Silicon Verification
9:45 AM – 11:15 AM
Forum 4
Speakers:
Saranyu Chattopadhyay, Robust Systems Group at Stanford;
Mohammad R. Fadiheh, Stanford Robust Systems Group;
Keerthi Devarajegowda, Siemens EDA

With the increasing integration of diverse hardware accelerator and processor IP cores into digital systems, pre-silicon verification becomes increasingly complex. Our approach, Generalized Quick Error Detection (G-QED) [3], addresses these challenges by offering a robust verification framework that enhances productivity. G-QED, utilizing Bounded Model Checking (BMC) [4] techniques, introduces a novel method for any design with a notion of actions (for example, instructions in a processor core) and architectural states (for example, register files of a processor core).

An industrial case study on production-ready AI hardware accelerators demonstrated the following outcomes:

Significantly improved bug coverage of G-QED by uniquely detecting critical bugs that escaped industrial (simulation- and formal verification-based) verification flow (in addition to detecting all bugs detected by the industrial flow).

Dramatically improved verification productivity of G-QED, from 52 person-weeks using industrial flow to only 3 person-weeks using G-QED -- an 18-fold boost.

Tutorial Program: Tuesday, October 15th (cont.)

T1.1: G-QED for Pre-Silicon Verification (cont.)

G-QED enabled short design-design verification loops with quick turnaround for rapidly evolving designs. This tutorial will equip design and verification engineers with the skills to implement G-QED for efficient pre-silicon verification of hardware designs. Participants will learn through practical demonstrations how to utilize G-QED in a commercial formal verification tool without needing extensive knowledge of formal methods. The session will cover:

Understanding and interpreting actions, architectural states, and idling in the hardware design-under-verification (DUV).

Building and utilizing the G-QED harness for interaction with DUV and performing essential checks.

Implementing the G-QED setup in Siemens OneSpin for robust verification.

Debugging techniques specific to G-QED and the DUV.

T2.1: Breakthrough in CDC-RDC Verification Defining a Standard for Interoperable Abstract Model

9:45 AM – 11:15 AM

Forum 5

Speakers:

Joachim Voges, Infineon Technologies AG

Jean-christophe Brignone, STMicroelectronics, Grenoble

CDC analysis has evolved as an inevitable stage in RTL quality signoff in the last two decades. Over this period, the designs have grown exponentially to SOC's having 2 trillion+ transistors and chiplet's having 7+ SOC's. Today CDC verification has become a multifaceted effort across the chips designed for clients, servers, mobile, automotives, memory, AI/ML, FPGA etc. with focus on cleaning up of thousands of clocks and constraints, integrating the SVA's for constraints in validation environment to check for correctness, looking for power domain and DFT logic induced crossings, finally signing off with netlist CDC to unearth any glitches and missing crossings during synthesis. As the design sizes increased in every generation the EDA tools could not handle running flat and the only way of handling design complexity was through hierarchical CDC analysis consuming abstracts. Also, hierarchical analysis helps to enable the analysis in parallel with teams across the globe. Even with all these significant progress in capabilities of EDA tools the major bottleneck in CDC analysis of complex SOC's and Chiplets is consuming abstracts generated by different vendor tools. Different vendor tool abstracts are seen because of multiple IP vendors , even in house teams might deliver abstracts generated with different vendors tools. The Accellera CDC Working- Group aims to define a standard CDC IPXact model to be portable and reusable regardless of the involved verification tool.

As moving from monolithic designs to IP/SOC with IPs sourced from a small/select providers to sourcing IPs globally (to create differentiated products), the quality must be maintained as driving faster time-to-market. In areas where the standards (SystemVerilog, OVM/UVM, LP/UPF) are present, the integration is able to meet the above (quality, speed). However, in areas where standards (in this case, CDC) are not available, most options trade-off either quality, or time-to-market, or both. Creating a standard for inter-operable collateral addresses this gap.

This tutorial aims to remind the definitions of CDC-RDC Basic Concepts and constraints, as well as the description of the reference verification flow, and addressing the goals and scope of the Accellera CDC Working Group in order to elaborate a specification of the standard abstract model.

T3.1: Unleash the Full Potential of Your Waveforms: From Extra-functional Analysis to Functional Debug via Programs on Waveforms

9:45 AM – 11:15 AM

Forum 6

Speakers:

Daniel Große, Johannes Kepler University Linz
Lucas Klemmer, Johannes Kepler University Linz

In the design phase, HDL simulation is the heart for functional and extra-functional verification. The HDL simulator produces a waveform for a simulation run. In case of a deviation from the expected behavior, the waveform has to be analyzed and understood. For this task, waveform viewers are utilized. However, they only allow for viewing signal relations visually which is a highly manual and tedious process. While advanced verification techniques have introduced automation and led to the generation of "better" waveforms (e.g. by employing formal methods, reducing the length of waveforms, or minimizing the signals involved in a failing trace), there has been almost no progress for automating the analysis of waveforms.

In this tutorial we bring automation to the analysis of waveforms and provide hands-on experience on the open-source Waveform Analysis Language (WAL); WAL allows to code your analysis tasks running on waveforms to answer questions like:

- What is the latency of my bus interfaces?
- What throughput is my bus achieving?
- When is the processor pipeline flushed or stalled during software execution?
- Which software basic blocks are executed on my processor?
- How can traditional waveform debugging be complemented with programmable waveform analysis?

WAL (**https://wal-lang.org** and **https://github.com/ics-jku/wal**) has been realized as a Domain Specific Language (DSL). In comparison to other programming languages, WAL programs have direct access to all signal values of a waveform. Accessing signals in WAL is similar to accessing variables with the difference that the value returned depends on the loaded waveform and the time at which the signal is accessed. The reference implementation of WAL is provided open-source in Python. In addition, WAL can be used as an Intermediate Representation (IR); this has been demonstrated by the implementation of WAWK. WAWK is making complex waveform analysis as easy as searching in text files. Moreover, recently a "SystemVerilog-Assertion-to-WAL compiler" has been developed, called WSVA, to check SVAs on simulation traces.

WAL has been used to analyze performance metrics of industrial RISC-V cores, estimate AXI performance in an industrial setting, analyze cache performance of configurable RISC-V cores, generate control flow graph for software running on a CPU, visualize pipeline instruction flows, and visualization of RISC-V programs on CPU diagrams in educational settings.

T4.1: A detailed tour of IEEE standard P3164

9:45 AM – 11:15 AM

Forum 7

Speakers:

Miltos Grammatikakis, Hellenic Mediterranean University
Joerg Bormann, Siemens EDA

The tutorial addresses security concerns asset identification for Security Annotation during intellectual property (IP) integration, providing a short tour of IEEE P3164 in a uniform way. The new IEEE P3164 white paper extends Accellera's Security Annotation for Electronic Design Integration (SA-EDI) standard by providing a methodology that identifies critical security-relevant hardware design elements (called assets) from the early stages of IP architecture development to implementation. The methodology helps identify vulnerabilities that relate to breaches of privacy and security properties in IP design elements. These breaches may relate to well-established security pillars, such as confidentiality, integrity, and availability, device authenticity, and non-repudiation, but also other desired properties, such as access control, anonymity, remote attestation, or unexpected behavior.

Break
11:15 AM – 11:30 AM

T1.2: "Calling All Engines" – Faster Coverage Closure with Simulation, Formal, and Emulation
11:30 AM – 1:00 PM
Forum 4
Speaker:
Yassine Eben Aimine, Siemens EDA

Logic simulation remains the dominant technology modern chip design flows rely on for functional verification. A combination of rising complexity and random stimulus testing made it necessary to measure verification coverage, and impose a coverage closure milestone in the design verification flow. But with silicon chips becoming entire systems, both hardware assisted verification and formal verification are playing a greater role in achieving verification levels adequate for safety critical and quality stringent high-volume applications.

Despite these technologies providing payloads and test vectors orders of magnitude higher than those of simulation, their contribution to coverage often plays a muted role in reaching closure. In this tutorial, we will present a coverage closure framework that encompasses simulation, emulation, and formal; focusing on the type of coverage these verification tools can compute or extract.

We will also look at coverage data formats and how much inter-operability it offers across the various streams of EDA tools, but also some of the shortcomings that need to be addressed to make inter-operability more accessible for all types of EDA verification. We will enumerate the various scenarios where it makes sense to combine different types of coverage; and offer guidelines for deploying coverage merging techniques across emulation, simulation and formal.

We will also highlight the challenges with simulation coverage tools when used to manage coverage, then underline the benefits of a data driven collaborative verification environment in streamlining coverage closure using existing coverage APIs and upcoming AI/ML algorithms.

T2.2: Modernizing the Hardware / Software Interface - Life beyond spreadsheets. How to bring your SoC register design into the 21st Century
11:30 AM – 1:00 PM
Forum 5
Speakers
Tim Schneider, Arteris
Insaf Meliane, Arteris

Advanced semiconductor designs have many components, including multi-core architectures, programmable peripherals, and purpose-built accelerators. These design elements require a pathway for embedded system software to communicate with them. This is the hardware/software interface (HSI) and it forms the foundation for the entire design project. There are many activities that need information about the HSI. These activities include device drivers and firmware, hardware design and verification, technical documentation, system diagnostics and application software. All of them need accurate, up-to-date HSI information in many different and specialized formats. A lack of unified, up-to-date information results in poor collaboration and an increased opportunity for design errors. This can lead to costly last-minute fixes or even design re-spins, impacting team productivity and compromising, the end quality of the SoC.

Arteris addresses these challenges with CSRCompiler. CSRCompiler provides new technology for a better HSI solution with a scalable infrastructure that promotes a rapid, highly iterative design environment to specify, document, implement, and verify address maps for complex SoCs and FPGAs.

During this tutorial, we will explain how CSRCompiler has the features and flexibility to speed development of the largest and most complex designs

T3.2: Developing Complex Systems using Model-Based Cybertronic Systems Engineering Methodology

11:30 AM – 1:00 PM
Forum 6
Speaker:
Petri Solanti, Siemens

Nowadays the systems are becoming more and more software (SW) defined. They contain a high number of dedicated hardware (HW) accelerators, heterogeneous processor architectures and huge amounts of software (SW) distributed to multiple electronic units in the network to provide the required functionality and configure the HW to reach the maximum efficiency. The problems of developing such multidisciplinary systems, so called cybertronics challenge, exceed the capabilities of today's development methodologies.

A new design methodology is needed to tackle the cybertronics challenge. It must be able to thread the requirements from the top-level to the final implementation, and to abstract the design to the level that all stakeholders can understand. It must be able to handle the domain specific implementation information too. Model-based methodologies are the most promising approaches, but none of the existing methodologies can handle the complexity alone. A Model-Based Cybertronics Systems Engineering (MBCSE) methodology borrows elements from multiple model-based system design methodologies. It provides a framework that can handle the system complexity, requirements threading, digitally assisted system decomposition, interfaces to domain specific implementation flows, and digitally threaded verification. This tutorial demonstrates the MBCSE methodology starting from system requirements going through multiple subsystem layers to System-on-Chip (SoC) design using a simple product example.

T4.2: USF-based FMEDA-driven Functional Safety Verification

11:30 AM – 1:00 PM
Forum 7
Speakers:
Francesco Lertora, Cadence Design Systems
Frederico Ferlini, Cadence Design Systems

As the degree of automation continues to increase, the intelligent SoC content in automobiles is growing faster than the general semiconductor market. As a result, the traditional automotive electronics suppliers are being rapidly joined in the market by many other established semiconductor companies and startups, as well as OEMs seeking differentiation through increased vertical integration. This ever-growing set of players all need to meet the functional safety requirements specified in standards such as ISO 26262. A process called Failure Modes, Effects, and Diagnostic Analysis (FMEDA) is critical to meeting these requirements. FMEDA so far has largely been the preserve of consultants using spreadsheet-based approaches. But now, automotive semiconductor design projects are looking for tools offering greater automation and consistency, as well as greater ownership and integration with the design and verification flow, of the FMEDA process. We believe the inherent ambiguity of functional safety standards will finally converge into a consolidated EDA standard to enable automation, results consistency, and information exchange between integrators into a product development lifecycle, analogous to industry standards for hardware description languages, timing, and power constraints.

In this workshop, Cadence will present the Midas™ Safety Platform, and how it uses the Unified Safety Formal (USF) – a formalized method for safety analysis and specification of safety mechanisms – to provide a holistic and automated approach to FMEDA at the architectural, design, and diagnostic coverage verification stages. We will demonstrate how USF provides the links between the FMEDA process and digital design and verification flows for both digital and analog/mixed signal, to provide a complete and consistent approach to meeting functional safety requirements.

Lunch
1:00 PM – 2:00 PM
Großer Saal

T1.3: cocotb 2.0: How to get the best out of the new major version of the Python-based testbench framework

2:00 PM – 3:30 PM

Forum 4

Speakers:

Philipp Wagner, IBM

Holger Horbach, IBM Research & Development GmbH

cocotb is the most popular Python-based verification approach. For a good reason: By writing verification code in Python, verification engineers have access to all the goodness that makes software development productive and enjoyable. It allows developers to focus on the verification task itself, and tap into a huge ecosystem of existing code where it makes sense.

With cocotb 2.0, the latest major version of the framework, writing testbenches got even easier. The programming interface got streamlined further, deprecated functionality was removed, and some long-standing quirks were ironed out.

In this tutorial, we'll show how to write testbenches the cocotb 2.0 way. We'll also show how to update existing cocotb testbenches benefit from all cocotb 2.0 has to offer.

This tutorial is suited for both people who would like to get an introduction to cocotb, as well as for users who already have embarked on the cocotb journey and are looking for a guided tour to future-proof their testbenches. Basic Python programming skills are helpful.

T2.3: QEMU and SystemC (QBox) tutorial

2:00 PM – 3:30 PM

Forum 5

Speakers:

Mark Burton, Qualcomm

Alex Benee, Linaro

I. QEMU DEEP DIVE

QEMU is a long established open source emulator and Virtual Machine Monitor. When run as an emulator it executes fully multi-threaded JITed code that can run on all the current major shipping ISA architectures. The front-ends for a number of the major guest architectures are actively developed allowing OS designers to test and debug their code long before available hardware starts shipping.

It comes with a number of useful tools intended to make software development easier. There is a fully featured debug interface targeting gdb along with a full view of all system registers. The TCG plugin system allows the JITed guest code to be instrumented allowing for deeper runtime analysis. Support for architecturally defined semi-hosting allows for quick early bring up of code before drivers have been written. This can even be combined with a light-weight user-mode which avoids the overhead of a full system emulation which is useful for test cases that don't involve hardware access.

This tutorial is aimed at those who would like to learn more about QEMU and it's capabilities. We will give an overview of the projects history, architecture and features with a focus on things that will hopefully be of interest to QEMU users in the Design and Verification space. There is a long history of projects that have been built on top of QEMU and we will look at the gaps they have tried to fill, why they never got merged and what developments are happening in the upstream to better support these use cases.

II. QEMU AND SYSTEMC, CHALLENEGES AND CURRENT QBOX SOUTIONS.

One of those libraries is QBox. This is an open source library intended to enable QEMU (including all the models and components) to be included in a 'standard' SystemC environment. This tutorial will focus on the technical challenges of memory management and time synchronization between QEMU and SystemC, how QBox currently deals with these issues and what is being done that will help within QEMU.

QBox can be considered as a staging ground for 3 separate bodies of code, code that is working around limitations in the way in which QEMU is currently 'usable' (that are slowly disappearing), Additions to the SystemC library which are being unstreamed to the SystemC Common Practices working group, and finally a (hopefully small) body of code that will bring these elements together to allow the simple construction of platforms.

T3.3: Scalable HW Performance Assessment
2:00 PM – 3:30 PM
Forum 6
Speaker:
Ingo Feldner, Robert Bosch GmbH
The assessment of HW components from different suppliers and evaluation of configurations options is a critical part in the successful creation of competitive products. A close integration of SW workloads combined with real execution data from the HW components is essential for taking informed decisions. However, this process is often tedious and limited to a few design options due to lengthy lead and bring-up times, different simulation and emulation environments, tool dependencies and lastly the required capacity on Tier-1 side.

Our tutorial puts focus on the SW infrastructure needed to efficiently integrate own and third-party models into large company setups. We will demonstrate the current state of APIs and DSLs used for running simulation setups and evaluations in early design phases. Using available SW methods to support the deployment of simulation solutions can significantly reduce the setup time of simulations and enable a continuous reproducible development process. Furthermore, we showcase and motivate the use of open description and exchange formats to increase the adoption of simulation and prototyping solutions.

T4.3: Novel Approach to Verification and Validation (V&V) for Multi-die Systems
2:00 PM – 3:30 PM
Forum 7
Speaker:
Tim Kogel, Synopsys
From the data center to the edge and deep within the web of smart everything, today's advanced multi-die systems are achieving previously unheard-of levels of performance. Instead of one-size-fits-all monolithic silicon, multi-die systems are comprised of an array of heterogeneous dies (or "chiplets"), optimized for each functional component. But while multi-die systems offer new levels of flexibility and achievement in system power and performance, they also introduce a high degree of design complexity.

The Universal Chiplet Interconnect Express (UCIe) standard was introduced in March of 2022, and UCIe 1.1 in July 2023, to help standardize die-to-die connectivity in multi-die systems. UCIe can streamline interoperability between dies on different process technologies from various suppliers. In just 1 years we have seen rapid evolution of the specification with UCIe 1.1 released in July 2023 and UCIe 2.0 expected soon.

Experts believe that verification and validation (V&V) complexity is a double exponential function of design complexity. It is evident that traditional V&V approaches aren't sufficient to fulfil this humongous need and new approaches are required to handle architecture, Simulation, Validation and testing of such heterogenous systems. This session, through following topics, will present changes to the traditional approach and new elements which may help fulfil the current and future needs of Systems –

- Multi-die System Overview
- Introduction and Evolution of UCIe
- Early architecture exploration for Multi-die Systems
- Kick starting with ready-to-use Design and Verification Collaterals
- Quick System Verification Simulations and convergence
- Software-first using Hardware Assisted Verification
- Modular approach to System bring-up.
- Welcoming your Partners into your Kitchen

Attendee Coffee Break
3:30 PM – 4:00 PM
Großer Saal

T1.4: A Holistic Approach to RISC-V Processor Verification
4:00 PM – 5:30 PM
Forum 4
Speaker:
Larry Lapides, Synopsys

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Processors using the open standard RISC-V instruction set architecture (ISA) are becoming increasingly common, with an estimated 30% of SoCs designed in 2023 containing at least one RISC-V core. Whether licensing RISC-V IP and adding custom instructions, using open-source RISC-V IP or building a RISC-V processor from scratch, verification of RISC-V processors is a task in the SoC project plan. With the variety of sources for the processor IP, the range of complexity and the span of use cases, a one-size-fits-all approach to RISC-V processor verification does not work.

This tutorial presents a holistic approach to RISC-V processor verification using various tools in the Synopsys portfolio. It will cover processor complexity from microcontrollers to application processors to arrays of processors for AI accelerators, different levels of integration from unit to individual processor to processing subsystem to SoC, and cover different scenarios depending on the source of the processor IP. Matching different technologies and methodologies to this multidimensional verification space is critical.

Figure 1 shows an overview of the technologies and products included in this holistic approach to processor verification. These can be separated at a high level into formal and dynamic verification technology groups, however, even within those groups there are multiple technologies, methodologies and use cases. For example, dynamic verification can include self-checking test, post-simulation trace-compare and lockstep continuous-compare methodologies, executed on RTL, hardware-assisted verification platforms or actual silicon.

The key metric for this holistic approach is functional coverage, driven by a comprehensive verification plan. Continuing the example above, the verification plan might utilize relatively simple post-simulation trace-compare for basic instruction verification. However, verification of asynchronous events such as interrupts, debug mode, privilege modes and more requires the lockstep continuous-compare flow (Figure 2), which utilizes the ImperasFPM RISC-V processor model, ImperasDV processor verification environment and ImperasFC functional coverage modules. The verification plan might drill down into specific units in the processor, for example using formal verification (VC Formal FPV plus RISC-V ISA AIP assertions) for the floating point unit or for micro-architectural features such as the pipeline (especially an Out-of-Order pipeline). It might also go to a higher level of integration, for example using PSS (VC PSS) for verification of high level caches in a multi-processor configuration.

The verification plan also needs to take into account processor complexity and the end use case. A simple microcontroller, e.g. RV32IMAC, that is going to have internally-developed software running on it (a limited use case) will need less verification than that same processor that will be exposed to end users running software that may exercise every feature of the core. Verifying custom instructions should be a task commensurate with the number and complexity of the custom instructions, however, there also needs to be some verification that adding the custom instructions did not add unexpected behaviors to the original processor.

Verification also takes a lot of cycles. One estimate is that verification of an application processor takes 1015 cycles, or 10,000 RTL simulators running in parallel for 1 year. Most teams do not have those resources and schedule available. One way to accelerate the verification task is by using hardware-assisted verification platforms. By running the RTL at millions of instructions per second, 1,000x faster than RTL simulators, a significant shift left in verification can be achieved.

This tutorial will elaborate different decisions that go into the verification plan for RISC-V processors, and review the different technologies and methodologies that are employed in a holistic approach to processor verification.

T2.4: Comprehensive Glitch Signoff – Learnings and experiences from industry use cases

4:00 PM – 5:30 PM

Forum 5

Speakers

Vikas Sachdeva, Real Intent

Vardan Vardanyan, Real Intent

Vikas Sachdeva serves as the Head of Business Development for the APAC region at Real Intent, where he leads business development and product strategy for the company's key static signoff products. A graduate of the Indian Institute of Technology Delhi, Vikas is an entrepreneur and technologist with a deep expertise in EDA and semiconductors. He is passionate about technology, product innovation, and nurturing the next generation of talent in VLSI. Additionally, he is a best-selling author on Amazon with his book, "Becoming Irreplaceable."

T3.4: Efficient AI: Mastering Shallow Neural Networks from Training to RTL Implementation

4:00 PM – 5:30 PM

Forum 6

Speaker

Tom Richter, MathWorks

In the dynamic arena of artificial intelligence, the distinction between deep and shallow neural networks is not just academic. As we navigate through the complexities of AI, understanding the nuanced differences between these two neural network architectures becomes crucial, especially when considering their unique implementation requirements. Shallow neural networks, often overshadowed by their deep counterparts' ability to handle intricate tasks, are perfectly suited for specific use cases such as regression neural networks. Shallow networks, with their streamlined layer structure, are not just easier to train but also significantly less demanding on computational resources, memory utilization, and more.

This tutorial will highlight the architectural and operational differences between deep and shallow neural networks, focusing on how the latter's efficiency and resourcefulness make them ideal candidates for direct implementation on ASICs or FPGAs without the need for a traditional processor structure or extensive memory. Furthermore, this approach ensures a very low-latency and low-power implementation.

Using an example of a battery management system to predict the state of charge, we will show all the necessary steps to:

- Train and validate a regression neural network in MATLAB.
- Import the regression model into a Simulink block diagram.
- Quantize the algorithm automatically using the Fixed-Point Tool.
- Optimize the Simulink model for an efficient hardware implementation.
- Generate VHDL, Verilog, or SystemVerilog code for the neural network.
- Verify the generated RTL code by interfacing HDL simulators with MATLAB/Simulink.
- Test the algorithm on a prototyping hardware.

The shown approach can also be adapted to more network types and use cases. It not only opens up new avenues for AI applications in resource-, latency-, and power-constrained environments but also showcases the versatility and potential of shallow networks in modern technology. Join us on this tutorial journey to learn what is possible in AI with minimalistic yet powerful solutions.

T4.4: Exploring the Next-Generation of Debugging with Verification Management and Integrated Development Environment
4:00 PM – 5:30 PM
Forum 7
Speakers
Ionut Cirjan, Synopsys
Noam Roth, Synopsys
Werner Kerscher, Synopsys

This tutorial presents an overview of the recently unveiled, cutting-edge advancements in the next-generation Synopsys Verdi® platform. Learn about the power of AI-driven debug and new root cause analysis engines designed to speed-up bug finding, while experiencing enhanced usability through a refreshed graphical user interface. In addition, this session will cover how you can access an integrated development environment (IDE) and a robust verification management system, integrated to boost productivity your verification workflows. Dive into state-of-the-art verification with us as we showcase these groundbreaking capabilities poised to redefine the landscape of verification and debug methodologies.

Reception
5:30 PM – 7:30 PM
Großer Saal

Program: Wednesday, October 16th

Opening Session
8:15 AM – 8:30 AM
Ballsaal

Keynote Speaker: Erik Norden (Stealth AI Startup CTO)
8:30 AM – 9:30 AM
Ballsaal
Next 10x in AI - System, Silicon, Algorithms, Data

This talk explores the critical elements driving the next 10x in AI acceleration, focusing on the interconnected pillars of System & Silicon, Algorithms, and Data. We delve into efficient codesign for accelerated computing, highlighting techniques like flash attention, quantization and compression, alongside silicon and system innovations. Moving beyond dense matrix workloads, the talk examines trends like retrieval-augmented Large Language Models (LLMs), multimodal systems and agents, while emphasizing the crucial role of data quality and training methods. This presentation offers a holistic view of the evolving AI landscape, providing engineers a roadmap for navigating and contributing to the future of AI acceleration and its applications.

Attendee Coffee Break
9:30 AM – 10:00 AM
Großer Saal

Exhibit Hall Open
9:30 AM – 5:45 PM
Großer Saal

Session 1A
10:00 AM – 11:00 AM
Forum 4
Automated Design Behaviour Extraction of SoC Interconnects Using Formal Property Verification
Jan Hahlbeck, Chandana Guddenahalli Palaksha and Görschwin Fey

Verification for Everyone
Noel McCarthy and Paul Wright

Session 1B
10:00 AM – 11:00 AM
Forum 5
Simulation States
Mark Burton, Mark Glasser, Karsten Einwich and Ramzi Karoui

CPAS : Cocotb Power Aware Simulation Framework
Ahmed Alsawi, Liam O'Reilly and Evin Hughes

Session 1C
10:00 AM – 11:00 AM
Forum 6
Synthesis Strategy for Standard Cell Library Validation
Hyeonyoung Shin, Sanggi Do and Jinho Lee

Who checks the checkers? Automatically finding bugs in C-to-RTL Formal Equivalence Checkers
Michalis Pardalos, Alastair F. Donaldson, Emiliano Morini, Laura Pozzi and John Wickerson

Session 1D
10:00 AM – 11:00 AM
Forum 7
Analogous Alignments: Digital "Formally" meets Analog
Hansa Mohanty and Deepak Gadde

Functional Coverage Sign-off assisted by Formal Connectivity
Asheque Mohammad Zaidi and Muhammad Ul Haque Khan

Session 1E
10:00 AM – 11:00 AM
Forum 8
Verifying Non-friendly Formal Verification Designs: Can We Start Earlier?
Bryan Olmos, Daniel Gerl, Aman Kumar and Djones Lettnin

A Novel Approach for HW/SW Co-Verification: Leveraging PSS to Orchestrate UVM and C Tests
Tom Fitzpatrick, Vishal Baskar, Wael Mahmoud and Mohamed Nafea

Break
11:00 AM – 11:15 AM

Session 2A
11:15 AM – 12:00 PM
Forum 4
An Innovative Approach to Verify the SoC Integration using the Formal Property Verification
David Vincenzoni and Marcello Dusini

Making code generation favourable
Tero Isännäinen

Session 2B
11:15 AM – 12:00 PM
Forum 5
Auto Generation is the key to rapid integration to UPF-like UPVM libraries for Unified Power Verification
Gopi Srinivas Deepala, Priyanka Gharat and Lakshay Miglani

Enhancing Automotive Security and Safety through CSEv2.0 Test Vector Validation with Synopsys MIPI CSI VIP
Venkata Naga Srideepti Pisipati and Andrew Elias

Efficient Workflow using Verilator for Processor Benchmarking in SystemC-based Automotive SoC Platforms
Johannes Sanwald, Andreas Mauderer, Mohammad Badawi, Javier Castillo, Jan-Hendrik Oetjens, Maryam Keeley, Tim Kogel and Andreas Wieferink

Session 2C
11:15 AM – 12:00 PM
Forum 6
Streamline PCIe 6.0 Switch Design with effective Verification strategies
Deep Mehta and Meghvendra Rathod

Single Source library for high-level modelling and hardware synthesis
Mikhail Moiseev and Nanda Kalavai

Heartbeat based early detection of hang issues
Vinaykumar Kori and Tejbal Prasad

Program: Wednesday, October 16th (cont.)

Session 2D
11:15 AM – 12:00 PM
Forum 7

Solving verification challenges for complex devices with a limited number of ports using Debugports
Shyam Sharma and Shravan Soppi

Functional Verification Using C Model: DPI-C VS Static Value Tables
Djordje Velickovic and Katarina Bozinovic

A new approach to integrated AI into analog/mixed-signal verification workflow
Long Hoang, Emanuel Popovici and George Duffy

Session 2E
11:15 AM – 12:00 PM
Forum 8

A lightweight Python framework for analogue circuit design, optimisation, verification and reuse
Wolfgang Scherr, Violeta Petrescu, Johannes Sturm, Dirk Hammerschmidt and Santiago Sondon

Safety Analysis of Automated Driving Platforms Using Digital Twin Simulation and Runtime Monitoring
Tasneem A. Awaad, Hanya A. Elged, Mohamed A. Abu-Bakr, Sama Y. Fathy, Sara H. Ahmed, Mohamed Abdelsalam and M. Watheq El-Kharashi

Lunch
12:00 PM – 1:00 PM
Großer Saal

Panel
1:00 PM – 2:00 PM
Ballsaal

Digital Transformation in Automotive – Expectations versus Reality

In many industries including Automotive, a digital transformation is happening at full speed right now. A digital transformation means that industries renew or replace traditional design and manufacturing approaches by introducing modern infrastructure to achieve a higher level of automation and intelligence with the aim of improving productivity and quality.

Things like creating a digital factory or building a "digital twin" of an electric vehicle are often mentioned as one of the ultimate goals in this digital transformation journey. Another aspect of the transformation is the application of artificial intelligence, AI, to enterprise workflows. However, are these realistic goals and does it really bring something to make everything "digital", "virtual", and "intelligent"? In other words, is the digital transformation really addressing a fundamental problem, and where are we in this journey?

The objective of this panel is to take an outside-in and inside-out view, to assess where the automotive industry stands today with respect to embracing new ways of working and introducing new technologies as proposed by these digital transformation and AI initiatives.

The panel discussion will be centered around the following topics and questions:

- Digital twins for vehicles: what does it include? Mechanics, compute, environment, software, …?
- What is the role of AI in automotive manufacturing?
- What is the role of AI in automotive end products?
- Is the automotive industry aligning digital transformation across the entire supply chain, from Tier2 to OEM and beyond, or are these initiatives only happening locally on a per-company level?
- What is the relation to systems-of-systems and/or software engineering in all this?
- What will be the impact on the design and verification community and industry practices? Can we expect more system modeling, simulation, formal, verification, unstructured data, and AI-based methods?

Moderator

- Andreas Riexinger, Bosch

Panelists

- Ralph Schleifer, CARIAD
- Manfred Thanner, NXP
- John Kourantis, ARM
- Erik Norden, Stealth AI Startup

Break
2:00 PM – 2:15 PM

Session 3A
2:15 PM – 3:45 PM
Forum 4

Hard Math – Easy UVM: Pragmatic solutions for verifying hardware algorithms using UVM
Mark Litterick, Aleksandar Ivankovic, Bojan Arsov and Aman Kumar

A Novel Approach in Proving Unreachable Paths in Hardware-dependent Software
Bryan Daniel Olmos Suquillo, Wolfgang Kunz and Djones Lettnin

Automating the Use of State-Space Representations in Mixed-Signal IC Design and Verification
Francesco Stilgenbauer, Matteo De Ferrari, Cristiano Meroni, Giuseppe Ridinò, Cristian Macario, Paolo Stefano Crovetti, Edoardo Bonizzoni and Piero Malcovati

Session 3B
2:15 PM – 3:45 PM
Forum 5

Retention Sufficiency Validation for Optimizing State Retention Cells in Low Power Design
Nitesh Kalwani and Mateus Silva

A UVM Testbench for Checking the Global Convergence of Analog/Mixed-Signal Systems: An Adaptive Decision-Feedback Equalizer Example
Jaeha Kim

Enabling True System-Level, Mixed-Signal Emulation
Paul Wright, Nimay Shah, Pranav Dhayagude, Raj Mitra and Adam Sherer

Session 3C
2:15 PM – 3:45 PM
Forum 6

uvm_objection – challenges of synchronizing embedded code running on cores and using UVM
Joachim Geishauser, Yassmina Eliouj, Vasundhara Gontia, Sefa Veske, Shripad Nagarkar and Tobias Thiel

OpenCar: A SysML v2 Modeling Framework for Early Analysis of BoardNet Architectures
Sebastian Post, Johannes Koch, Aida Bevrnja and Christoph Grimm

Session 3D
2:15 PM – 3:45 PM
Forum 7

Automatic Insertion of a Safety Mechanism for Registers in RTL-Modules
Holger Busch and Jonathan Ross

Harnessing Regenerative AI and Machine Learning for Efficient Fault Simulation
Himanshu Vishwakarma, Ranjitha M and Lakshya Miglani

Design and Verification of SEE-Tolerant ASICs at CERN: Methodologies and Challenges
Adithya Pulli, Matteo Lupi, Stefano Esposito, Simone Scarfi, Szymon Kulis and Xavier Llopart Cudie

Session 3E
2:15 PM – 3:45 PM
Forum 8

Enable Reuse of SystemVerilog Verification IPs in cocotb/pyuvm
Yilou Wang, Thorsten Dworzak and Johannes Grinschgl

Unleash the Power of Formal for Post Silicon Debugging
Jan Hahlbeck and Shreya Upadhyay

Virtual Prototyping Framework for Pixel Detector Electronics in High Energy Physics
Francesco Enrico Brambilla, Davide Ceresa, Jashandeep Dhaliwal, Stefano Esposito, Kostas Kloukinas and Jeffrey Prinzie

Attendee Coffee Break
3:45 PM – 4:15 PM
Großer Saal

Program: Wednesday, October 16th (cont.)

Session 4A
4:15 PM – 5:45 PM
Forum 4

Harnessing the Strength of Statistics and Visualization in Verification
Olivera Stojanovic and Uri Feigin

Securing SoC: A Scalable Hardware Security Verification Methodology
Muhammad Abdullah Al Faisal, Jaimini Nagar, Thorsten Dworzak, Sebastian Simon, Ulrich Heinkel and Djones Lettnin

Trustworthiness Evaluation of Deep Learning Accelerators Using UVM-based Verification with Error Injection
Randa Aboudeif, Tasneem A. Awaad, Mohamed Abdelsalam and Yehea Ismail

Session 4B
4:15 PM – 5:45 PM
Forum 5

Addressing Fixed-Point Format Issues in FPGA Prototyping with an Open-Source Framework
Vishal Chovatiya, Gabriel Rutsch and Wolfgang Ecker

Compiling AI Workloads for On-Device Inference on Heterogeneous Systems using MLIR
Jan Moritz Joseph, Maximilian Bartel and Rainer Leupers

Session 4C
4:15 PM – 5:45 PM
Forum 6

Scalable and mergeable functional coverage flow for highly configurable IP signoff and specific customer deliveries
Fryderyk Koziol and Sebastian Cieslak

Reliable and Real-Time Anomaly Detection for Safety-Relevant Systems
Hagen Heermann, Johannes Koch and Christoph Grimm

Enhanced VLSI Assertion Generation: Conforming to High-Level Specifications and Reducing LLM Hallucinations with RAG
Hafiz Abdul Quddus, Md Sanowar Hossain, Ziya Cevahir, Alexander Jesser and Md Nur Amin

Session 4D
4:15 PM – 5:45 PM
Forum 7

Deployment of containerized simulations in an API-driven distributed infrastructure
Tim Kraus, Axel Sauer and Ingo Feldner

libtcg -- Accurate lifting of executable code using QEMU
Anton Johansson and Alessandro Di Federico

A Roundtrip: From System Requirements to Circuit Variations and Back
Sören Kwasigroch, Nicolas Theobald, Johannes Koch and Christoph Grimm

Program: Wednesday, October 16th (cont.)

Session 4E
4:15 PM – 5:45 PM
Forum 8

Improved Performance of Constraints
Milos Pericic

UVM Portable Stimulus: Synchronized Multi-Stream Parallel-State Scenario in UVM
Ahmed Allam

Formal RTL Sign-off with Abstract Models
Lucas Deutschmann, Osama Ayoub, Rohith Batthineni, Michael Schwarz, Tobias Ludwig, Dominik Stoffel and Wolfgang Kunz

Closing Session & Best Paper Award
5:45 PM – 6:15 PM
Ballsaal

SYSTEMC EVOLUTION DAY 2024

The ninth SystemC Evolution Day is a full-day, technical workshop on the evolution of SystemC standards to advance the SystemC ecosystem. In several in-depth sessions, selected current and future standardization topics around SystemC will be discussed in order to accelerate their progress for inclusion in Accellera/IEEE standards.

SystemC Evolution Day is intended as a lean, user-centric, hands-on forum bringing together experts from the SystemC user community and the Accellera Working Groups to advance SystemC standards.

Learn More: **https://systemc.org/events/sced2024/**

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