Gatelevel Simulations
Continuing Value in Functional Simulations

Ashok Chandran — Project Manager

Roy Vincent — IC Design Engineer

accellera SYSTEMS INITIATIVE™

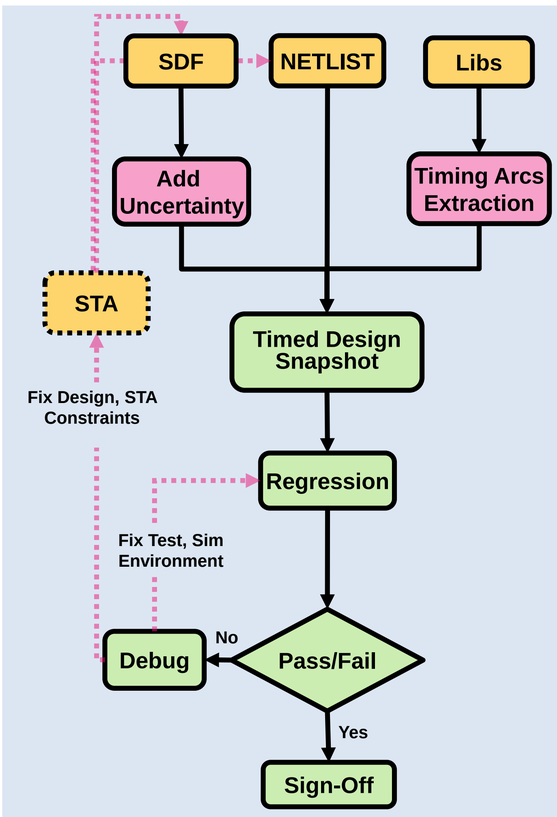
2014 DESIGN AND VERIFICATION DVCON CONFERENCE AND EXHIBITION INDIA

What is GLS?

- ❑ Netlists will be simulated with annotated delays
- ❑ Run the entire regression suite at different corners
- ❑ Analog macros verified by models with timing checks extracted from libs

Main Challenges

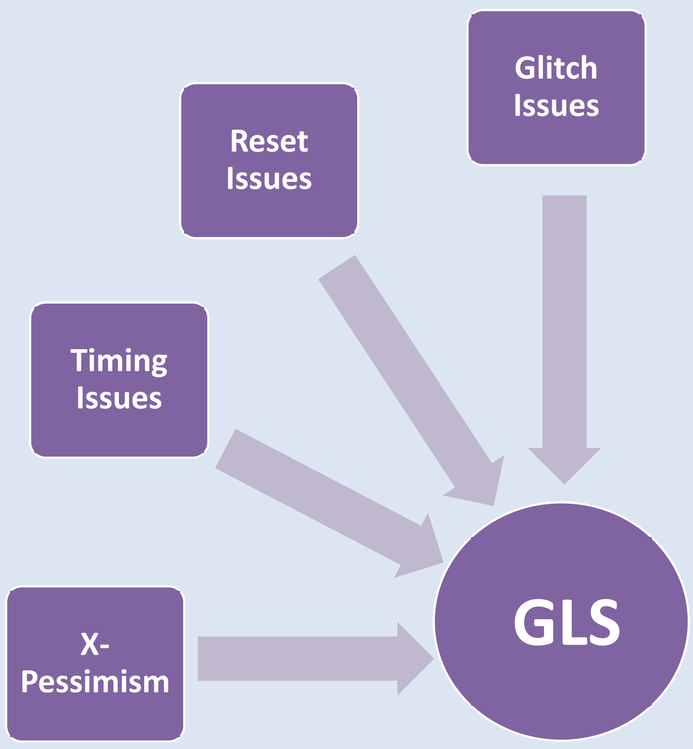
- ❑ Generating functionally qualified test suite
- ❑ Getting the setup issues resolved
- ❑ Compile, simulation speed; high memory requirement
- ❑ Significant time spent on failure debug



Why GLS?

- ❑ Integral Part of IC-Design Flow and critical for confidence.
- ❑ SoCs are becoming more timing complex (40nm and down)
- ❑ Performs quality check on Timing and Functionality.
- ❑ Covers timing checks not feasible by STA.
- ❑ Necessary for Scan simulations
- ❑ Verify the power up and reset operation of the design
- ❑ Verification of low power structures, absent in RTL and added during synthesis.
- ❑ Power estimation is done on netlist for the power numbers
- ❑ Check the critical timing paths of asynchronous designs that are skipped by STA

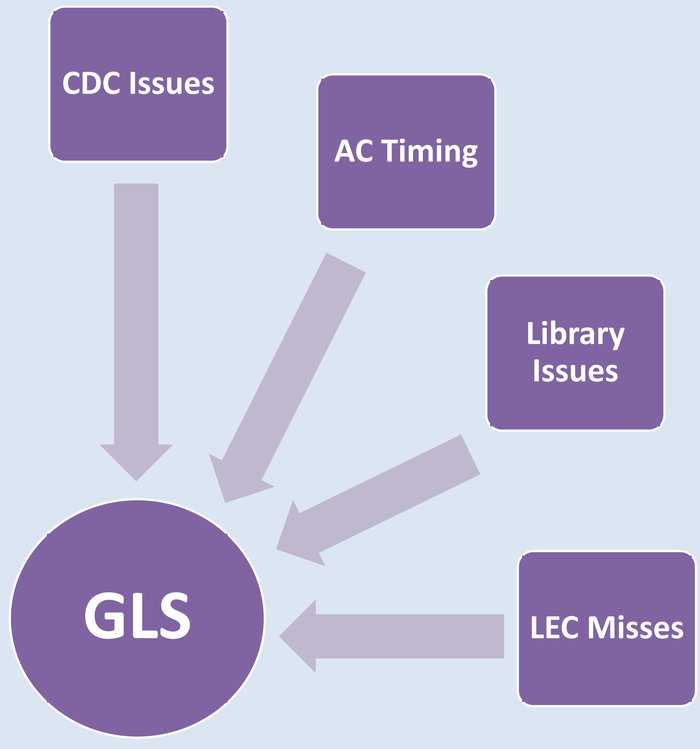
GLS Bugs Caught



- ❑ **X-Optimism in RTL**
  - RTL simulations are optimistic in handling X **values**
- ❑ **Timing Related**
  - Wrong multi-cycle and false path constraints
  - Implementation is not done for the rated frequency
- ❑ **Reset Paths**
  - Design has multiple reset domains
  - Glitch on generated resets
- ❑ **Glitch Issues**
  - Glitch from combo logic can cause issues

GLS Bugs Caught

- ❑ **CDC Issues**
  - Glitch on Synchronizer input can cause wrong sampling
  - Missing Synchronization in CDC paths
- ❑ **Lib Issues**
  - Libs sometimes miss some timing arcs
- ❑ **AC Timing**
  - AC Timing violation at chip ports
  - Invalid region is injected X and should not be sampled
- ❑ **LEC Misses**
  - RTL ifdef can cause trouble



Faster Bring Up

Tap Preserved Synthesis

Partition Compile Design & TB
↓
Get TB -> Design 'HREF' list
↓
Synth Netlist with 'Preserve HREF'
↓
PNR Netlist with 'Don't Touch HREF'
↓
Agent -> Design Taps preserved

Auto Inversion Detection

'HREF' list
↓
RTL-Netlist Equivalence Checking Tool
↓
Logic Inversion List
↓
Agent -> Design Tap Inversion Detected

Methodology Suggestions

- ❑ Avoid multi-cycle paths when possible
- ❑ No combo on generated resets - Check in Synthesis/STA
- ❑ Run Spyglass CDC
- ❑ Run X-prop simulations in RTL Phase
- ❑ GLS is as good as the functional coverage of tests
- ❑ Make good use of simulator options to improve speed
- ❑ 'Tap Preservation Flow' to avoid very high level netlist optimization
- ❑ Run Zero-Delay simulations for faster bring up

Contact
Ashok Chandran Ashok.Chandran@analog.com
Roy Vincent Roy.Vincent@analog.com

ANALOG DEVICES