



Wednesday, September 10, 2025							
Start	End	General Sessions - Grand Victoria					Exhibit Area Setup
9:00	9:30	DVCon India 2025 Inauguration					
9:30	10:15	Vision Talk: Software-defined hardware design relies on AI and intelligent verification Jean-Marie Brunet, VP & GM HW Assisted Verification Siemens					
10:15	11:00	Vision Talk: The SDC 'Root-of-Trust' Problem, And How We Solve It Dr. Sam Appleton, CEO Ausdia Inc					
11:00	11:30	Tea Break & Networking					EXHIBIT HOURS 11:00am to 7pm
Start	End	Track 1 - Grand Victoria B	Track 2 - Grand Victoria A	Track 3 - Robusta & Arabica	Track 4 - Brain Box	Track 5 - Shao	
11:30	12:15	Tutorial 1A:	Tutorial 2A:	Short Workshop 3A_1:	Short Workshop 4A_1:	Short Workshop 5A_1:	
12:15	13:00			Short Workshop 3A_2:	Short Workshop 4A_2:	Short Workshop 5A_2:	
13:00	14:00	Lunch Break					
14:00	14:30	Keynote: Power. Performance. Proofs: Scaling Formal for the AI-Driven Compute Revolution <Dr. Ashish Darbari, CEO Axiomise					
14:30	15:00	Industry Panel: Transforming the Silicon Landscape: The Impact of 3D-IC on Design, Verification & Validation Moderator: Ashok Kumar Natarajan, Google; Panelists: Avinash Seegehalli, Quest Global; Brijesh Chandraa, Prodigy Techno; Harinagarjun Chippagi, TCS; Biswajit Patra, Krutrim (MiraFra Partnership)					
15:00	15:45	Industry Talk: AI-Driven EDA: Evolving Trends and Technologies Dr. Alok Jain, VP - Verification Group Cadence					
15:45	16:00	Tea Break & Networking					
16:00	16:45	Tutorial 1B:	Tutorial 2B:	Short Workshop 3B_1:	Short Workshop 4B_1:	Short Workshop 5B_1:	
16:45	17:30			Short Workshop 3B_2:	Short Workshop 4B_2:	Short Workshop 5B_2:	
17:30	17:45	Day 1 Closing Remarks					
17:45	19:00	Networking					
19:00	19:15	DVCon India 2025 Awards Welcome					
19:15	20:00	Leadership Talk					
20:00	20:30	DVCon India 2025 Awards					
20:30	22:00	Dinner					

Thursday, September 11, 2025							
Start	End	General Sessions - Grand Victoria					EXHIBIT HOURS 9am to 5:30pm
9:00	9:15	Welcome & TPC Update					
9:15	9:45	Keynote: Re-engineering Engineering for AI Chip Design, Verification, and Optimization Vikas Gautam , VP-Engineering Synopsys					
9:45	10:15	Industry Talk: AI-Driven Design and Verification: Scaling Complexity with Intelligence Jayanth Thimmaiah, Sr. Director Sandisk					
10:15	11:00	Industry Panel: Silicon Strategy, Tariffs and the Chip Race: What It Means for India's Fabless and Foundry Future Moderator: Ruchir Dixit, Siemens Panelists: Huzefa Cutlerywala, Tessolve; Souvik Basu, Qualcomm; Anil Kempanna, Accenture; Ashok Chandran, Analog Devices					
11:00	11:30	Industry Talk: AI-powered Chip Design: Spec to Silicon P R Sivakumar, Founder & CEO Maven Silicon					
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11:45	13:15	Paper Session 1A:	Paper Session 2A:	Paper Session 3A:	Paper Session 4A:	Paper Session 5A:	
11:45	12:15	1A1:	2A1:	3A1:	4A1:	5A1:	
12:15	12:45	1A2:	2A2:	3A2:	4A2:	5A2:	
12:45	13:15	1A3:	2A3:	3A3:	4A3:	5A3:	
13:15	14:15	Lunch Break					
14:15	15:45	Paper Session 1B:	Paper Session 2B:	Paper Session 3B:	Paper Session 4B:	Paper Session 5B:	
14:15	14:45	1B1:	2B1:	3B1:	4B1:	5B1:	
14:45	15:15	1B2:	2B2:	3B2:	4B2:	5B2:	
15:15	15:45	1B3:	2B3:	3B3:	4B3:	5B3:	
15:45	16:00	Tea Break & Networking					
16:00	17:30	Paper Session 1C:	Paper Session 2C:	Paper Session 3C:	Paper Session 4C:	Paper Session 5C:	
16:00	16:30	1C1:	2C1:	3C1:	4C1:	5C1:	
16:30	17:00	1C2:	2C2:	3C2:	4C2:	5C2:	
17:00	17:30	1C3:	2C3:	3C3:	4C3:	5C3:	
17:30	18:00	Best Paper Awards & Closing					

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		Track Chair - Sundararajan A	Track Chair - Ray Ranjan Varghese	Track Chair - Somasunder K S	Track Chair - Narasimha Babu G V L	Track Chair - Lakshmanan B	
11:30	12:15	Tutorial 1A: Agentic AI in Action: Enhancing Debug, Diagnostics, and Decision-Making Anika Sunda , Sundararajan A, Amod Khandekar Cadence	Short Workshop 2A_1: Real-Time Handwriting Detection using an AI Model running on HAPS-200 Nilesh Shilankar & Kailas Senan Synopsys	Short Workshop 3A_1: Verify your next AI/ML design with Questa One Avery VIP Ankit Garg Siemens	Short Workshop 4A_1: CDC/RDC Interchange Format Standard Update Suman Chalana, Ashish Soni, Jebin Mohandas, Rahul Parashar Qualcomm, ST, Intel, Agnisisys	Short Workshop 5A_1: Power Dynamics: Shaping the future of the data centric era and the role of AI Sanjay Gupta & Vijay Chobisa Siemens	
12:15	13:00		Short Workshop 2A_2: Achieve software prototyping verification success with Veloce proFPGA CS Marshneil Koul Siemens	Short Workshop 3A_2: Addressing Protocol Verification Challenges in the Evolving Landscape of AI & HPC Diksha Sharma, Gaurav Chugh, Varun Agrawal Synopsys	Short Workshop 4A_2: Supercharge your RISC-V Designs with Higher Abstraction Shift-Left Ayush Mewati, Saswat Mund Circuitsutra	Short Workshop 5A_2: SystemVerilog Assertions - Bindfiles & Best Known Practices for Simple SVA Usage Cliff Cummings Sunburst-Design	
13:00	14:00	Lunch Break					
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16:00	16:45	Tutorial 1B: Boost Verification Efficiency with VC Execution Manager: Harnessing AI/ML for Superior Regression Management Taruna Reddy & Raghuram Srinivasarao Gururaja Synopsys	Tutorial 2B: Liberating Functional Verification from Boolean Shackles Vikas Sachdeva Real Intent	Short Workshop 3B_1: Addressing Formal Verification Challenges with GenAI technology & RISC-V solutions Raja Mahadevan & Ravindra Aneja Synopsys	Short Workshop 4B_1: PSS Accellera WG Update Akshay Bhosale AMD	Tutorial 5B: Introduction of IEEE 1801-2024 (UPF4.0) Improvements for the Specification and Verification of Low-Power Intent Lakshmanan Balasubramanian , Raguvaran Easwaran , Shubham Saha & Pottlapalli Santhosh,Manash Ranjan Raiguru, Jeevan Medaramitta TI, Intel, TI, Cadence,Synopsys, Siemens	
16:45	17:30			Short Workshop 3B_2: Unleashing the Potential of Agentic AI Within Design & Functional Verification Mark Carey & Nishtha Siemens	Short Workshop 4B_2: PSS in Action: Scalable Test Reuse from Design Verification to Silicon Klaus-Dieter Hilliges & Akshay Bhosale Advantest & AMD		
17:30	17:45	Day 1 Closing Remarks					
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11:45	13:15	Paper Session 1A: Design Verification - SV & UVM	Paper Session 2A: Static/Formal Verification	Paper Session 3A: Design & Architecture	Paper Session 4A: 3D Chiplet Verification	Paper Session 5A: AMS & Low Power
11:45	12:15	1A1: UVM based Generic Interrupt Service Routine (gISR) <i>Google</i>	2A1: Reducing Area and Leakage Power: Novel Formal Methodology for Retention Sufficiency in Low Power Designs <i>Qualcomm</i>	3A1: Efficient Booth Multiplier for FIR Filter Structure <i>SCET</i>	4A1: Breaking barriers in Advanced Multi-Chiplet AI SoCs using scalable Ucle and Boot Verification techniques <i>Samsung</i>	5A1: Optimizing CA-UDFM Models for Efficient Custom IP and Standard Cell Library Development <i>NXP</i>
12:15	12:45	1A2: Accelerating Debug with Experience-Driven Insights: A Tool-Based Approach for IP and SoC-Level Verification <i>Marvell</i>	2A2: Navigating Complexity to Convergence: Formal Verification for Single Precision FMA Units <i>Intel</i>	3A2: Adaptive Multi-Modal Sensor Fusion Accelerator with Real-Time On-Device Learning for Dynamic Environments <i>VIT Chennai</i>	4A2: Novel Approach For Verification Of Homogeneous Multi Die Booting Using Disruptive Distributed Simulation Methodology <i>Samsung</i>	5A2: Unified Digital Mixed-Signal UVM Checkers Framework: Enabling Reuse and Scalability Across Verification Projects <i>Analog Devices</i>
12:45	13:15	1A3: Pumping Up Test Development with Task Based, C-callable UVM based Tests <i>Siemens</i>	2A3: Solving Formal Complexity for Linked List Hardware Designs <i>Marvell</i>	3A3: Design and development of a Hybrid Out-of-Order RISC-V Processor Model <i>NXP</i>	4A3: Efficient Verification of Multi-Die Systems using Multi-Die Co-Simulation Framework <i>Renesas</i>	5A3: EEnet based Real-Number Modelling of an RF receiver <i>Analog Devices</i>
13:15	14:15	Lunch Break				
14:15	15:45	Paper Session 1B: Design Verification - SV & UVM	Paper Session 2B: Static/Formal Verification	Paper Session 3B: Design & Architecture	Paper Session 4B: Emulation & Prototyping	Paper Session 5B: Design Verification - AI & ML
14:15	14:45	1B1: A Summary and Examination of UVM Virtual Sequence Techniques <i>Paradigm-Works/Sunburst Design</i>	2B1: Halstead, McCabe, & Lint in Action: Quality Metrics for SystemVerilog Testbenches <i>Verifworks</i>	3B1: PCIe and AXI Domain Ordering - A Novel Approach using Arteris NoC and Synopsys PCIe controller <i>Meta</i>	4B1: Offline FSDB based Data-Integrity Debugger for Sub-System Emulation based Runs <i>Qualcomm</i>	5B1: Scaling Generative AI for Hardware Design Verification through Synthetic Data Augmentation & Adaptive Test Bench Validation <i>TCS</i>
14:45	15:15	1B2: Sequencer Coverage Exclusion Optimiser: Streamlining Coverage Closure in Dynamic Sequencer-Based Designs <i>Google</i>	2B2: Cherry-picking Assertions to Enhance Convergence <i>nVidia</i>	3B2: System design exploration with fully customizable NoC <i>Synopsys</i>	4B2: A Hybrid Functional Verification Approach of complex designs using Python based Models <i>Samsung</i>	5B2: RAG-Powered AI Agent for Verification: Accelerating CI, Regression Debug, and Document Intelligence <i>Renesas</i>
15:15	15:45	1B3: CVM - A Library for Unified C++ and SystemVerilog Testbench Development <i>Tenstorrent</i>	2B3: Breaking Barriers: Formal Verification in Complex Compressor Controller Architecture <i>Intel</i>	3B3: HBM in Custom Compute Systems: An Architectural Exploration for Future Computing Paradigms <i>Synopsys</i>	4B3: Accelerated Coverage Closure with Emulation: Covering Real-Time Use Case Corners <i>Qualcomm</i>	5B3: AI-Augmented and Automated Environment for Intelligent Verification <i>SmartSocs</i>
15:45	16:00	Tea Break & Networking				
16:00	17:30	Paper Session 1C: Design Verification - SV & UVM	Paper Session 2C: Static/Formal Verification	Paper Session 3C: RISC V/Processor	Paper Session 4C: Post Silicon	Paper Session 5C: Design Verification - AI & ML
16:00	16:30	1C1: Optimizing CPU-Based Configuration Path Verification Through Automated C Test Case Generation with UVM RAL <i>Google</i>	2C1: Novel Formal Equivalence approach to verify yield improvement in Complex Design <i>Qualcomm</i>	3C1: Decoding the RAS Maze: Microscopic Complexity Meets Verification <i>Tenstorrent</i>	4C1: Enhancing Anomaly Detection in Post-Silicon Validation Using Unsupervised Learning Techniques <i>NXP</i>	5C1: RAG for Formal Aware Property Generation <i>Synopsys</i>
16:30	17:00	1C2: Ensuring Deadlock-Free ASIC Operation: A Comprehensive Integration of Frequency & Operation Coverage Matrices <i>Micron</i>	2C2: Uncovering Hardware Vulnerabilities: Formal Verification for Security-Focused Negative Testing <i>Intel</i>	3C2: Implementing and Verifying RISC-V Nexus Trace Compliant Trace Encoder for High Performance Cores <i>Tenstorrent</i>	4C2: Strategic Optimization of Process Parametric Sampling: Leveraging Skew Sample Selection in Derivative Programs <i>Intel</i>	5C2: Coverage Prediction and Testcase Generation Framework using Machine Learning <i>Qualcomm</i>
17:00	17:30	1C3: Robust Verification of Clock Tree Network using "Clock Monitor" Integrated by ACRMG <i>Samsung</i>	2C3: Decoding the Unknown: A Synergy of Formal and Simulation Methods for Unclassified Faults <i>Analog Devices</i>	3C3: Catching the Unseen: A Case Study on Conquering Caching & Ordering Verification Challenges in Release Critical Unit <i>nVidia</i>	4C3: Accelerating DPMO Workflows Using Jenkins and AI: A Cross-Platform Validation Framework <i>Intel</i>	5C3: Scalable and cost-effective mixed signal modelling using AI with SV-RNM <i>Infineon</i>
17:30	18:00	Best Paper Awards & Closing				

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9am to 6pm

POSTER HOURS
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12:15	12:45	1A2: Accelerating Debug with Experience-Driven Insights: A Tool-Based Approach for IP and SoC-Level Verification Maitreyi Vemulapalli and Vinay Datta Marvell	2A2: Navigating Complexity to Convergence: Formal Verification for Single Precision FMA Units Swaresh Phadke and Madhurima Eranki Intel	3A2: Energy-Efficient Neuromorphic In-Memory Computing for Edge AIoT: A Crossbar-Based Architecture for Sustainable Intelligence Abhay Nayak, Sakshi Pai and Shubhan Kulkarni KLE Tech (Academic)	4A2: Novel Approach For Verification Of Homogeneous Multi Die Booting Using Disruptive Distributed Simulation Methodology Manikanta G, Chetan Kumar, Nitin Kumar M, Pradeep Kumar S & Sunil Kashide Samsung	5A2: Unified Digital Mixed-Signal UVM Checkers Framework: Enabling Reuse and Scalability Across Verification Projects Shruti Easwaran and Ameya Deshpande Analog Devices
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15:15	15:45	1B3: CVM - A Library for Unified C++ and SystemVerilog Testbench Development Varun Koyyalagunta, Jiahan Zhang, Mansoor Anees and Pravin Tavagad <i>Tenstorrent</i>	2B3: Breaking Barriers: Formal Verification in Complex Compressor Controller Architecture Namita Rawat, Usha Rani Bagadi, Rahul Dabur and Sarsij Saurabh <i>Intel</i>	3B3: High-Bandwidth Memory (HBM) in Custom Compute Systems: An Architectural Exploration for Future Computing Paradigms Puneet Kaushik, Vishal Kumar and Ratnala Naga Sai Madana <i>Synopsys</i>	4B3: Accelerated Coverage Closure with Emulation: Covering Real-Time Use Case Corners Vivek Tiwari and Bichu Sajeev <i>Qualcomm</i>	5B3: AI-Augmented and Automated Environment for Intelligent Verification Suguna Rasu, Sireesha Gedela, Harika Mali, Venkatasai Buthukuru and Issac B <i>SmartSocs</i>	
15:45	16:00	Tea Break & Networking					
16:00	17:30	Paper Session 1C: Design Verification - SV & UVM	Paper Session 2C: Static/Formal Verification	Paper Session 3C: RISC V/Processor	Paper Session 4C: Post Silicon	Paper Session 5C: Design Verification - AI & ML	
16:00	16:30	1C1: Optimizing CPU-Based Configuration Path Verification Through Automated C Test Case Generation with UVM RAL Ravi Mangal, Alisha Parvez & Apurva Shah <i>Google</i>	2C1: Novel Formal Equivalence approach to verify yield improvement in Complex Design Sanjana Jain and Ipshita Tripathi <i>Qualcomm</i>	3C1: Decoding the RAS Maze: Microscopic Complexity Meets Verification Shubham Mathur, Nimesh Kharat, Hadmath Singh and Darshan Hadadi <i>Tenstorrent</i>	4C1: Enhancing Anomaly Detection in Post-Silicon Validation Using Unsupervised Learning Techniques Santosh R and T Nandha Kumar <i>NXP</i>	5C1: RAG for Formal Aware Property Generation Pradip Prajapati and Anshul Jain <i>Synopsys</i>	
16:30	17:00	1C2: Ensuring Deadlock-Free ASIC Operation: A Comprehensive Integration of Frequency & Operation Coverage Matrices Sohel Langardar, Naman Kothari & Balwinder Sethi <i>Micron</i>	2C2: Uncovering Hardware Vulnerabilities: Formal Verification for Security-Focused Negative Testing Vedprakash Mishra and Ravi Mugidi <i>Intel</i>	3C2: Implementing and Verifying RISC-V Nexus Trace Compliant Trace Encoder for High Performance Cores Sajosh Janarthanam, Rahul Behl, Sharanesh R and Hitesh Pavan Oleti <i>Tenstorrent</i>	4C2: Strategic Optimization of Process Parametric Sampling: Leveraging Skew Sample Selection in Derivative Programs Pankaj Sharma <i>Intel</i>	5C2: Coverage Prediction and Testcase Generation Framework using Machine Learning Vardhana M, Suban Basha Shaik and Kota Subba Rao Sajja <i>Qualcomm</i>	
17:00	17:30	1C3: Robust Verification of Clock Tree Network using "Clock Monitor" Integrated by ACRMG Tejas Dipakkumar Dalal, Giridhar S, Jeevan Nataraju and Garima Srivastava <i>Samsung</i>	2C3: Decoding the Unknown: A Synergy of Formal and Simulation Methods for Unclassified Faults Siri Rajanedi and Prashantkumar Ravindra <i>Analog Devices</i>	3C3: Catching the Unseen: A Case Study on Conquering Caching & Ordering Verification Challenges in Release Critical Unit Ayush Saraogi, Gaurav B, Vivek Singh, Atharva Kakde & Ketki Gosavi <i>nVidia</i>	4C3: Accelerating DPMO Workflows Using Jenkins and AI: A Cross-Platform Validation Framework Aditi Bharmaik, Lakshminarayana Kammath, Shiju Philip Samuel and Kishan Kumar <i>Intel</i>	5C3: Scalable and cost-effective mixed signal modelling using AI with SV-RNM Sathyanarayana Ramamoorthy, Rutvikumar Patel, Anand Rahul, Kranthi Kiran and Hareesh Perumal <i>Infineon</i>	
17:30	18:00	Best Paper Awards & Closing					