Design and Verification Conference & Exhibition 2024

Speaker Presentation

23-08-2024

Agenda

- Introduction – Semiconductor Industry
- Evolving landscape of Semico design
- Challenges in modern chip design verification
- Innovations in chip design verification
- Need for new-age design verification strategies
- Quest Global efforts/support for Semico Industry

Success keys

Leadership Commitment

Strategic approach for Partnership

Local Global Presence

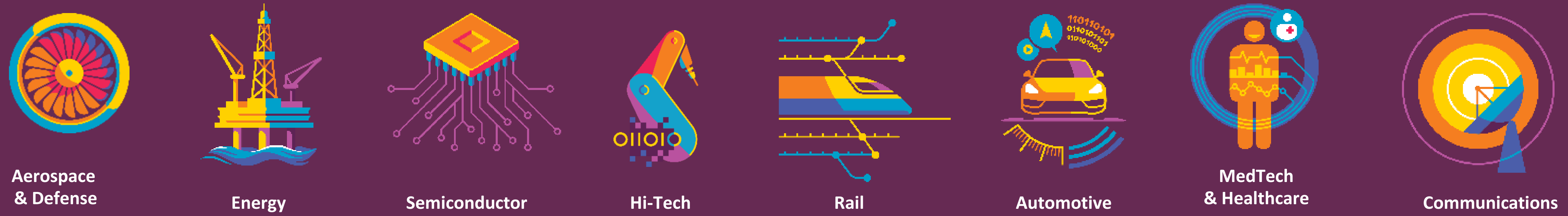
Technical Capability

Understanding products/tools

Readiness to start the engagement

Introduction

- New era driven by rapid technological advancements and ever-increasing market demands
- Chip Design - the critical design verification phase becoming more complex and vital
- Exploring the challenges and innovations in chip design verification
- Highlighting the industry's need for speed, higher throughput, and unwavering reliability
- Survival in an increasingly competitive landscape
- Global economy focus on design, manufacturing and sales of semico devices
- Understanding - the evolution, modern trends, challenges and latest strategies of semiconductor industry



Evolving landscape of semiconductor design

Rapid advancement in semiconductor technology has been fueled by the growing demands of:

Artificial intelligence (AI)

5G

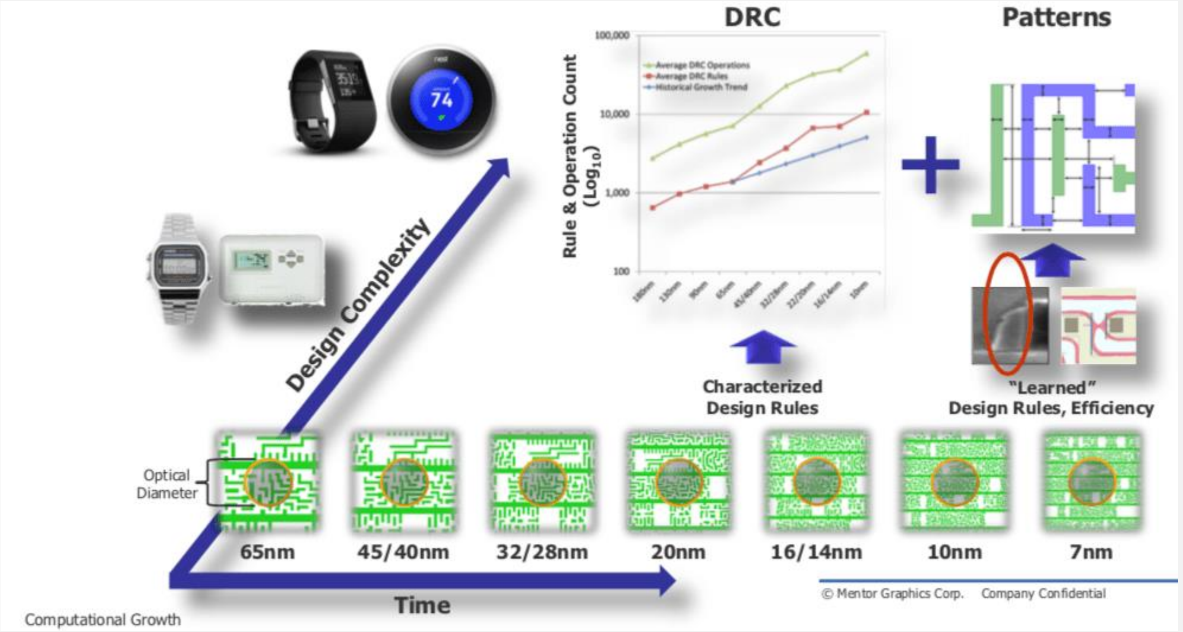
Internet of Things (IoT)

High Performance Computing (HPC)

Applications require chips that are more powerful, energy-efficient, and reliable

Evolving landscape of semiconductor design

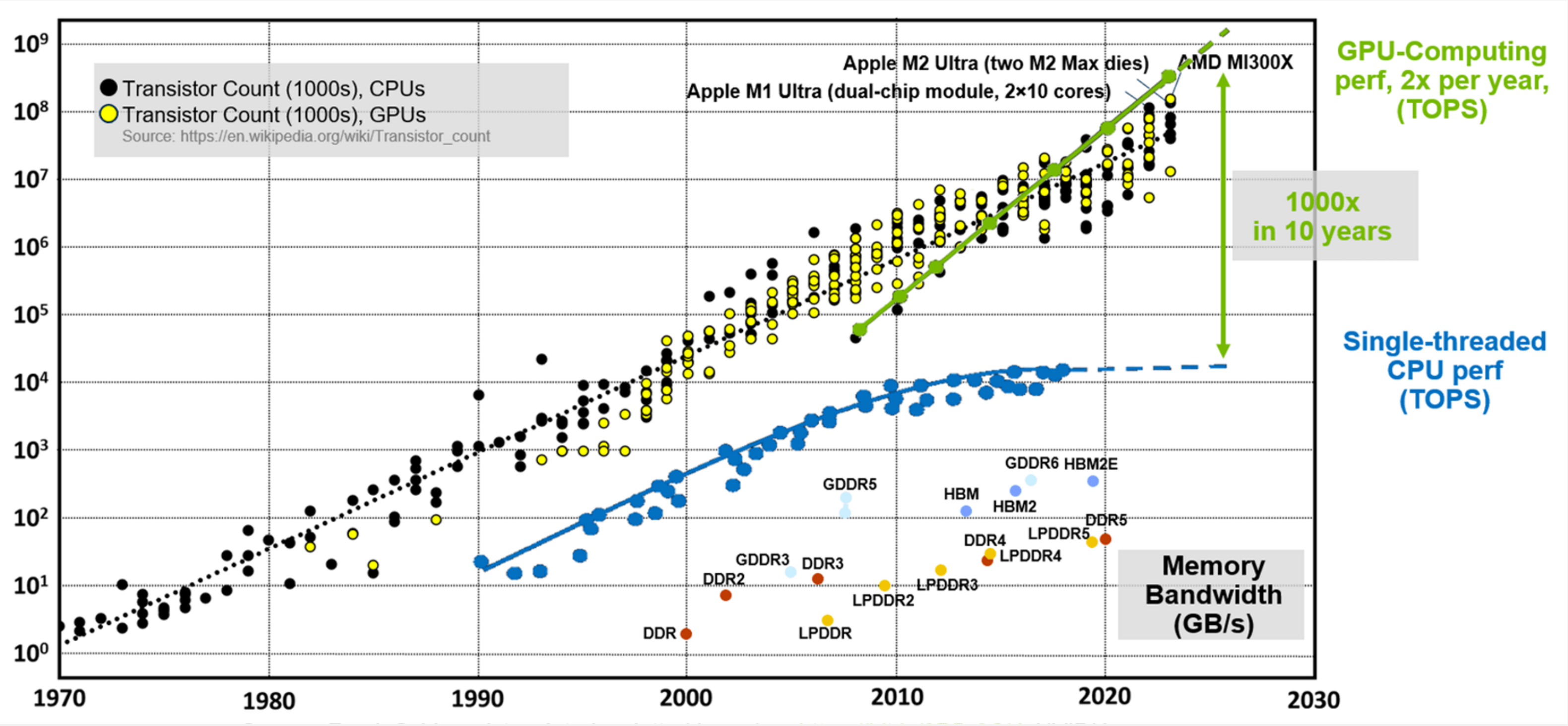
- Moving to lower geometry nodes and increasing design complexity
- Reduction in feature size allows for more logic gates to be packed into a smaller footprint
- Increasing the complexity of the design makes the verification process more intricate and time-consuming.
- The industry faces a critical challenge: how do we ensure the reliability and functionality of these complex designs while still meeting aggressive time-to-market goals?



Challenges in modern chip design verification

Increasing Design Complexity

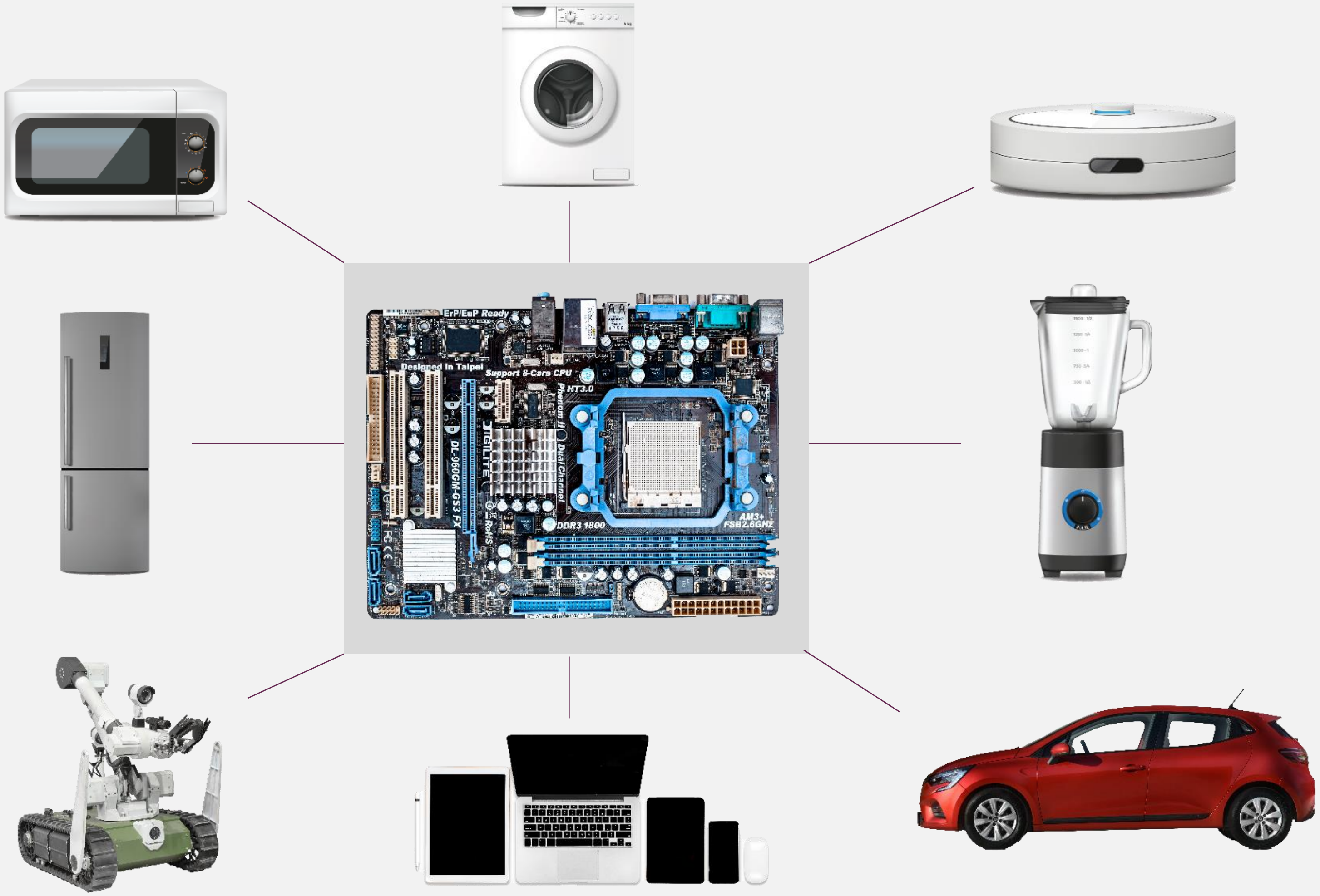
Increasing design complexity in modern chip design verification poses significant challenges



Challenges in modern chip design verification

Power Management

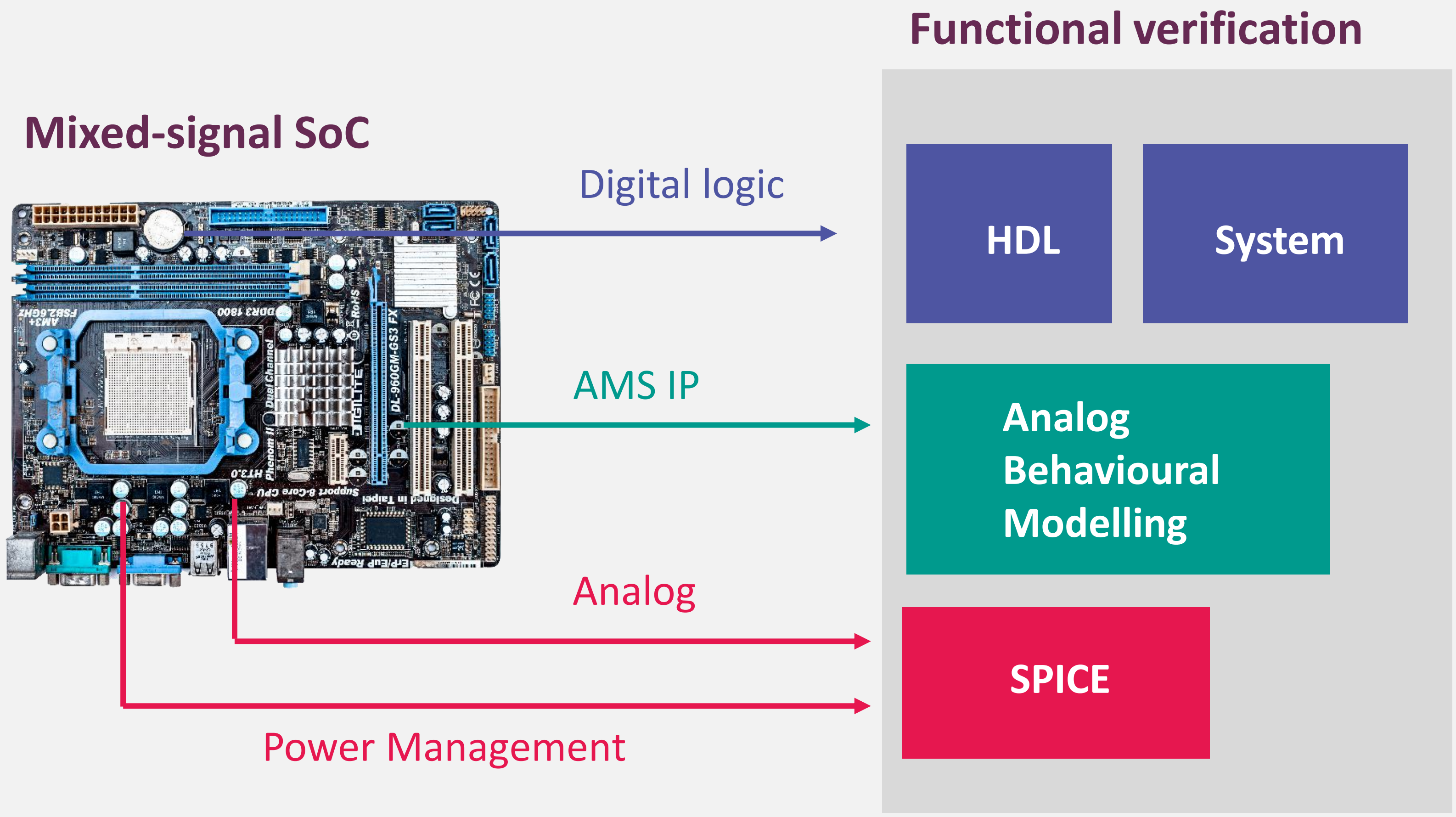
With the push for more energy-efficient devices, power management has become a critical aspect of chip design.



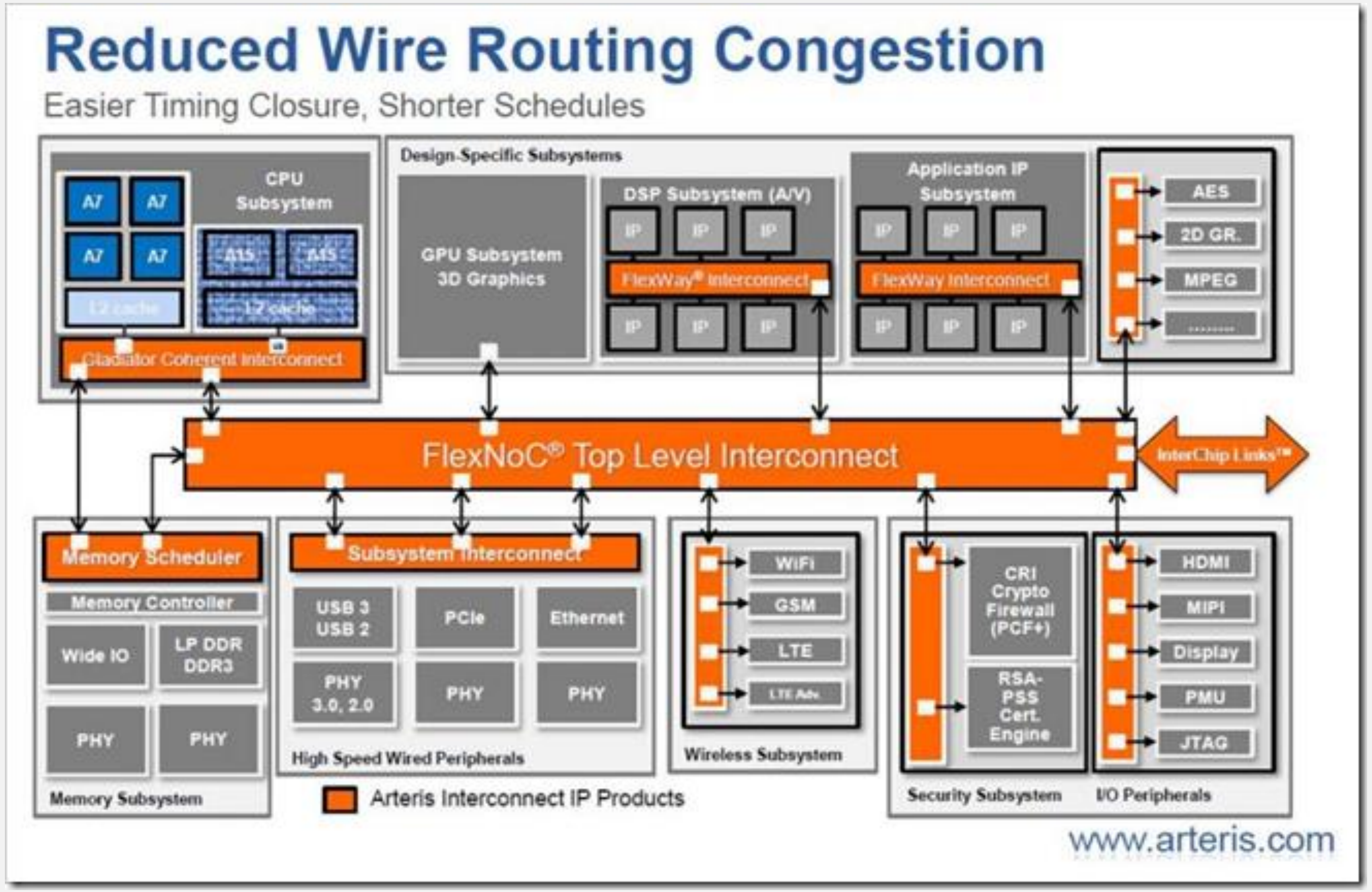
Challenges in modern chip design verification

Mixed-Signal Verification

Many modern chips incorporate both digital and analog components. Verifying them presents unique challenges and requires specialized tools and expertise



Challenges in modern chip design verification



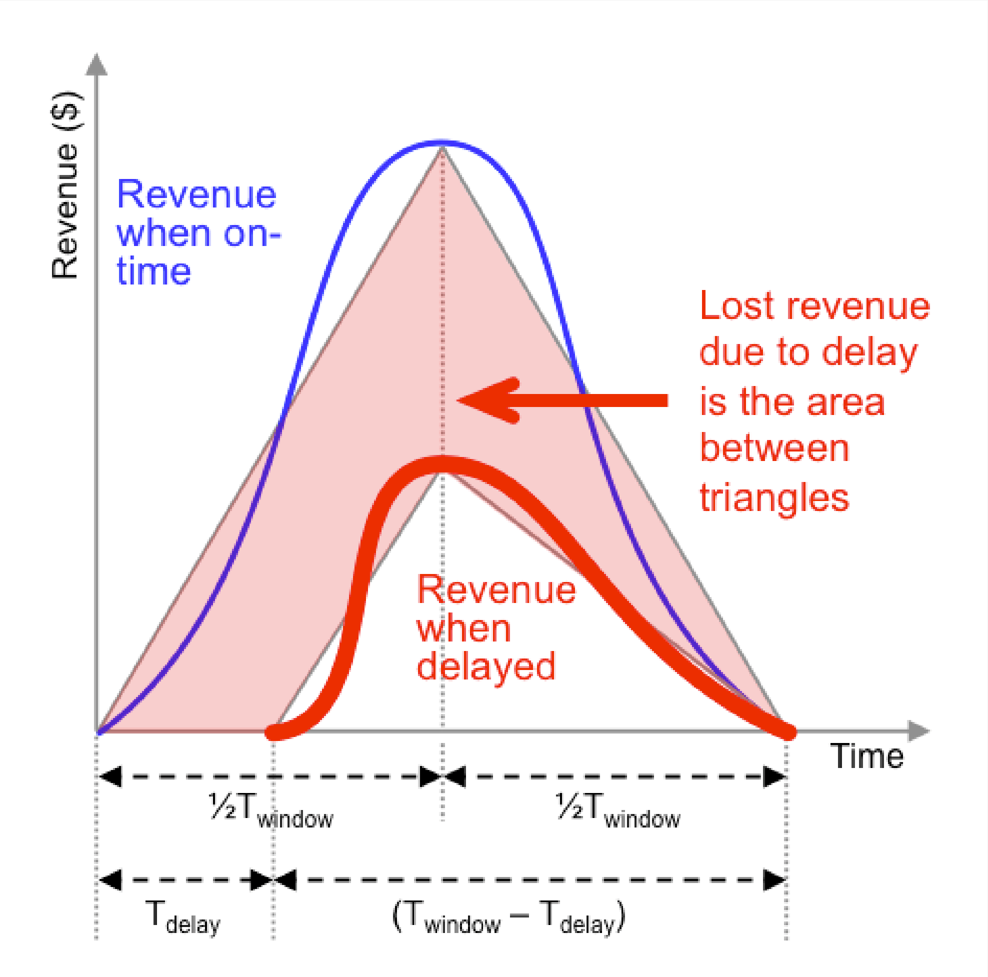
System-Level Verification

Chips more complex , incorporate multiple subsystems, verifying them becomes increasingly important and challenging.

Challenges in modern chip design verification

Time-to-Market Pressure

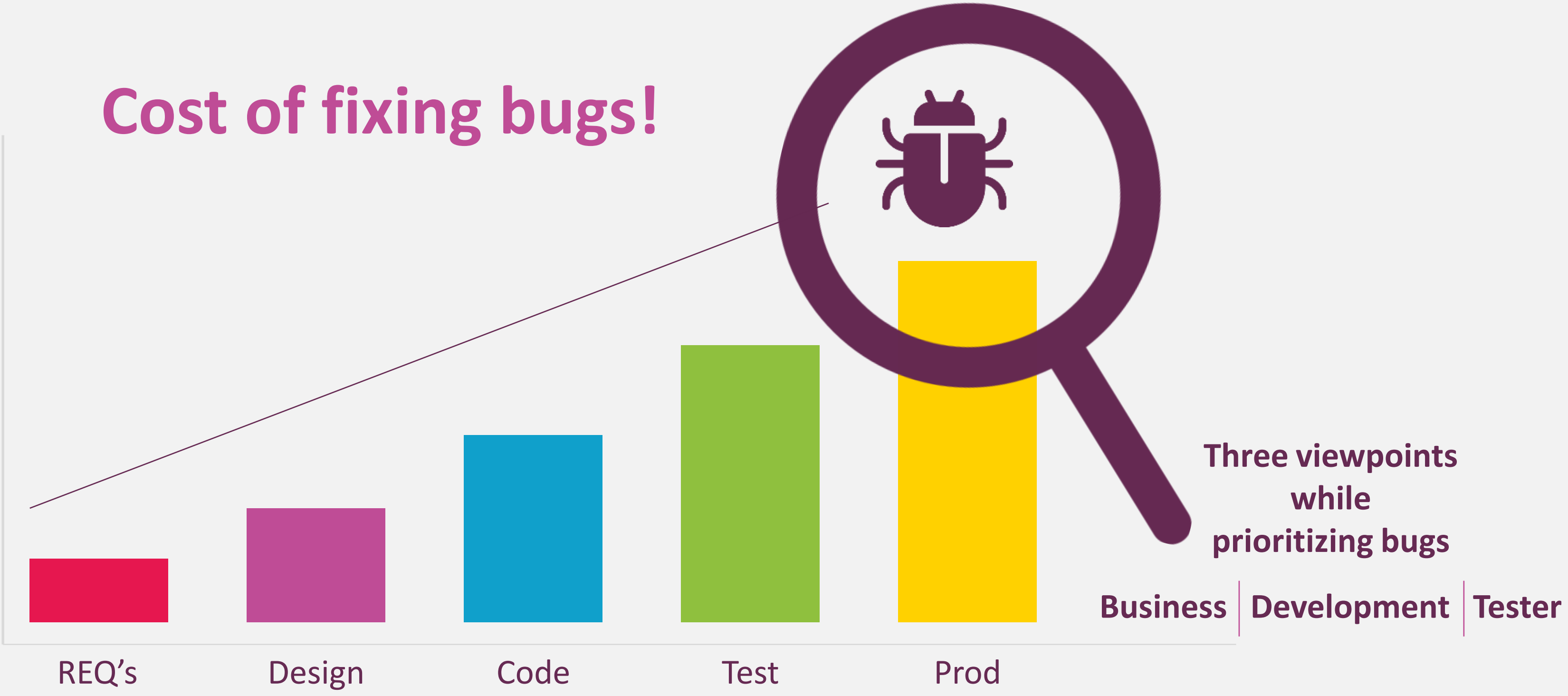
Competitive nature of the semiconductor industry demands faster product cycles. This puts immense pressure on verification teams to complete their work quickly without compromising on quality



Challenges in modern chip design verification

Achieving Low Bug Rate

As designs become more complex, ensuring a low BUG rate becomes more challenging, requiring more comprehensive verification strategies.



Innovations in chip design verification

Advanced Simulation Techniques

High-performance simulators - capable of handling large, complex designs are crucial.

Tools often leverage parallel processing and distributed computing to speed up simulation runs

Emulation and FPGA Prototyping

Hardware-assisted verification using emulators and FPGA prototypes for much faster verification of large designs.

Approach is particularly useful for system-level verification and software validation.

Formal Verification

Mathematical methods are increasingly being used to prove the correctness of certain aspects of chip designs.

Formal verification can provide exhaustive and identify corner cases that might be missed by traditional simulation.

Machine Learning and AI in Verification

AI and machine learning techniques are being applied to various aspects of the verification process, from test generation to coverage analysis.

Tools can help identify patterns and potential issues that human engineers might miss.

Innovations in chip design verification

Power-Aware Verification

Specialized tools and methodologies have been developed to verify power management features

Mixed-Signal Verification

- Advanced tools can handle both digital and analog domains
- Allow more comprehensive verification of mixed-signal designs

Verification Reuse and IP Integration

Methodologies for efficient integration and verification of components within larger systems are becoming crucial.

Need for new-age design verification strategies

DV strategies came a long way in past few years driven by improvement in technology and increased complexity in Chips. **Below are few main components of new age design verification strategy.** Combined these methods we can do a robust verification of complex chips, making sure bug free products

- AI & ML Learning
- Formal Verification
- Model Based Verification
- Simulation & Emulation
- Advance Debugging Tools
- Automated Testing
- Hardware & Software Co Verification

Quest Global – Specialized Engineering Partner

Quest global

Architecture and Specifications: We develop specifications and system-level designs, laying the foundation for robust chip architectures.

RTL Design and Integration: From micro-architecture specifications to RTL development and verification, we ensure seamless integration of all design elements.

Design Verification (DV): We offer comprehensive functional verification, low power design verification, and FPGA emulation services to ensure design integrity.

Design For Test (DFT): Our team provides test architecture, MBIST insertion, and ATPG pattern generation, enhancing the testability of your designs.

Physical Design (PD): We handle floor planning, placement, timing optimization, and power analysis, optimizing your chip's physical implementation.

Analog Design and Layout: We offer expertise in analog and mixed-signal design, including SerDes, PMU, and RF layouts, catering to diverse design requirements.

FPGA Prototyping and Emulation: We map client SoCs/ASICs to FPGA platforms for hardware and software validation, accelerating the verification process.

Post Silicon Validation: Our services include conducting validation, device characterization, and qualification, ensuring your chip meets all specifications

Thank you