Confidently Sign-off any Low-Power Designs without Consequences

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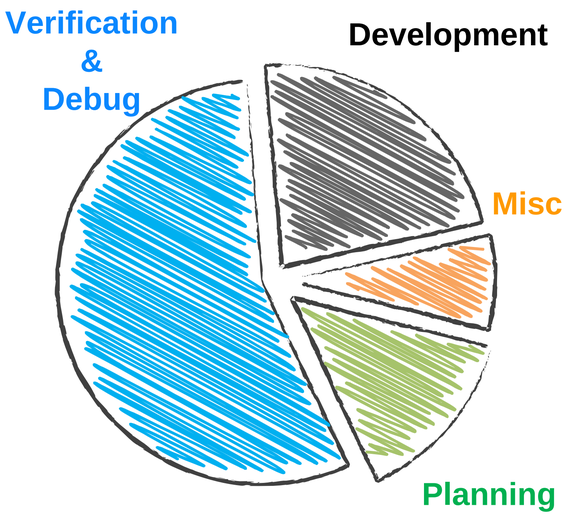
INTRODUCTION

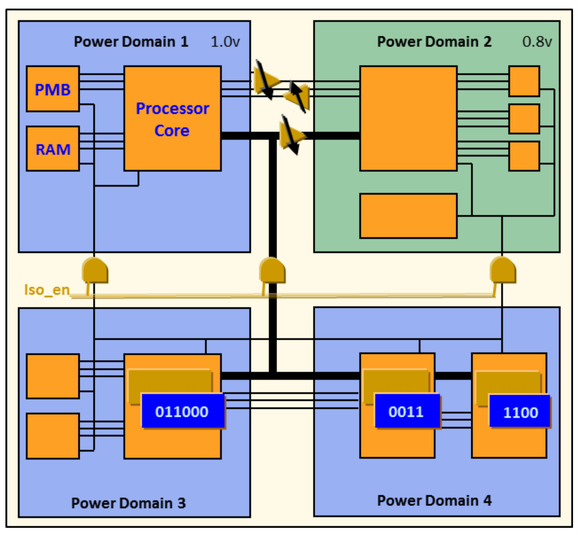
- Electronic devices have become complex and energy aware
- Require sophisticated power management architectures and strategies
- Need for advanced & efficient power aware verification



Time Spent

- Need to catch the low-power issues early in the design cycle, that is, at the RTL stage itself
- Save on verification & debug time

BASIC CONCEPTS OF UPF



- Power Domain
- Isolation
- Level Shifting
- Power States
- Driver / Receiver Supply

MOTIVATION FOR METHODOLOGY

Common Verification Questions

1. Is design free of all common low-power design issues?
2. Are enough test vectors specified?
3. Is design checked for design specific conditions ?

Address above questions

- Understand common low-power issues, root cause and debugging strategies
- Ensure enough test vectors are provided
- Not relying completely on tool generated assertions : use custom low-power assertions

LOW POWER DESIGN ISSUES & DEBUGGING STRATEGIES

Isolation Issues

1. **Isolated Port Value is different from Clamp Value**

Issue:

Logic reading the port sees a different value at isolation enable/disable since the new value is the clamp_value

Root Cause:

- **Either the port is isolated with a wrong strategy (unexpected clamp value) or**
- **Inputs are not consistent with the clamp value**

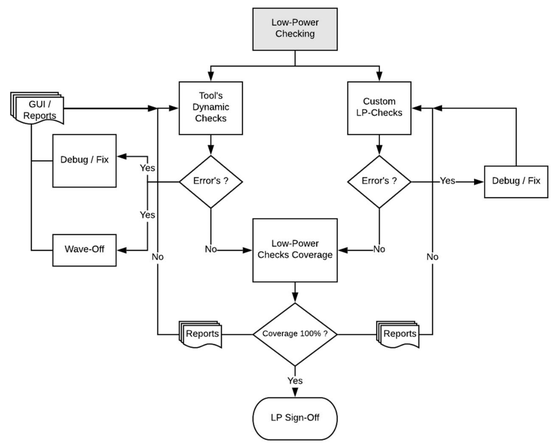
Debugging Strategy

- **Check waveforms : Isolated port, control, clamp value**
- **Check isolation supply : is cell switched off ?**
- **Is isolation control signal active when there is no requirement for isolation?**
- **Isolation control not enabled when power is switched OFF**

LOW POWER DESIGN ISSUES

- **Activity on Isolated Port at / during the isolation period**
- **Incorrect value on isolated port during Non-Isolation period**
- **Redundant Activity on isolation control signal**
- **Missing Level Shifters in the design**
- **Incorrect Level Shifter**
- **Retention protocol issues for Master Slave configuration**
- **Retention Issue : Value mismatch in saved and restored value**
- **Control ports Switch/Iso/Ret strategy got corrupted**
- **Isolation or retention supplies are switched off during the active isolation or retention period**

PROPOSED VERIFICATION METHODOLOGY



- With verification tools **dynamic checking** capability combined with **user's custom low-power assertions**, one is ensured that all the low-power checks are built into the design or simulation run.
- Another important thing to note is that enough test vectors will be required to capture issues or exercise all possible scenarios.
- The verification cycle continues till design is free from all low-power error's and checks coverage is 100%

CUSTOM LOW-POWER CHECKS

Get Handle of low-power objects using HDL package function (IMDB API)

```
upfHandleT pd = upf_get_handle_by_name("/tb/dut/pd")
```

Fetch dynamic property of low-power objects using UPF 3.0 continuous access HDL package function

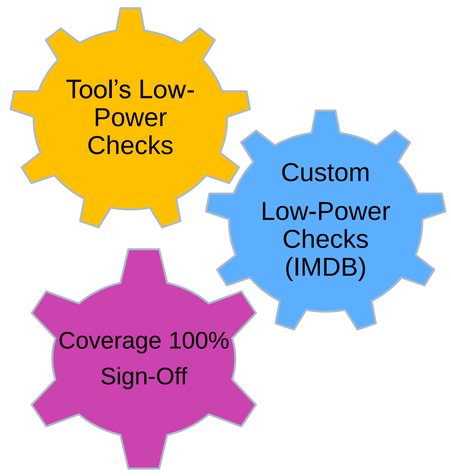
```
upf_create_object_mirror("/tb/dut/pd",
"pd_hdl");
```

Assertion Module : Pass the above handles to SV assertion module. Module can be instantiated in testbench.

```
module assertionPowerState (int
state_ON_CAMERA, int
state_ON_VIDEO)
reg cov_clk = 0;
…
always@(posedge cov_clk)
   assert (state_ON_CAMERA !=
state_ON_VIDEO) else $error("Camera
and Video both on at same time");
endmodule
```

CONCLUSION

Foremost understanding of common low-power issues, their root cause and debugging strategies is important!



Consistent, Robust, Scalable Low-Power Verification Methodology

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