Channel Modelling in Complex Serial IPs

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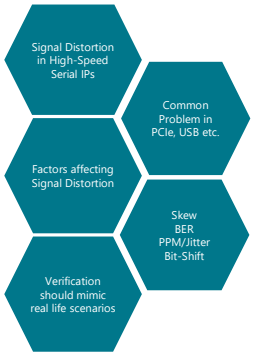
Problem Statement/Introduction

- In High-speed Serial Interface IPs (e.g.: PCIe, USB etc.,) there are numerous reasons for signal distortion due to practical environmental behavior or material behavior.
- The data received by a high-speed Serial IP have a large amount of signal distortion due to multiple factors like lane-to-lane skew, PPM variation in clocks, Jitter, Bit Error Rate (BER) in data and Bit shift caused due to CDR circuit.
- So, there is a real need to exercise the design with data consisting of all the signal distortion parameters.
- In this poster, we have demonstrated methodology for stimulus creation with real life scenarios to effectively verify a high-speed Serial Controller IP.



Proposed Methodology

Proposed solution enables signal distortion embedded within the TB for all scenarios

DUT is always stressed with data that is affected with Skew/Jitter/BER/ PPM/Bit-Shift

To create a robust IP, there is a need to create stimulus with real-life data that has Lane-to-Lane Skew, Clock PPM Variations, Lane Jitter, Bit-Error-Rate (BER) and Bit shift.

Across industry there are no push button mechanisms provided to enable real-life scenario modelling

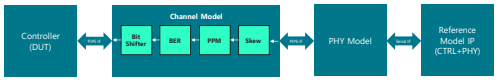
Proposed Method : A "Channel Model" that can Inject/Add Skew, Jitter, PPM, BER and Bit-Shift to the data received by DUT would be an ideal solution.

We have accomplished this Channel Model through a sequence of channel models which provides mechanism to create realistic modelling in the received data.

The Channel Model is in an always-on mode, across complete regression test suite, allowing us to run tests effectively such that the DUT (represented as "Controller" below) is always stressed

Implementation Details/Diagram

- The received data from link partner is manipulated by passing through the following modules in sequence



Ref Model
- The Data transmitted by Link Partner Device (BFM) is good data without any signal distortion.
- The raw good data from Link Partner Device (BFM) is passed through the below channel models in sequence.

Skew
- Adds Static and Dynamic Skew.
- The data received on each lane is delayed depending on the programmed skew value.

PPM
- The output data from skew model is passed to the PPM and Jitter model for PPM and Jitter addition.
- The PPM and Jitter is added to the received data by generating the recovered clock with variation in clock period.

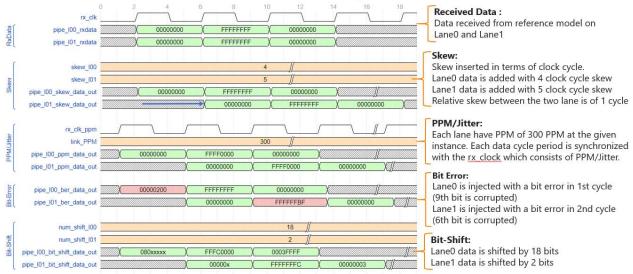
BER
- This model has a speed sensitive bit error injection mechanism which flips a bit at regular interval in controlled random manner.
- The model also predicts the expected error and downgrade them on the fly.

Bit Shifter
- This model essentially mimics the CDR circuit output data which has the bit shifted data.
- The data coming out of Bit-Shifter is fed into the DUT.

DUT
- The final data received by DUT has Skew, PPM, Jitter, Bit Error Rate (BER) and Bit shifting.
- This matches with the real-life data received by any High-speed Serial IP.

Implementation Details

Channel Model example waveform:



Results Table

Task	Effort	Comments
Architecture Development/Reviews	~45 days	Effort for re-usable TB model development and reviews
Testing	~30 days	Regression failure debug and analysis
Bugs Found	multiple bugs were found	Too Many Pre-silicon RTL bugs pertaining to handling of Skew, Jitter, Bit Shift etc.
Code Coverage Metrics	~20 days	Minimal effort in hitting corner case scenarios

- The proposed method with the sequence of channel models provides 4x reduction in effort when compared to directed testing.
- Adapting this approach has certainly helped in exposing many critical Pre-silicon RTL bugs and reduced the unexpected faults & failures.

Conclusion

- The content of this paper comes from the most common issues faced by the serial IPs operating at high frequencies.
- Designing a robust high-speed serial IP is a critical need due to the increased complexities and functionality in AI, IOT, Automotive, Cloud and Storage applications.
- It makes sense to verify the high-speed serial IPs with real life signal distortion scenarios that are common at high frequencies.
- The proposed method aids in mimicking the real-life scenarios that any complex Serial IP would face and this helps in making a robust IP.
- Thus, a channel model that mimics and adds real life signal distortion factors provides an ideal solution to verify complex high-speed Serial IPs.
- The proposed concept can be extended and adapted for verification of any complex Serial IP (for example – USB,SATA etc.).

REFERENCES

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