Successes and Challenges of Validation Content Reuse

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Summary

Agile, scalable content is a cornerstone to today's hardware validation.

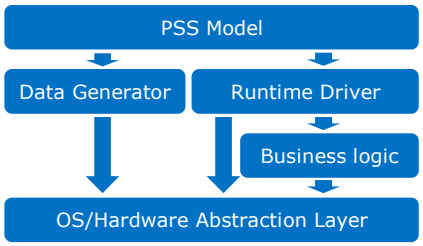
- Hardware coverage is achieved through various platforms (simulation, emulation, post-si)
- IPs and hardware standards continue to increase and evolve
- Validation expands scope from the IP to the SoC

Designing software to validate for this ecosystem is an equally difficult problem to solve. We have taken a multi-year journey down the path to create validation content to validate IPs in pre-silicon validation, extend this to SoC validation, and ultimately reuse this into manufacturing. In this paper, we'll discuss how we have tackled the growing challenges through reuse, our approach to solving a scalability problem, and the results of this effort.

Technical Solution

Focus on IPs:

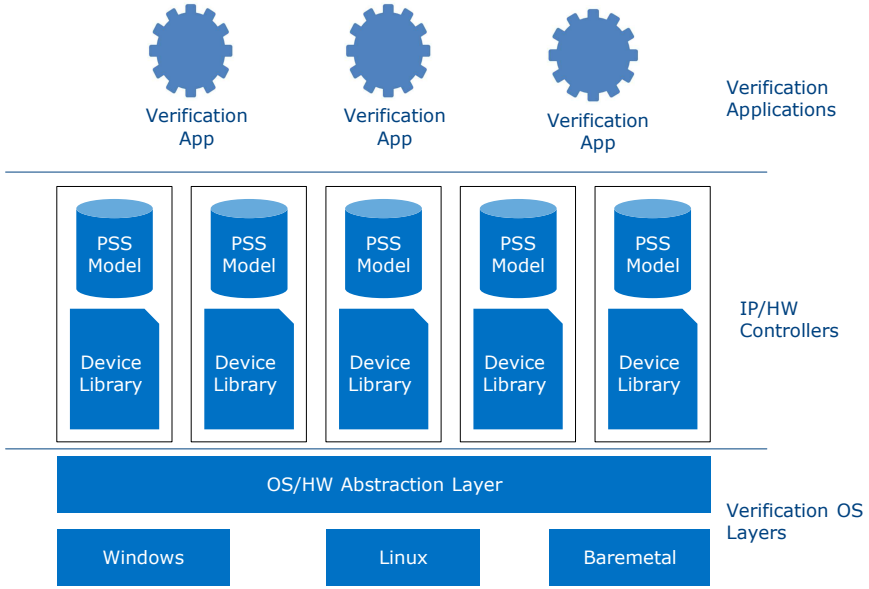
- Specific code partitions
  - PSS Model – Supported operations of the IP
  - Data Generator – data buffers, IP parameter selection/resolution
  - Runtime driver – OS-specific driver
  - Business logic – Device programming



Scalability to SoC:

- Create SoC modeling by combining IPs
- Add support for SoC-specific features

Block Diagram



Description

Verification Apps –

- Utilize PSS modeling and SW drivers for the IP/SoC to create and execute content for full system validation

IP/HW Controllers and Model

- SW implementing the functionality of the IP.
- Modeling expresses the supported, executable intent of each IP.

Verification OS

- Abstraction layers that allow code to be reusable across different execution OS targets and platforms (sim., emu. silicon)

Future Directions

Portable Stimulus

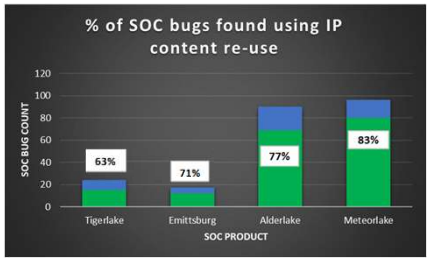
- Standardize modeling to industry standards
- 70% of current needs addressed by standards
  - Drive for closure on remaining modeling challenges and gaps

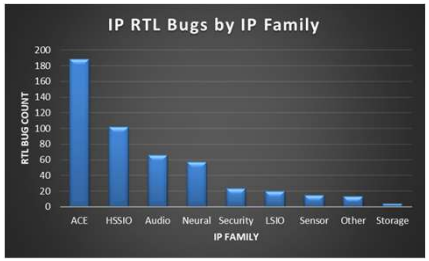
Scalability – Verification OS

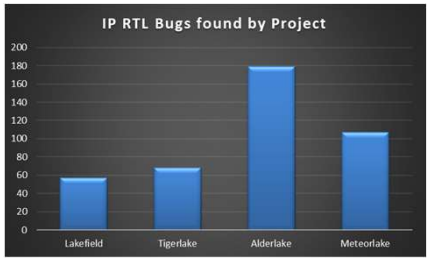
- A foundation for interoperable code that scales across different platforms and usage models
- Allows internal and 3rd party collateral to be used together
- Addresses scalability of different ISAs (x86, ARM, RISC-V, etc.)

Impact and Results

Downstream Re-use Customers	HC Savings
South complex pre-si	4
North complex pre-si	4
Cross-die pre-si	4
Post-si Client/Devices	14
Manufacturing	6
Total	**32**







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