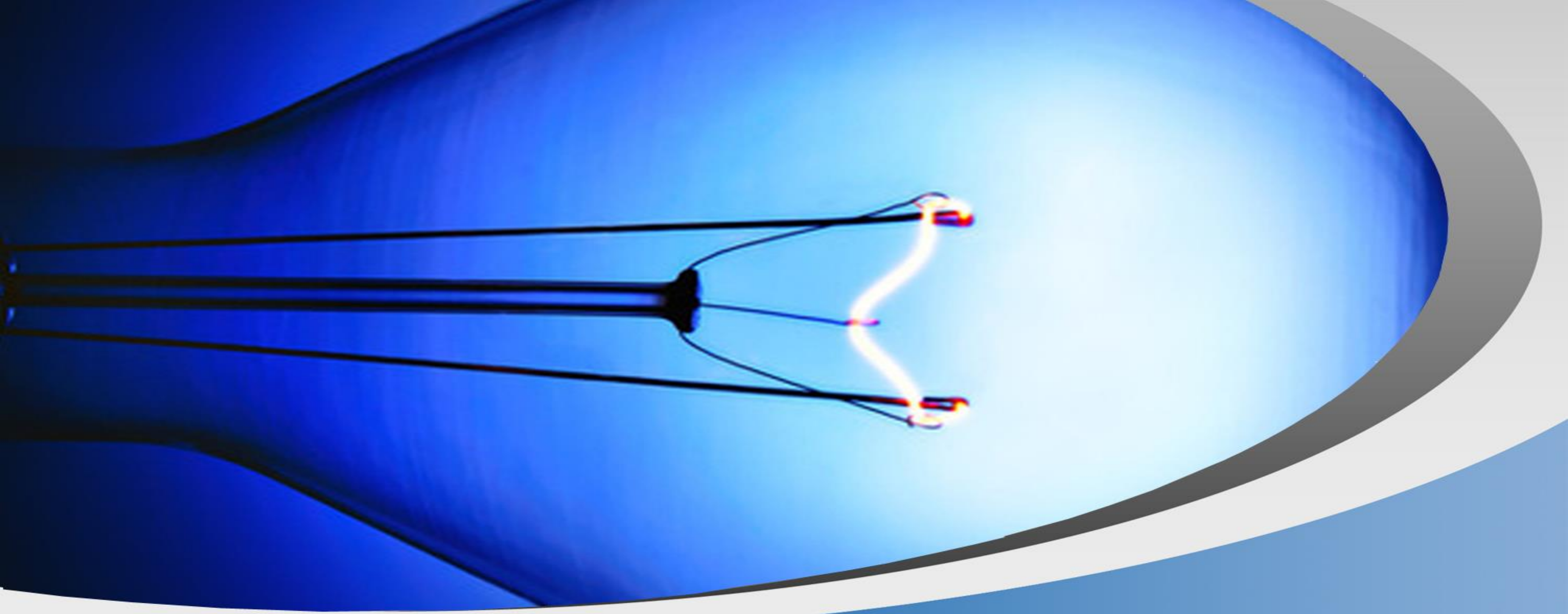


Accellera Overview

October 2025

Lu Dai | Accellera Chair

accellera
SYSTEMS INITIATIVE

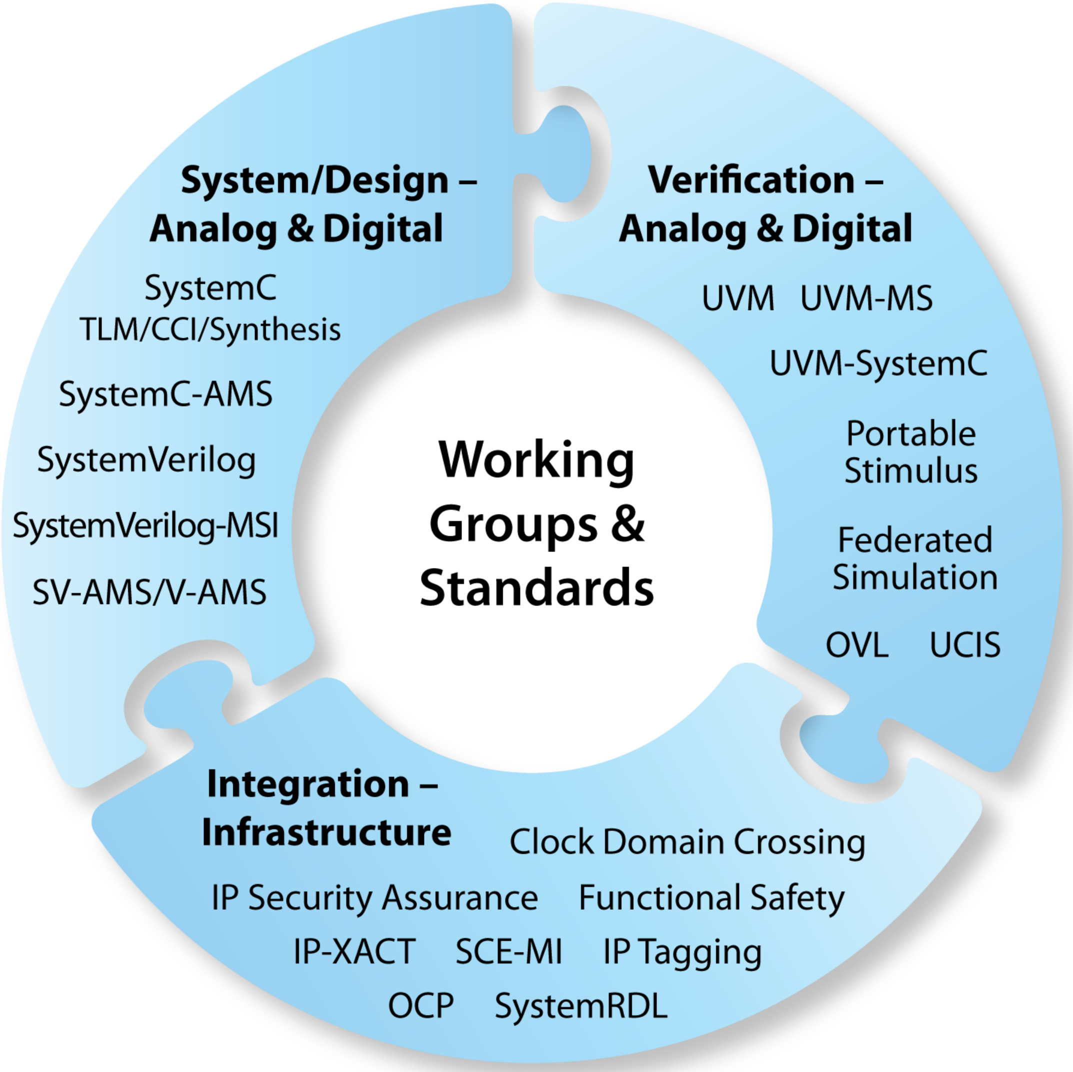
Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global Electronic Design Automation and IP standards that improve design and verification productivity for today's advanced integrated circuits and embedded systems. In addition, we strive to promote the widespread adoption of these standards.

PORTABLE STIMULUS
SYSTEM C™
SystemVerilog
VHDL
UVM
IP-XACT™
SystemRDL™
UPF UNIFIED POWER FORMAT

The Accellera Ecosystem



System/Design – Analog & Digital

SystemC TLM/CCI/Synthesis

SystemC-AMS

SystemVerilog

SystemVerilog-MSI

SV-AMS/V-AMS

Verification – Analog & Digital

UVM UVM-MS

UVM-SystemC

Portable Stimulus

Federated Simulation

OVL UCIS

Integration – Infrastructure

Clock Domain Crossing

IP Security Assurance Functional Safety

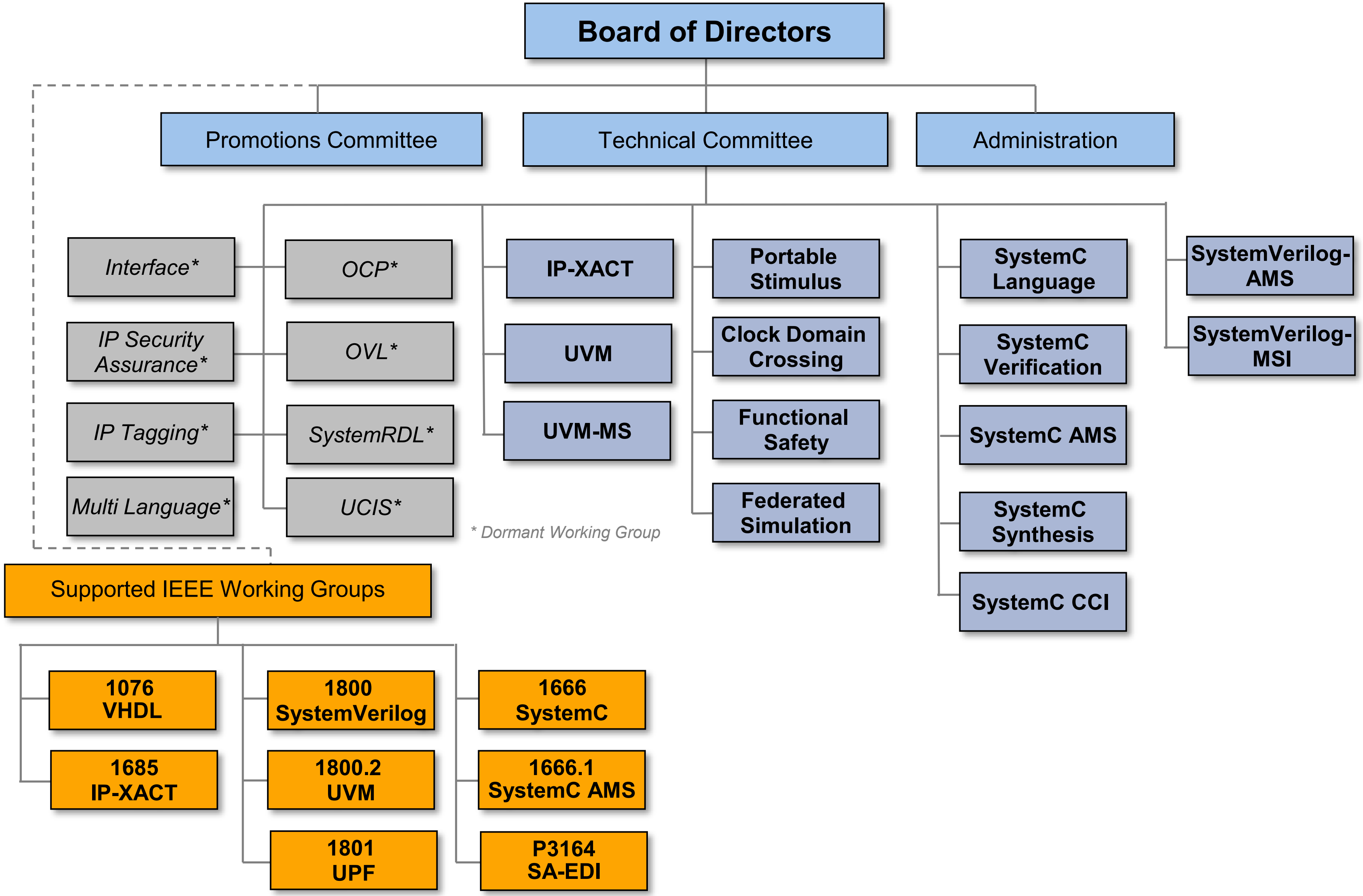
IP-XACT SCE-MI IP Tagging

OCP SystemRDL

Working Groups & Standards

Helping you bring all the pieces together

Accellera Systems Initiative



* Dormant Working Group

Broad Industry Support

Corporate Members

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NVIDIA RENESAS S2C EDA SOLUTIONS SAMSUNG SANDISK

Scientific Analog Ubilinx Ubilinx Technology, Inc. Vayavya Labs Pvt. Ltd. Verific Design Automation

CDC Working Group and Accellera

- **Charter**
  - Define a standard CDC collateral specification to ease SoC integration
  - Address incompatibility of collateral generated by different CDC verification tools
- **Scope**
  - Develop a standard format to capture CDC/RDC/Glitch intent
  - Produce a formal Language Reference Manual (LRM)
- **History**
  - Holistic SoC-level CDC verification requires reconverge IP with SoC
  - SoC teams can’t reuse IP-level CDC collateral in the SoC environment if teams use different CDC tools
  - Standardization of CDC collateral will bring significant benefits to product companies, IP design houses, EDA tool companies, and the entire ecosystem
  - Accellera Board approved the official Working Group in December 2022

Accellera and IEEE

- Accellera will release 10 standards for 10 years under an extended IEEE Get program
- IEEE standards Access at No Charge
- More than 221,000 downloads to date!

IEEE GET EDA Standards

Download IEEE Standards

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- or find links to specific standards at -

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SIEMENS

SYNOPSYS

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

MUNICH, GERMANY
OCTOBER 14-15, 2025

CDC-RDC Standardization: Concepts & Status

AGNISYS SYSTEM DEVELOPMENT WITH CERTAINTY	Anupam Bakshi Aiyush Aggarwal Rahul Parashar
SIEMENS	Farhad Ahmed Abdelouahab Ayari Yassine Eben Aimine
ST life.augmented	Jean-Christophe Brignone Ashish Soni
arm	Don Mills

Blue Pearl Solutions™	Bill Gascoyne
BOSCH	Jan Hayek
Infineon	John Selwyn Shimron Jebakumar
intel.	Jebin Mohandas
MARVELL™	Jebin Mohandas
Qualcomm	Suman Chalana
RENESAS	Kranthi Pamarthi

Accellera CDC Working Group

accellera SYSTEMS INITIATIVE

Presenters Bio

- **Yassine Eben Aimine**
  - Yassine works currently as Product Architect for the Static and Formal verification division at Siemens EDA.
  - Yassine has over 25 years of experience in the semiconductor industry mainly in EDA. Spanning several roles and domains in both RTL implementation and verification
  - As part of Product Engineering at Siemens, Yassine has responsibility for aligning product roadmaps with latest industry trends by defining technical requirements for the static and formal tools
  - Yassine holds an Engineering Diploma from the ENSET, Toulouse (France)

Presenters Bio

- **John Selwyn Shimron Jebakumar**
  - is currently a Principal Engineer leading Digital IP development and owning the RTL Sign-off Methodologies at Infineon Technologies AG from within the Central Engineering Group located in Dresden, Germany
  - holds an M.Sc. in Microelectronics Systems Design from the University of Southampton (UK) and a B.E. in Electrical and Electronics Engineering from Anna University, Chennai (India)
  - has 10+ years of experience working in Standard-cell, I/O, and Memory modeling; Digital IP design and automation; and RTL sign-off workflows
  - contributes to the Accellera ‘CDC/RDC’ Working Group from within the Output Collateral and Training sub-groups

Presenters Bio

- **Jean-Christophe Brignone**
  - JC works currently as a Senior Member of the Technical Staff for the CDC-RDC Verification of RF & MPU SoC at STMicroelectronics in Grenoble (France), leading the Company level CDC-RDC Verification Methodology Working Group for tool-flow deployment
  - He is a member of the Accellera Working Group "CDC", leading the “Training” subgroup & representing his Company as voter
  - He has authored over 18 papers on static checks and Hierarchical flows, presented at industrial & scientific international conferences and won Best Paper awards
  - Reaching more than 26 years of experience in the semiconductor industry as digital designer, he specializes in static & formal verification for 12 years
  - He holds a Master degree in Microelectronics engineering from the University of Toulouse (France)

Presenters Introduction

- **Yassine Eben Aimine**
  - Product Architect for the Static and Formal verification division at Siemens EDA in UK
  - 25+ years of experience
  - Responsible in the Product Engineering at Siemens for aligning product roadmaps with latest industry trends
- **John Selwyn Shimron Jebakumar**
  - Principal Engineer at Infineon Technologies AG in Dresden (Germany)
  - 10+ years of experience
  - owning the RTL Sign-off Methodologies at Infineon Technologies AG
- **Jean-Christophe Brignone**
  - Senior Member of the Technical Staff at STMicroelectronics in Grenoble (France)
  - 26+ years of experience
  - Leading the CDC-RDC Verification Methodology Working Group at Company level

Agenda

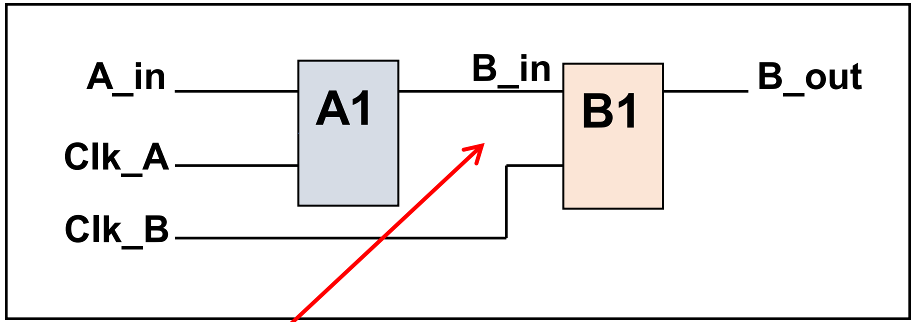
	Topic	Slide update/create	Presenter	Time
#0	**Workshop introduction**		**Lu Dai**	**8m**
#1	**CDC-RDC**			**50m**
	CDC-RDC Basic Knowledge	Bill Gascoyne (Blue Pearl), Jan Hayek (Bosch Sensortec)	**Yassine Eben Aimine (Siemens EDA)**	8m
	Setup Constraints & Verification	Ping Yeung (Nvidia) Jebin Vijai (Intel)	**Yassine Eben Aimine (Siemens EDA)**	5m
	Structural CDC/RDC	Chetan Choppali Sudarshan (Marvell) Suman Chalana (Qualcomm)	**Yassine Eben Aimine (Siemens EDA)**	10m
	CDC Assertion-Based Verification	Kranthi Pamarthi (Renesas Electronics), Don Mills (ARM)	**John Jebakumar (Infineon)**	12m
	CDC-RDC Hierarchical Flow	Jean-Christophe Brignone, Ashish Soni (STMicroelectronics)	**Jean-Christophe Brignone (ST)**	5m
	Q & A			10m
#2	**Accellera CDC WG**			**32m**
	Standard	Iredamola Olopade, Jebin Vijai (Intel)	**Jean-Christophe Brignone (ST)**	3m
	Assertion	Kranthi Pamarthi (Renesas Electronics), Don Mills (ARM)	**John Jebakumar (Infineon)**	3m
	Output	Joachim Voges (Infineon), Devender Khari (Agnisys)	**John Jebakumar (Infineon)**	5m
	Testing	Farhad Ahmed (Siemens EDA), Suman Chalana (Qualcomm)	**Jean-Christophe Brignone (ST)**	3m
	Format	Devender Khari (Agnisys)	**Jean-Christophe Brignone (ST)**	3m
	Training	Jean-Christophe Brignone, Diana Kalel, Ashish Soni (ST)	**Jean-Christophe Brignone (ST)**	3m
	Call For Contribution	Jean-Christophe Brignone (ST), Anupam Bakshi (Agnisys)	**Jean-Christophe Brignone (ST)**	2m
	Q & A			10m

1.1 CDC-RDC Basic Knowledge:

CDC-RDC Basic Knowledge:

- Synchronous vs. asynchronous clocks
- Problems related to Clock Domain Crossing (CDC)
- CDC Synchronization
- Problems related to Reset Domain Crossing (RDC)
- RDC Synchronization

What is Clock Domain Crossing?

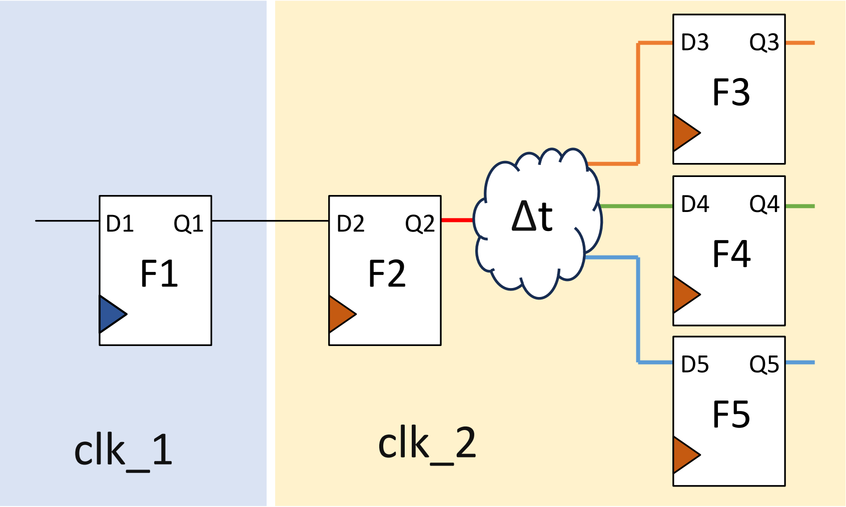


- What is a Clock Domain?
  - flip-flops with same clock (clock tree) or derived clocks sharing the same source
- Clock Domain Crossing
  - Data from one clock domain is captured (sampled) in another clock domain

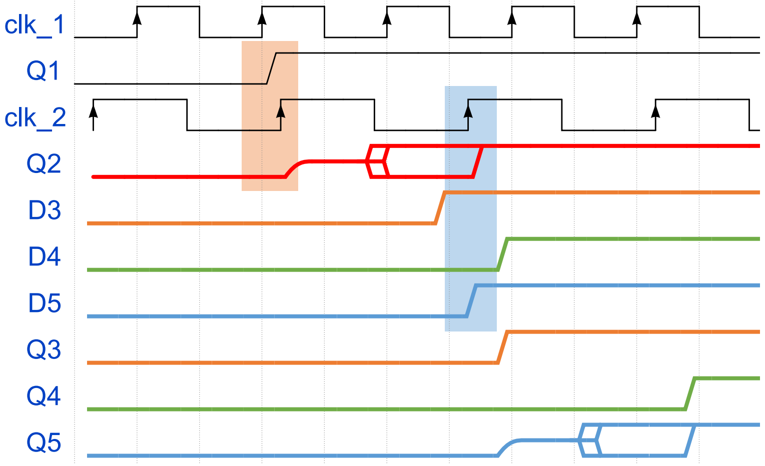
Why do CDCs need fixing?

- Metastability
  - Timing violations on registers resulting in an indeterminate state lasting long enough to violate timing assumptions of the following circuits

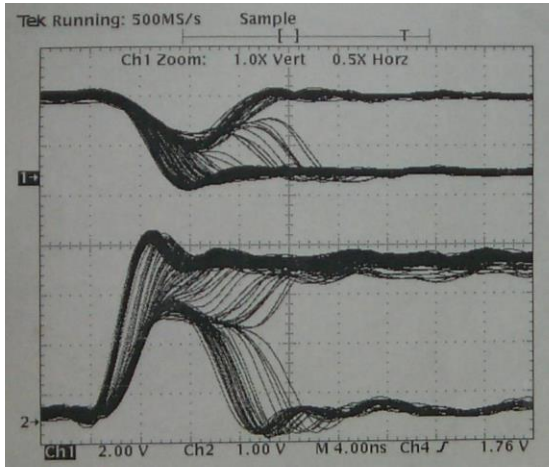
    … the coin decided too late / has not decided yet



(a) structure



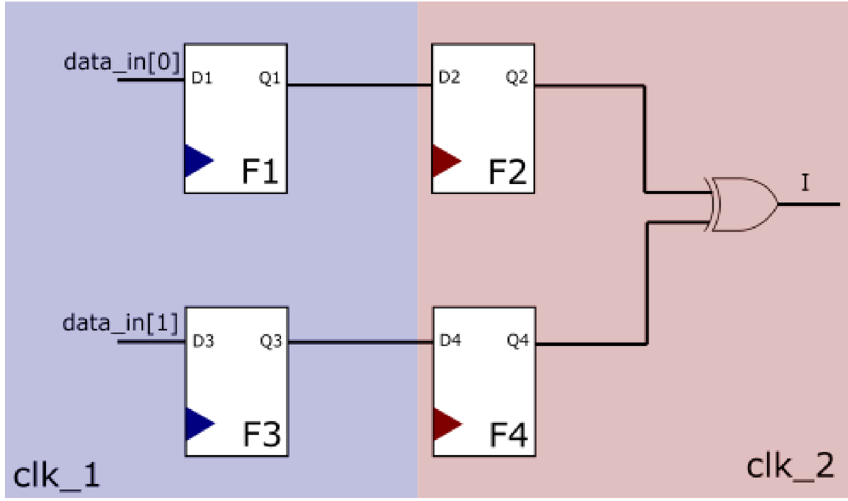
(b) waveform



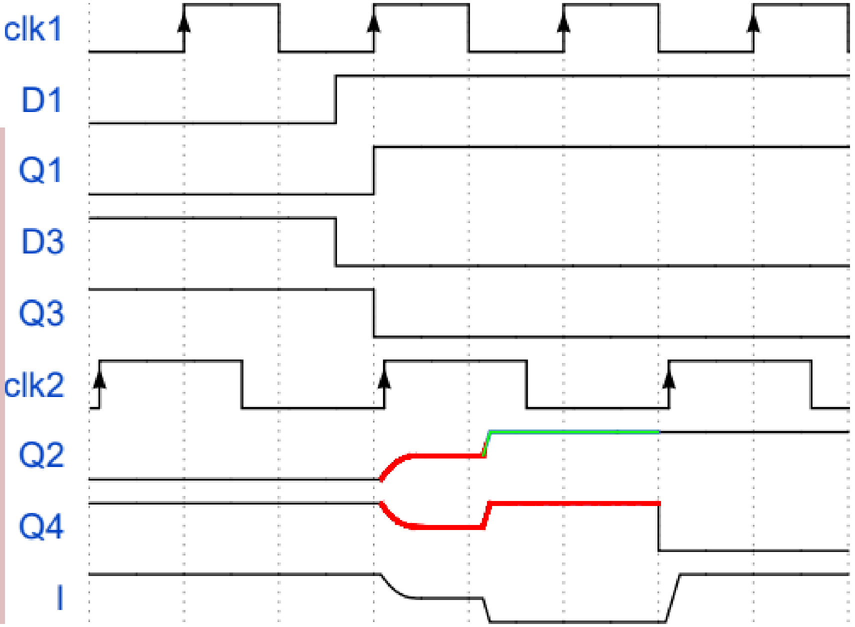
(c) Physical representation

Why do CDCs need fixing?

- Loss of Data Coherency
  - The indeterminate state settles to a random value



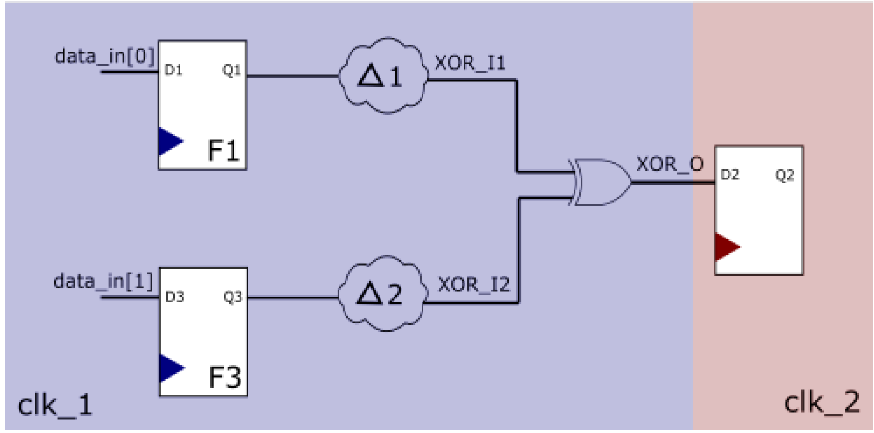
(a) Structure



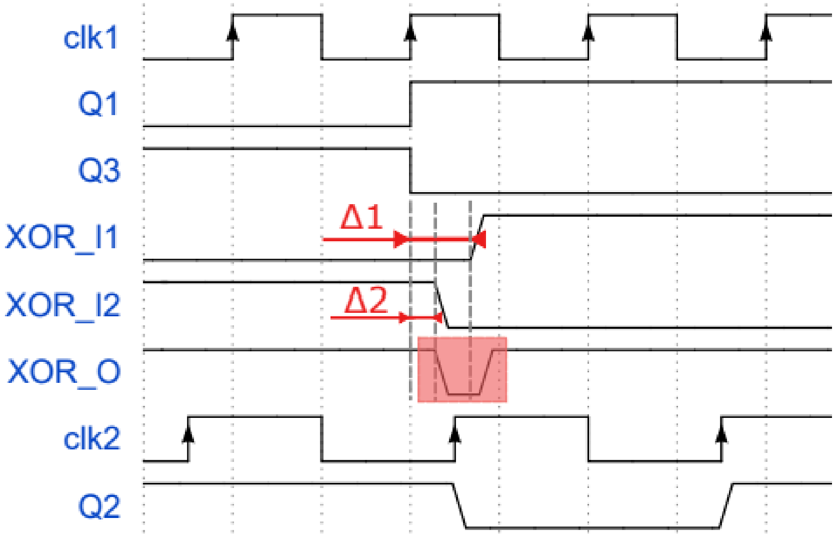
(b) Waveform

Why do CDCs need fixing?

- Glitches
  - Multiple synchronized paths reconverge to cause unexpected momentary transitions



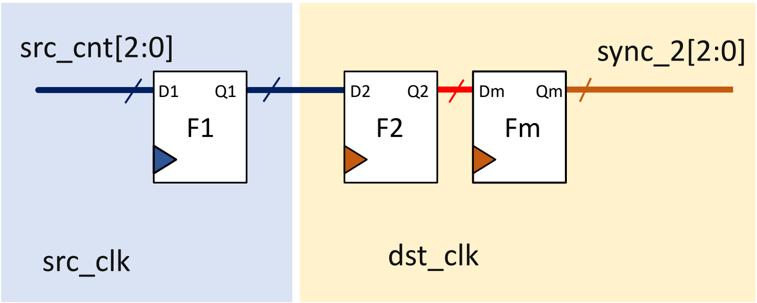
(a) Structure

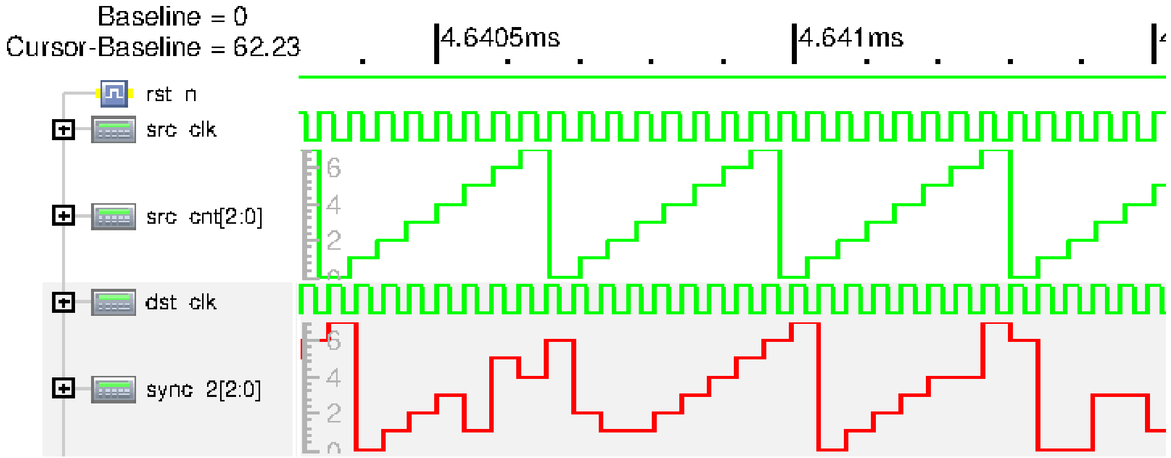


(b) Waveform

Synchronization

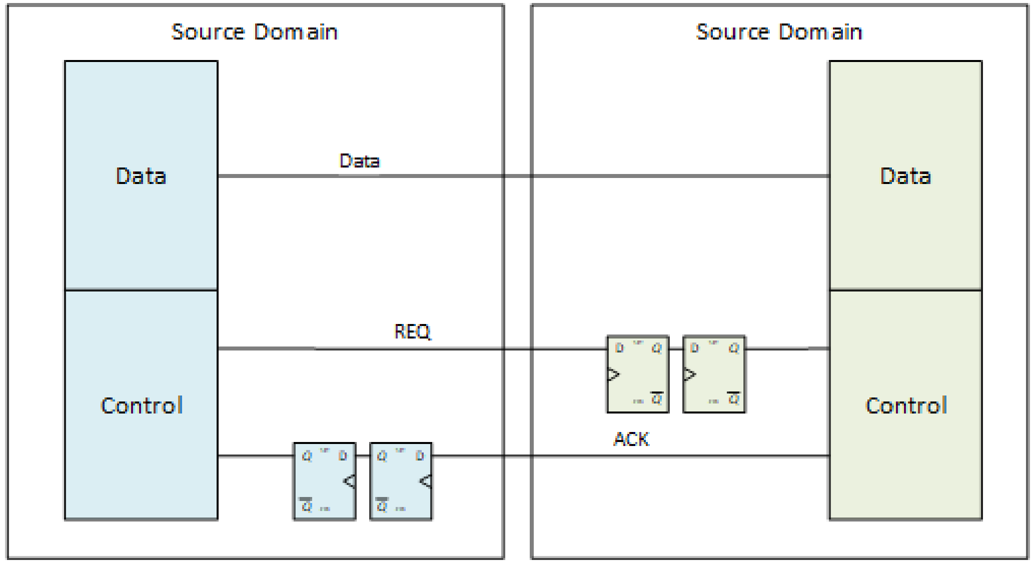
- With multiple bits, metastability is still addressed but data coherency is a problem!
  - If multiple bits change on the same cycle, the result of each bit is random
  - This synchronization works only if the data is “gray” (only one bit changes)



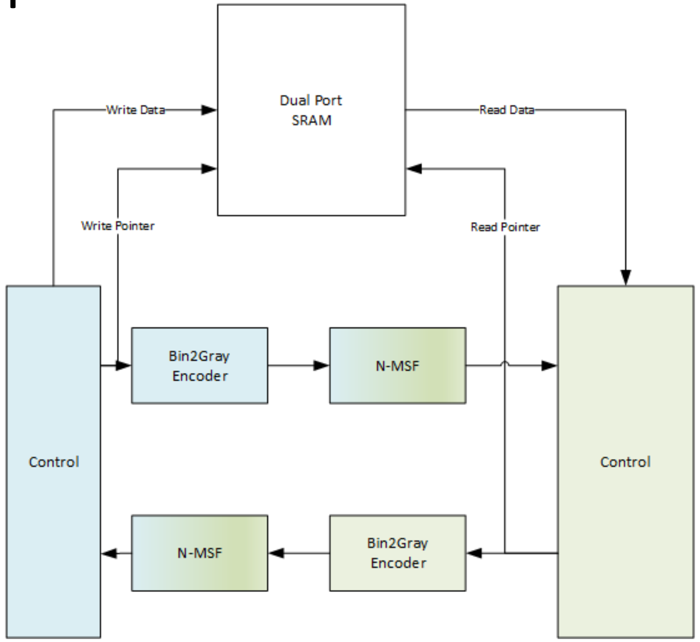


More Complex Synchronization

- Handshake Protocol

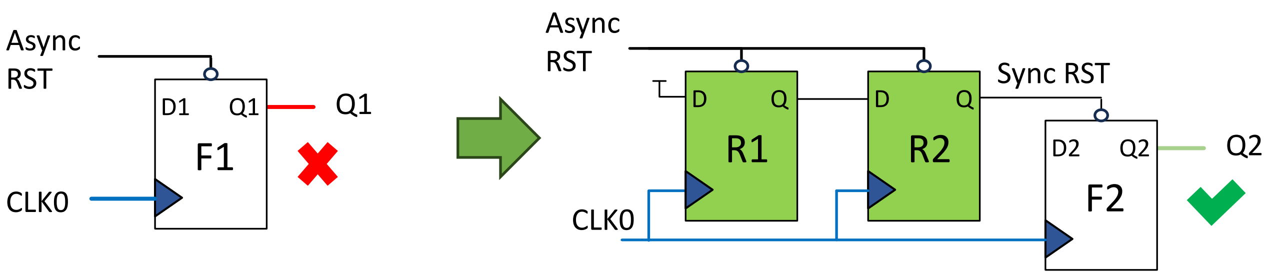


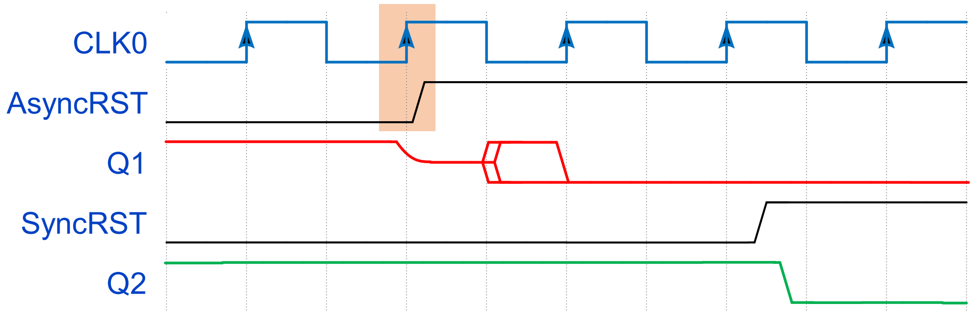
- FIFO
  - Increased bandwidth
  - Throttling
  - Handles intermittent peaks of incoming data rate



Asynchronous Reset Release

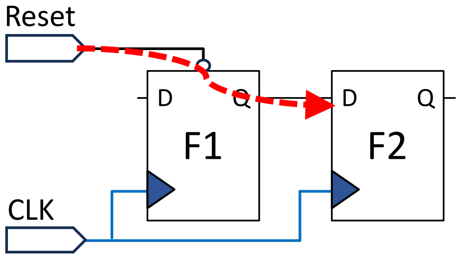
- In addition to setup- and hold-, DFF models also have **recovery-time**
    - Time between asynchronous Set/Reset release and clock when data and output are different
    - Violating recovery time is no different than violating setup/hold
- Possible to synchronize asynchronous reset on release edge only
    - Static analysis is sufficient to make this determination

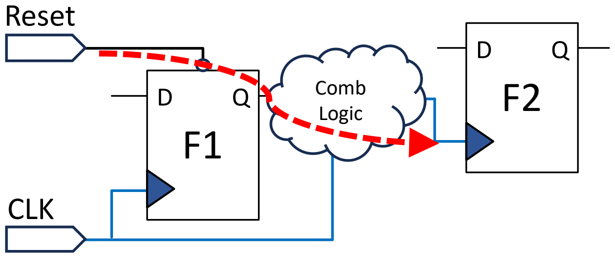




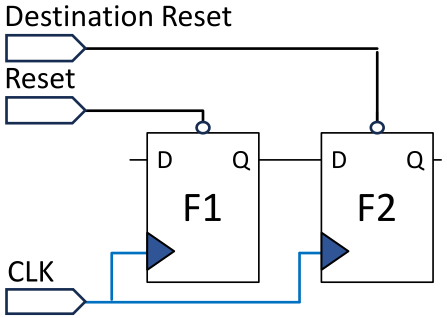
The Reset assertion RDC problem

- Paths passing from CLR to Q are usually not timing closed



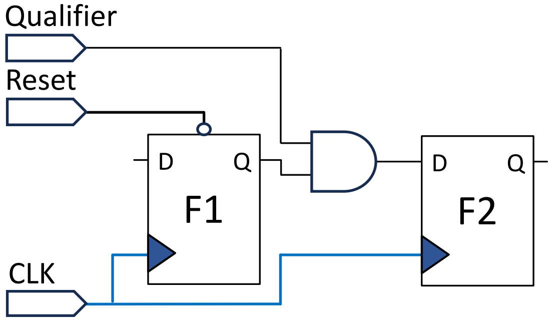


- Using reset ordering



- Using a CDC Control

  CDC Control must be synchronous with target domain



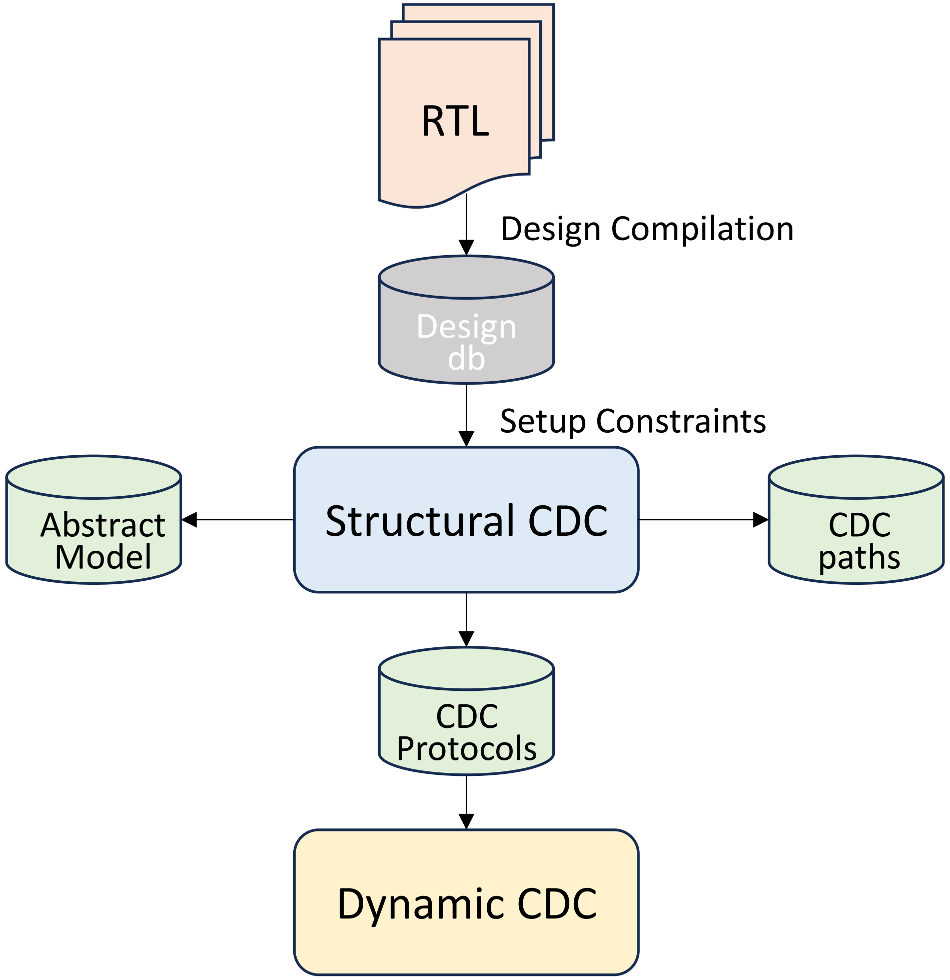
1.2 CDC Setup & Constraints

CDC Setup & Constraints

- CDC Verification flow
- Setup constraints
- Challenges

CDC Verification flow

- Design Compilation
  - Parameters, defines
  - SV packages, SV configuration, SV interfaces
- Setup Constraints
  - Clock, reset, and IO signals
  - Configuration: stable, constant inputs
- Structural CDC Check
  - CDC schemes validation and debugging
- Abstract Model Generation
- Dynamic/Formal CDC Verification
  - CDC constraints and protocols



Setup Constraints

- The set of constraints used to guide CDC verification

- Clocks
- Resets
- Configuration signals
- Black boxes
- Primary inputs/outputs

Don’t rely blindly on timing constraints

⚠

Reusing timing constraints is risky

- Pseudo-static signals
- Exclusive signals
- Gray coded buses
- Custom synchronizers
- False path

Clock groups for timing analysis ≠ Clock groups for CDC analysis
Signal paths waived for timing analysis ≠ Signal paths waived for CDC analysis

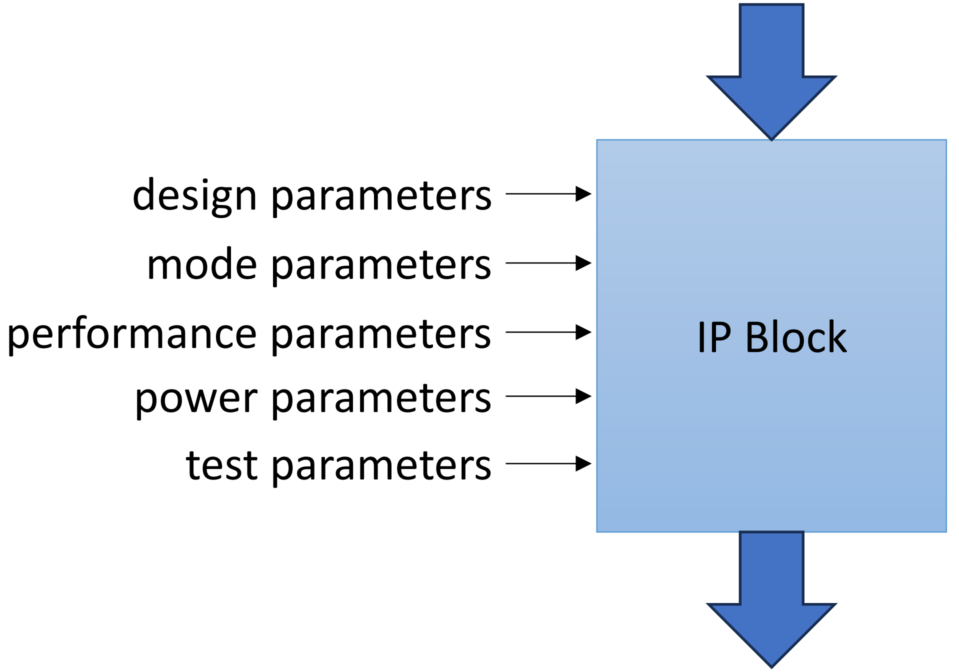
Challenge #1: Design Parameters

- Blocks/IPs have many parameters
  - Some used for design, performance, optimization
  - Some used for integration, mode
  - Some used for DFT, DFP, DFM, etc

- Most parameters will affect CDC results

- Some parameters may not affect CDC results
  - Data_width, Addr_width
  - RAM_size

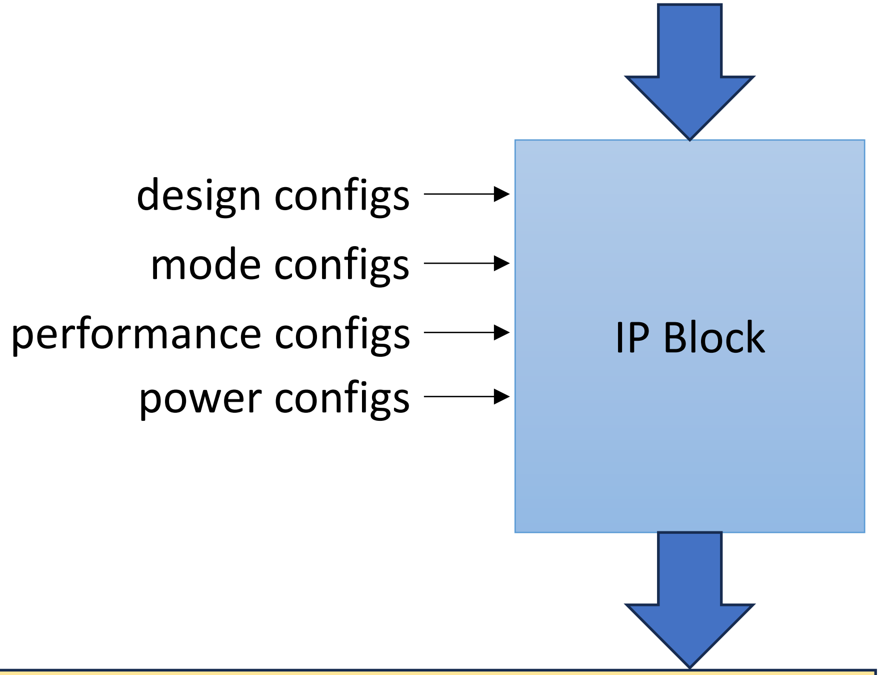
- The Abstract Model will become parameter-specific



Specifying design parameters is essential

Challenge #2: Configuration Signals

- Blocks/IPs have many configuration signals
  - Some used for design, performance, optimization
  - Some used for integration, mode
  - Some used for DFT, DFP, DFM, etc
- Most configuration signals will affect CDC results
  - Clock select, gating signals
- The Abstract Model will become configuration-specific



Specifying constraints on configuration signals is essential

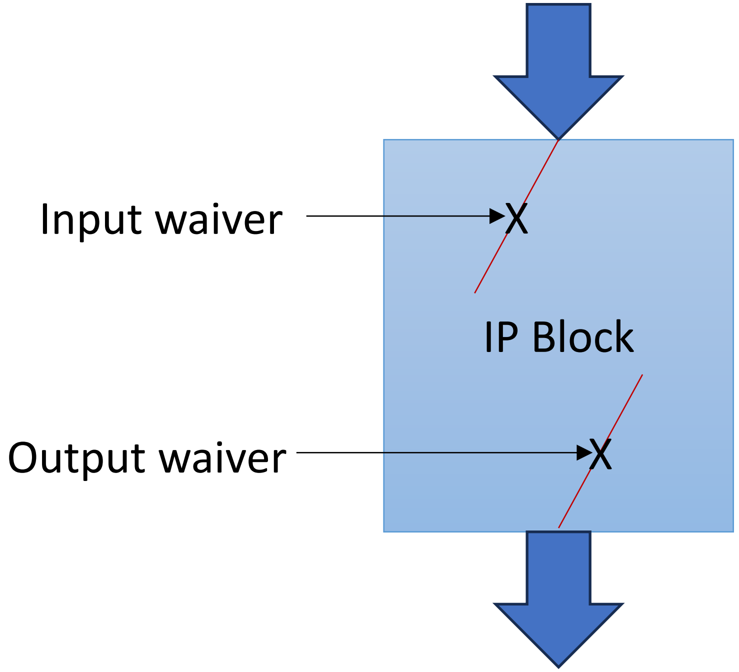
Challenge #3: CDC Waivers

- Blocks/IPs have many CDC violations
  - Some are on the input signals
  - Some are on the output signals

- Some of the input violations can be waived
  - Pseudo-static input signals
  - Output signals

- Some of the input violations must not be waived

- The Abstract Model will become waiver-specific



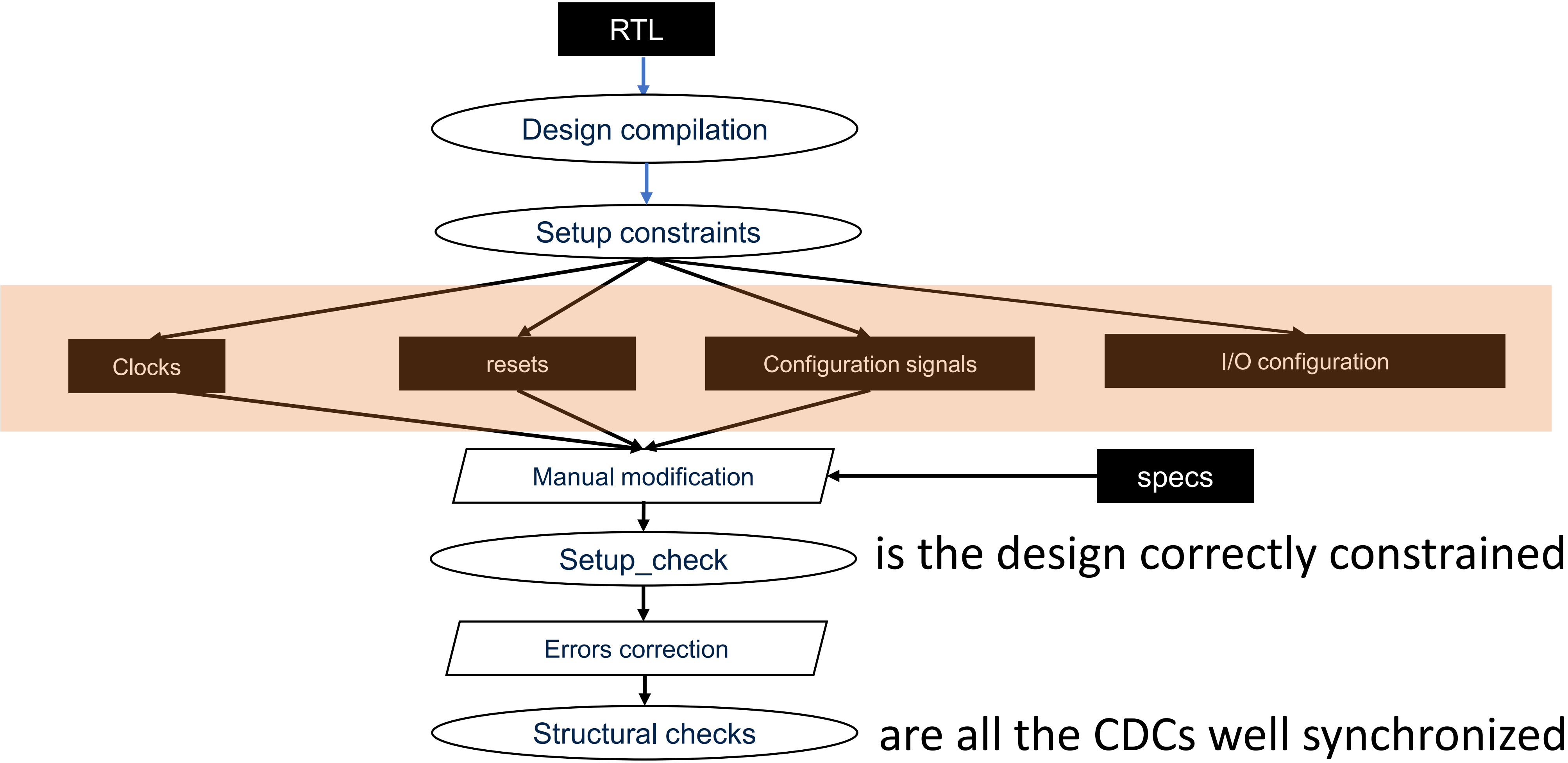
Specifying waivers is useful

1.3 Structural CDC/RDC

Structural CDC/RDC

- Structural CDC
- User defined synchronization modules
- CDC constraints
- Reset Domain Crossings

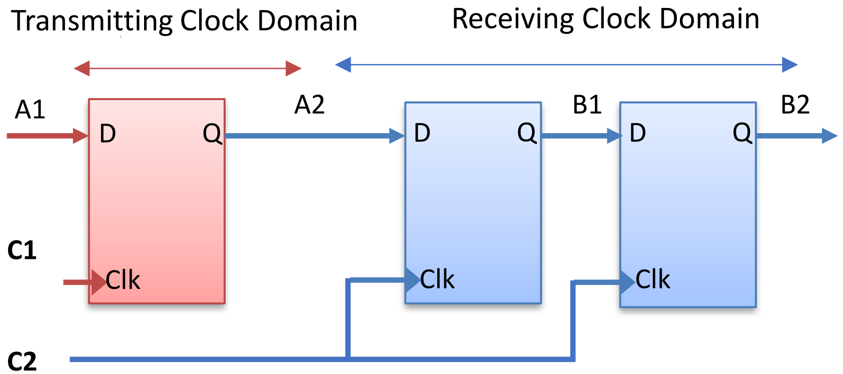
Structural CDC Analysis Process



is the design correctly constrained ?

are all the CDCs well synchronized ?

Structural CDC - Commonly Used Synchronization Schemes

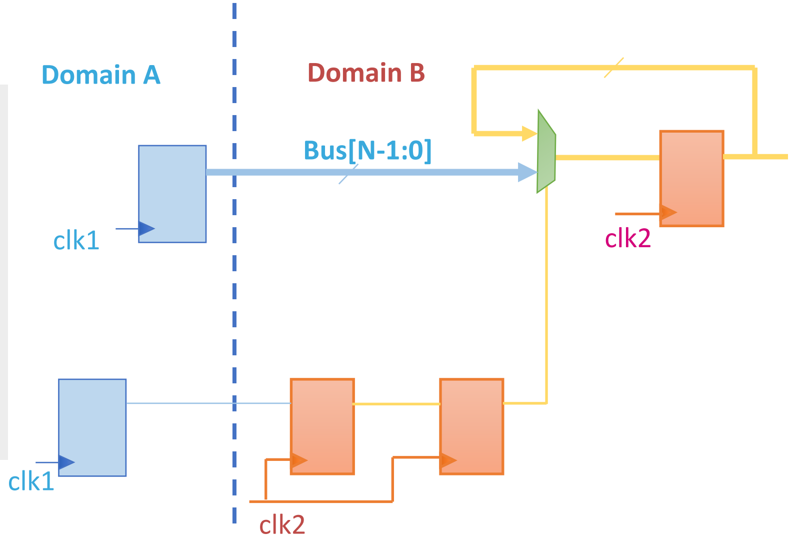


Double-FF synchronizer

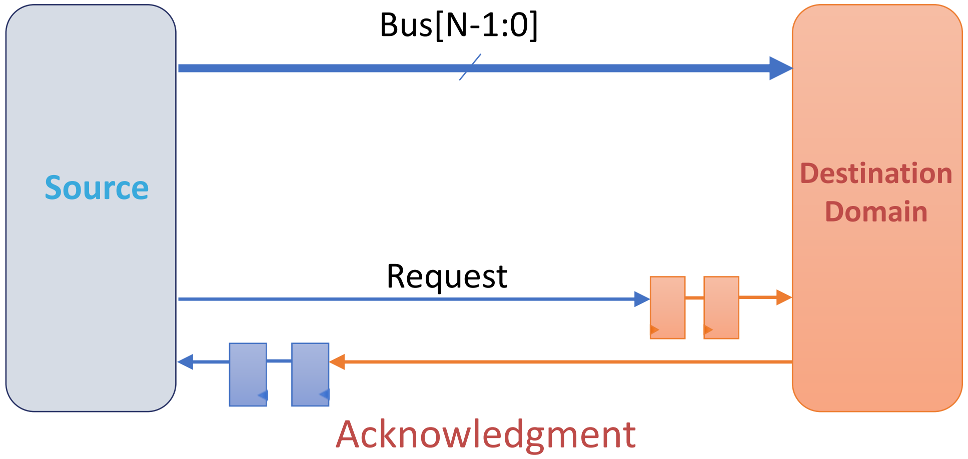
CDC Component:

- Disable automatic detection of the specific synchronizer type that you don't want the tool to recognize automatically.
- Declare your own scheme as user-defined synchronizer (before scheme detection)

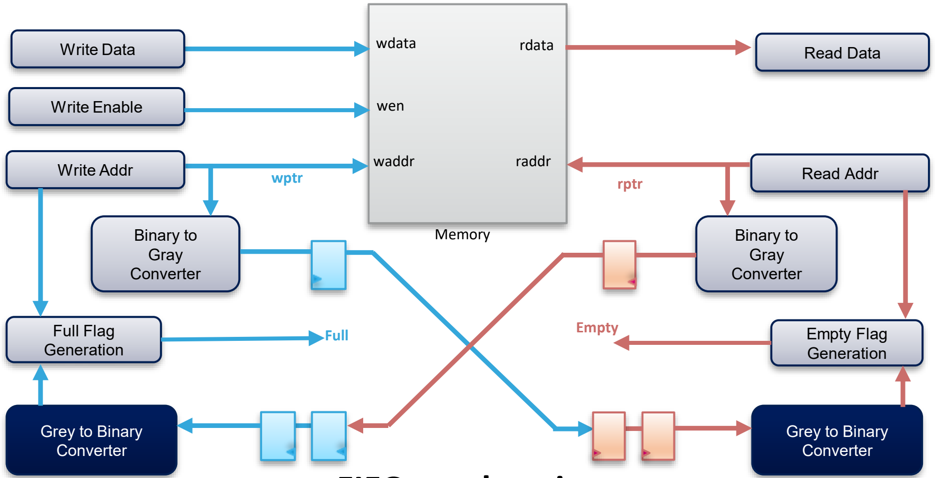
Eg: 2DFF cdc component



MUX synchronizer



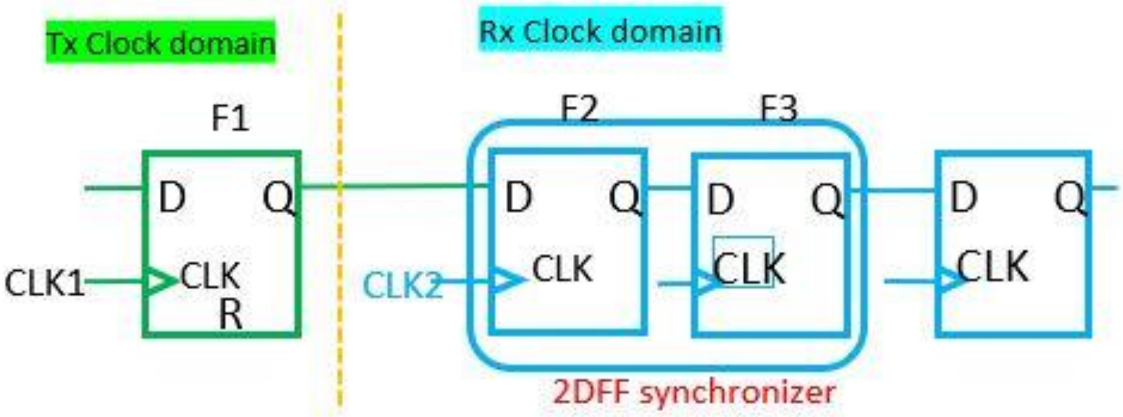
Handshake synchronizer



FIFO synchronizer

Structural CDC – User defined sync modules

- Double FF Synchronizer
  - Most design houses prefer to use their own CDC components
    - Disable automatic detection of the specific synchronizer type that you don't want the tool to recognize automatically
    - Declare your own scheme as user-defined synchronizer (before scheme detection)
  - Example: Use my own 2DFF only
    - Disable auto-detection of 2DFF
    - Declare your own module as 2DFF



Structural CDC

- Various Signal Configurations possible for structural CDC Analysis
  - Constant
  - Static
  - Mutually exclusive / Gray code
  - Externally synchronized
  - CDC False paths
    - *Not recommended (avoid using it to mask real CDCs)*
- Purpose
  - Define signal behavior that can help to reduce CDC analysis noise
    - Exclude certain paths which may not have any standard synchronizer but safe for CDC
    - Helps to speed up CDC analysis

Structural CDC

- CDC Constraints – Constant Declaration
  - It can be applied on a port or on an internal signal
  - A constant signal does not change in a given mode and hence does not cause a CDC issue

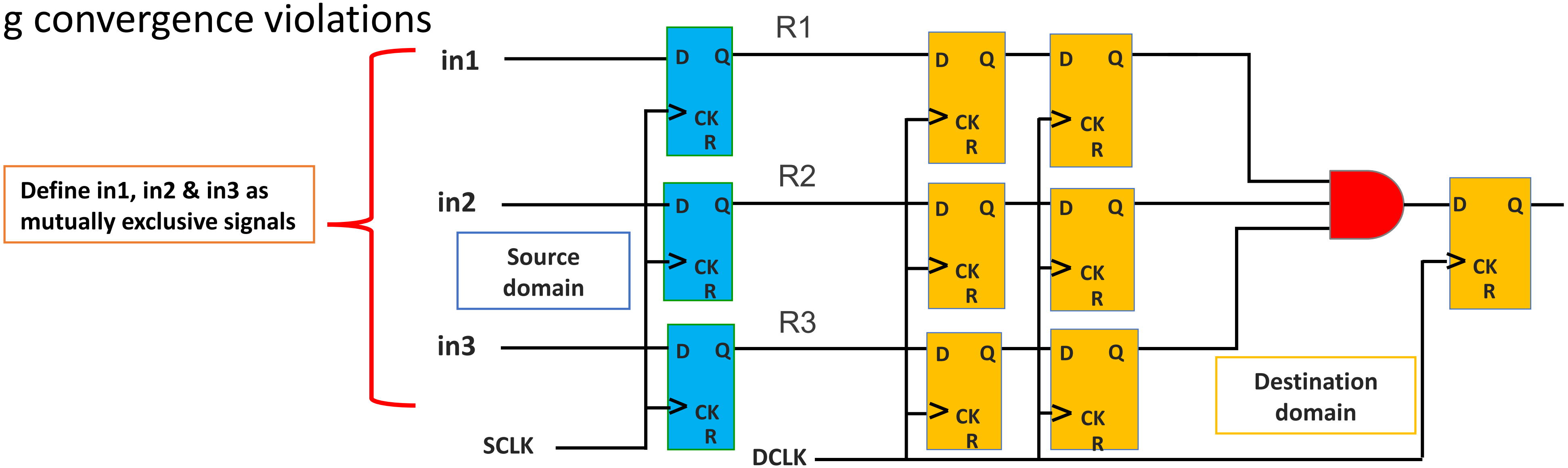
- Purpose
  - Define signal behavior that can help to reduce CDC analysis noise
    - Exclude certain paths which may not have any standard synchronizer but safe for CDC
    - Helps to speed up CDC analysis

Structural CDC

- CDC Constraints – Static Declaration
  - Any signal that does not change while the destination is active
  - Same as quasi-static or pseudo-static
  - A static signal does not cause CDC issues because
    - The receiver clock is not active
    - The receiver is under reset

Structural CDC

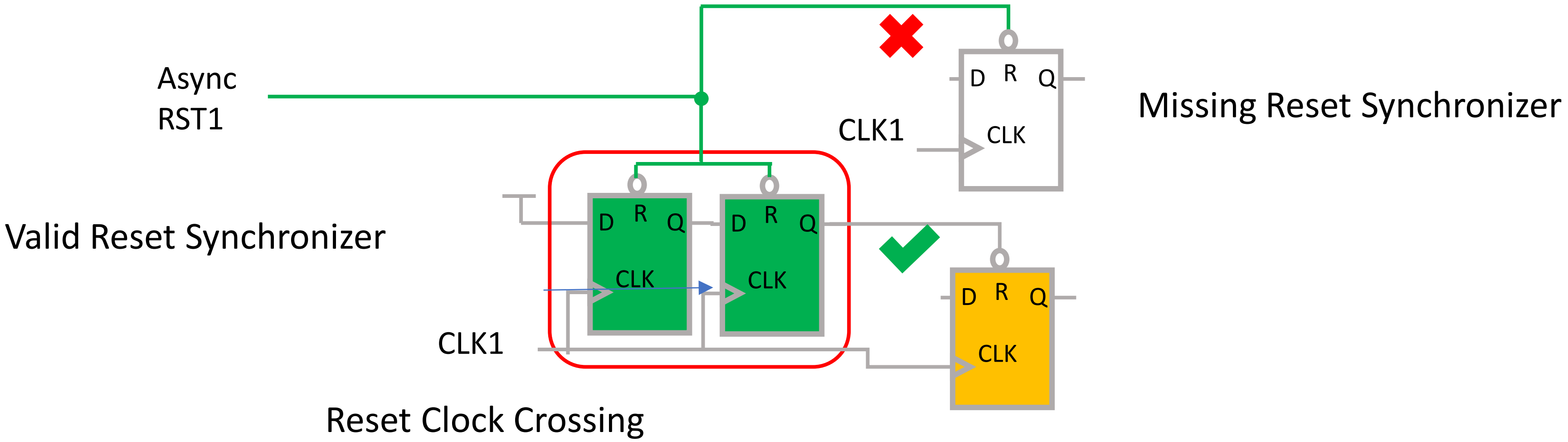
- CDC Constraints – Gray Coded Declaration
  - A bus can be specified as gray coded – Only one bit can toggle at a time
- CDC Constraints – Mutually Exclusive Toggle Declaration
  - A set of independent signals that can toggle only one at a time can be defined as mutually exclusive toggle
    - Helps in avoiding convergence violations



Structural CDC

- CDC Constraints - Externally Synchronized
  - A block level input/output port can be declared as *externally synchronized*
    - Represents the output of a control synchronizer (2DFF/Edge/Pulse)
    - Can be used as the control path for complex synchronizers (MUX Synchronizer, Glitch Protector)
    - Helps in auto-detection of the above composite synchronization scheme types
- CDC Constraints - CDC False Path Declaration
  - CDC Checks can be disabled on certain paths by user-defined constraints
  - User can set a constraint to let the tool automatically identify a functionally false path and hence reports the path as a safe path

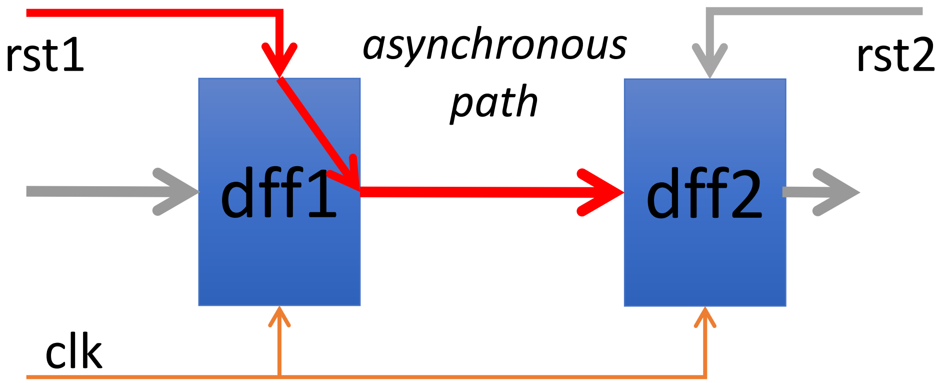
Asynchronous Reset De-assertion



- Reset signal crossing from one clock domain to another
  - The asynchronous de-assertion of the reset signal at the destination flop can cause the signal to become metastable
  - Reset signals are required to be synchronized to destination domains for synchronous de-assertions

Reset-Domain Crossing

- Asynchronous reset domains causes meta-stability
  - Contain registers whose resets are asserted asynchronously
  - Originate in one asynchronous reset domain
  - Sampled by register(s) in a different reset domain
  - Reset ordering of different resets in the design

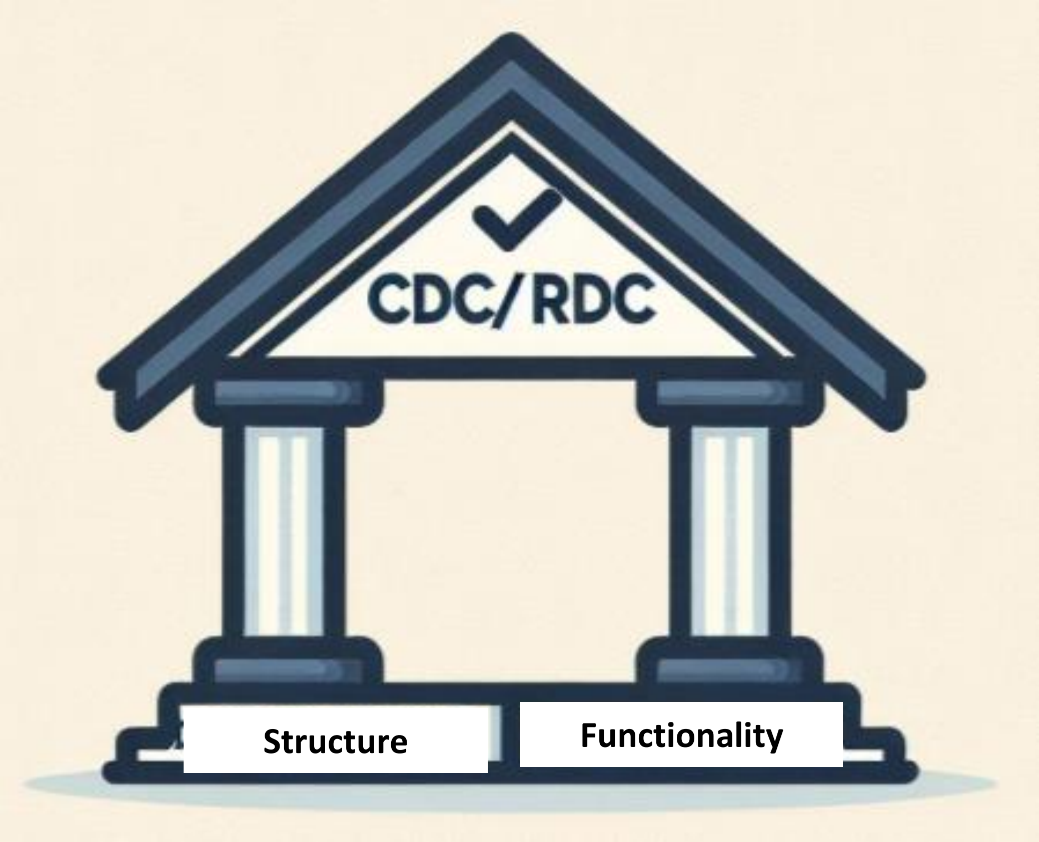


1.4 CDC Assertions

CDC Assertions

- Assertion Based Verification
- Overcoming Limitations

Structural Verification vs Assertion



- ***Structural CDC/RDC Verification*** analyze the design structure. It doesn’t analyze the design functionality. As long as the structure is valid, the verification pass.
- ***Assertions*** covers design functionality. They can be used in Dynamic Simulation and/or Formal Verification.

Valid CDC/RDC =

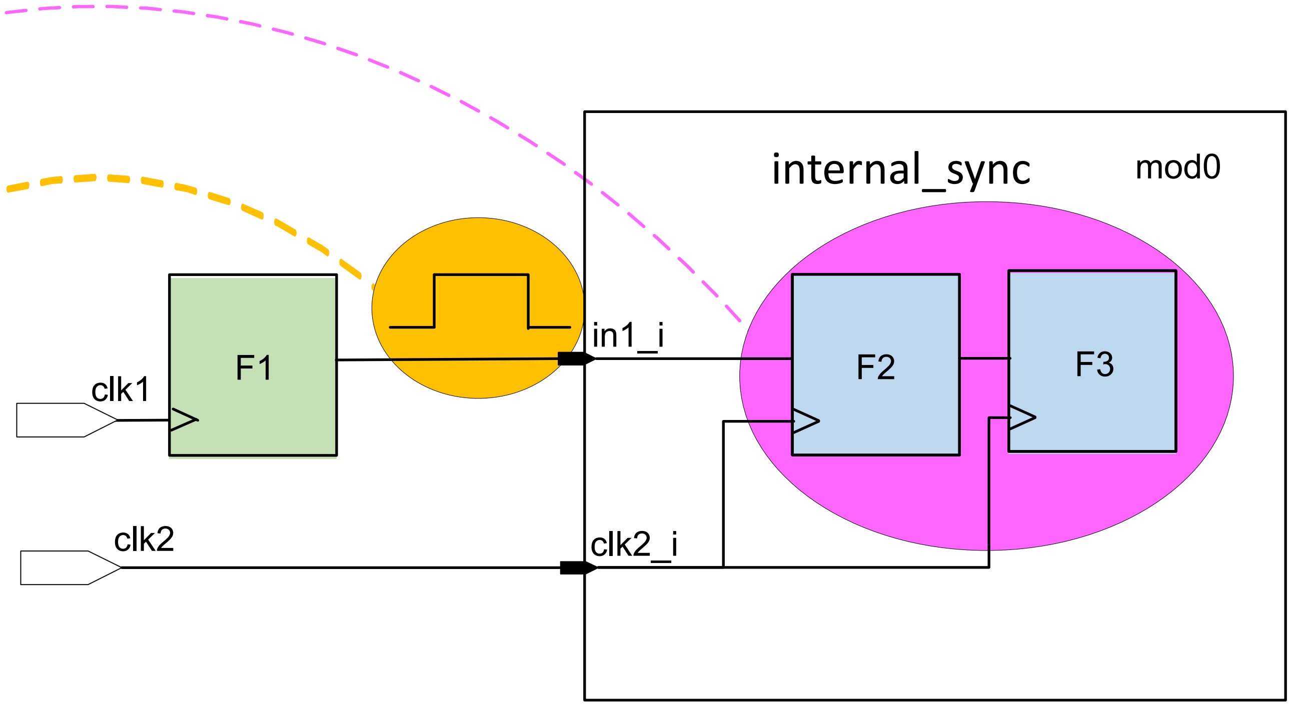
Correct Structure +

Correct Functionality

A Simple CDC Example

Correct structure:
There is a 2-DFF synchronizer between clock domains.

Correct functionality:
Pulse width of in1_i must be wide enough to be sampled by clk2_i.



Covered by Assertion

A Simple CDC Example: Pulse width check

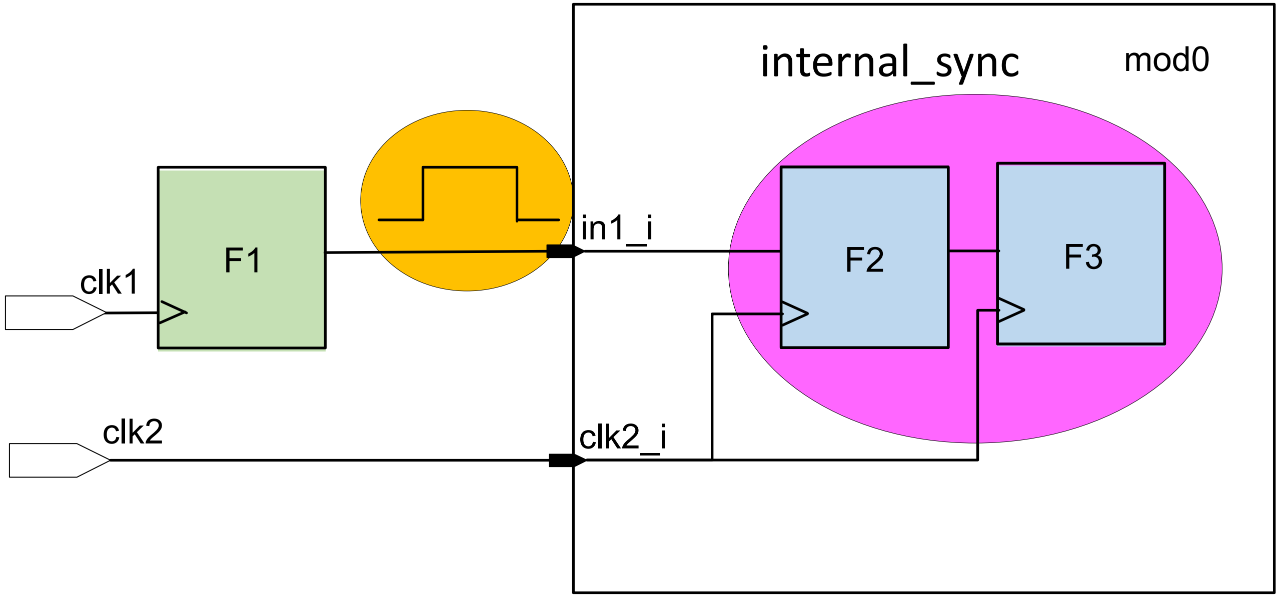
mod0’s collateral:

```
cdc_set_port in1_i                \
  -direction input                \
  -type data                      \
  -logic internal_sync            \
  -associated_to_clocks clk2_i
```

Assertion property generated from the information

Example:

```
property pulse_width;
  @(posedge clk2_i)
    $changed(in1_i) |=> $stable(in1_i)[*2];
endproperty
```



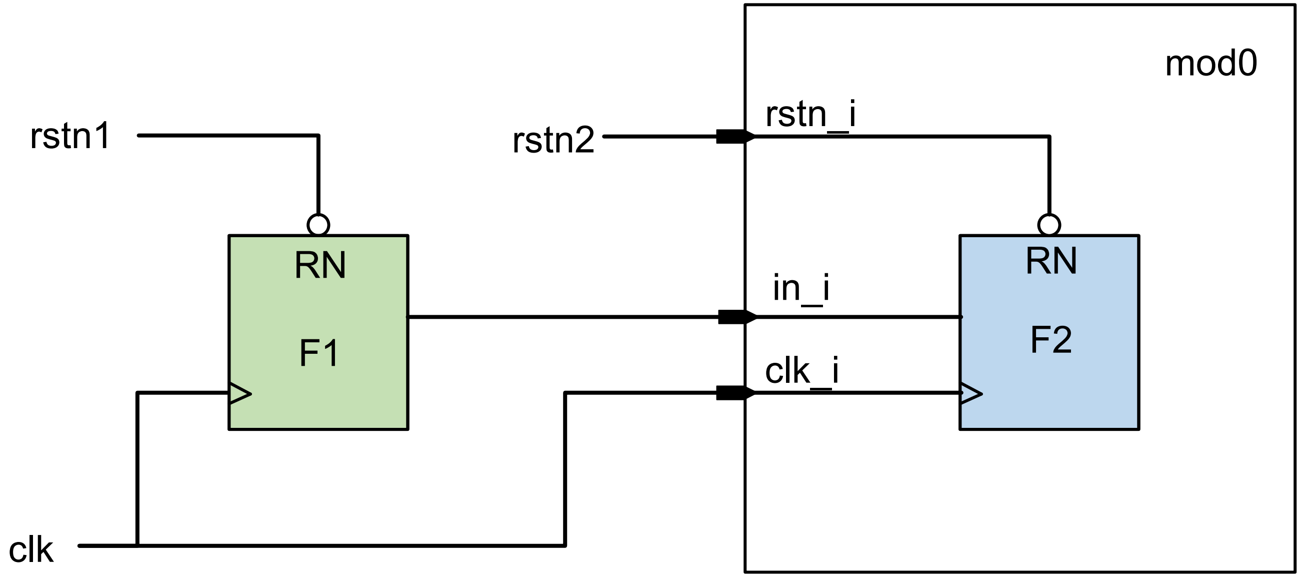
NOTE: The SVA here is just an example. It may vary in different EDA tools.

Reference:
Pragmatic Simulation-Based Verification of Clock Domain Crossing Signals and Jitter using SystemVerilog Assertions, Mark Litterick, Verilab, Munich, Germany

A Simple RDC Example

Structure:
mod0 doesn’t provide any RDC handling.

Correct Functionality:
rstn2 must be already 0 or going to 0 when rstn1 is going to 0.

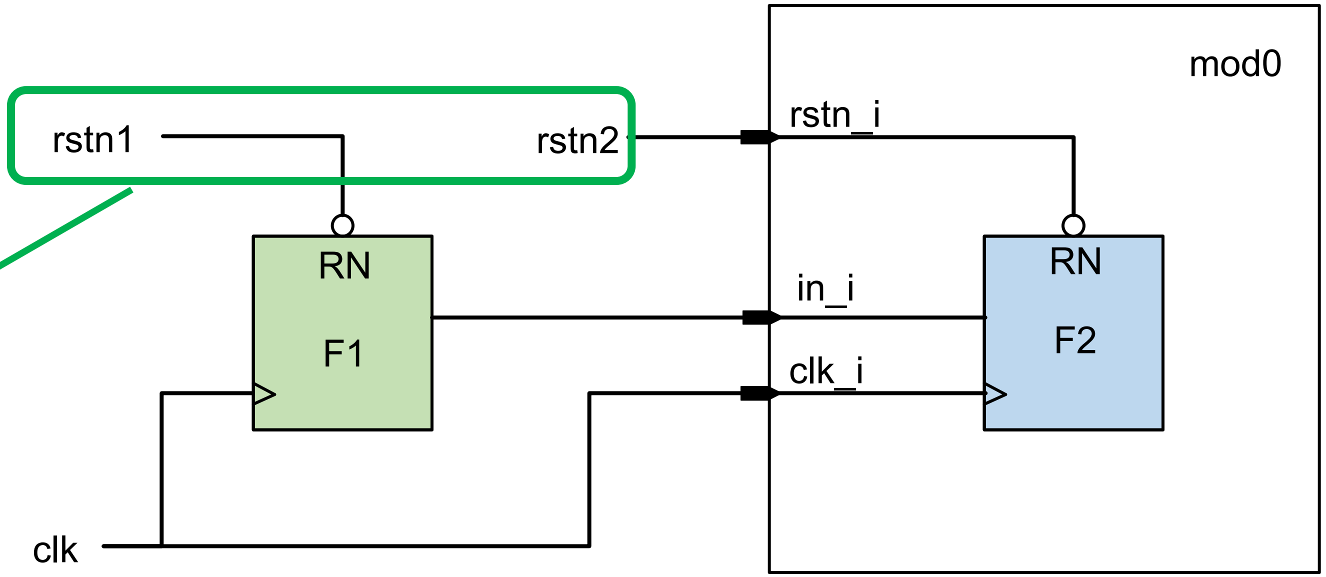


A Simple RDC Example: Reset sequence

mod0’s collateral:

```
cdc_set_port in_i                \
  -direction input               \
  -type data                     \
  -associated to clocks clk i    \
  -associated_to_reset rstn_i
```

NOTE: The SVA here is just an example. It may vary in different EDA tools.



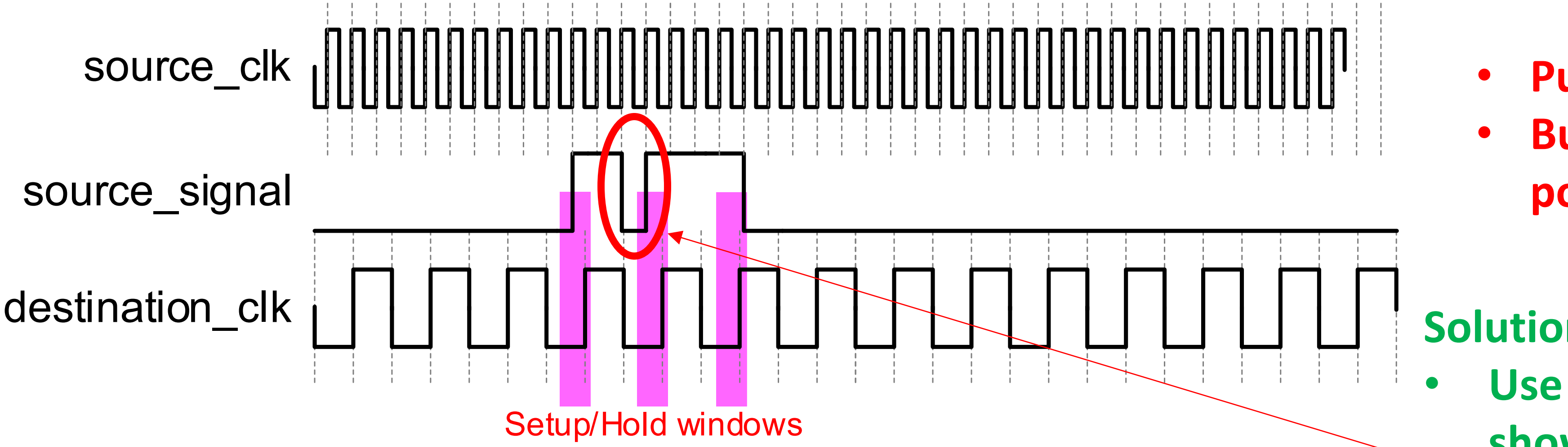
Assertion property generated from the information

Example:

```
property reset_order;
  @(negedge rstn1)
    (rstn2 === 1’b0);
endproperty
```

```
property reset_order_sync;
 @(posedge clk)
    $fell(rstn1) |-> (rstn2 === 1’b0);
endproperty
```

Assertion Clocking Concern



- **Pulse width assertion pass**
- **But silicon fail as it is a false positive in RTL for this example**

Solution:

- **Use fastest clock in the system shown on next slide**

Do not use this property as this misses the glitch on source_signal

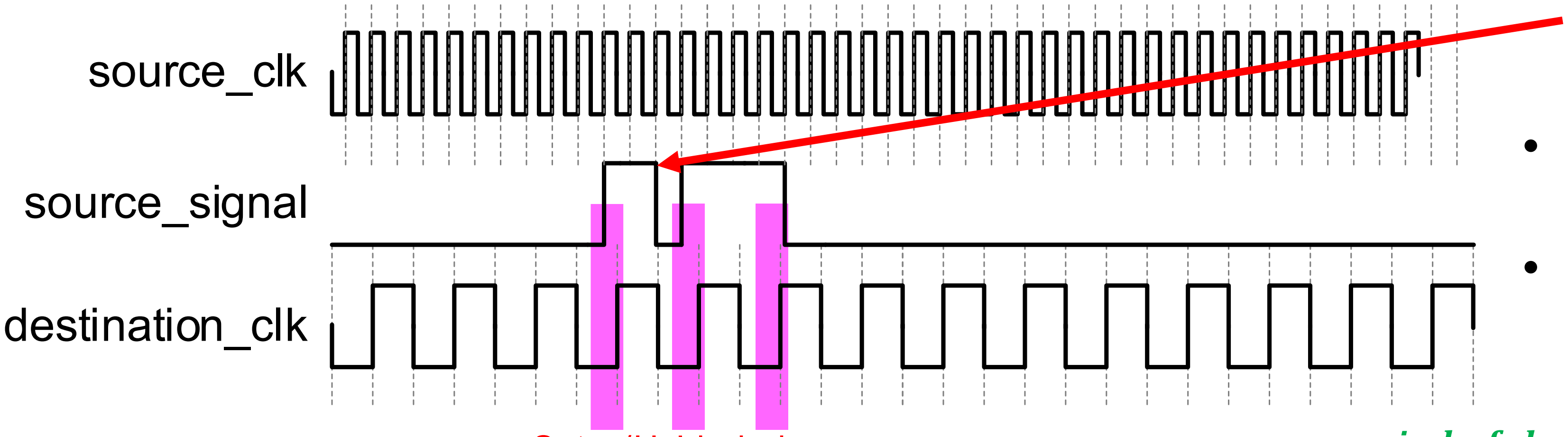
```
property pulse_width;
  @(posedge destination_clk)
    $changed(source_signal) |=> $stable(source_signal)[*2]
endproperty
```

NOTE: The SVA here is just an example. It may vary in different EDA tools.

Assertion Clocking Concern – Solution

Solution:

- **Use fastest clock in the system**



Setup/Hold windows

- **Pulse width assertion fail**

- **Source_clk is the fastest clock in this example.**
- **We can create a virtual faster clock depending on need.**

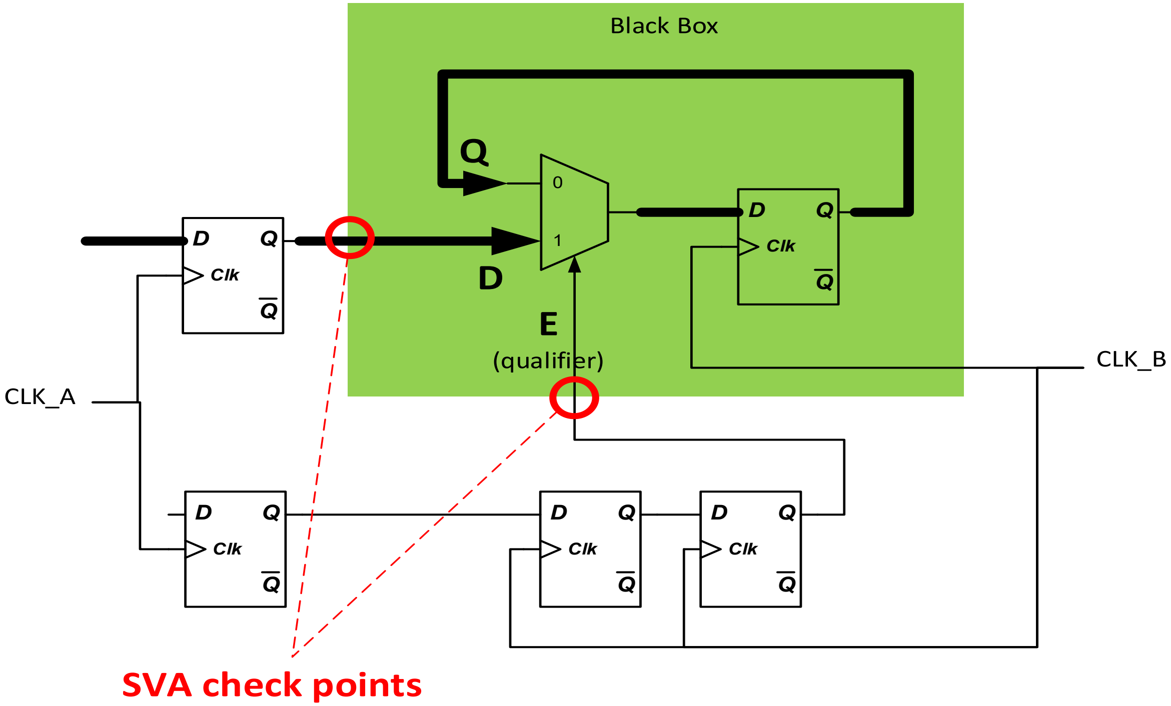
$$\mathbf{N = ceil}[2 * ({}^{period\ of\ destination\_clk}/_{period\ of\ fast\_clk})]$$

```
property pulse_width(fast_clk,source_signal,N);
  @(posedge fast_clk)
    $changed(source_signal) |=> $stable(source_signal)[*N]
endproperty
```

NOTE: The SVA here is just an example. It may vary in different EDA tools.

SVA limitation: Black Box Complexity

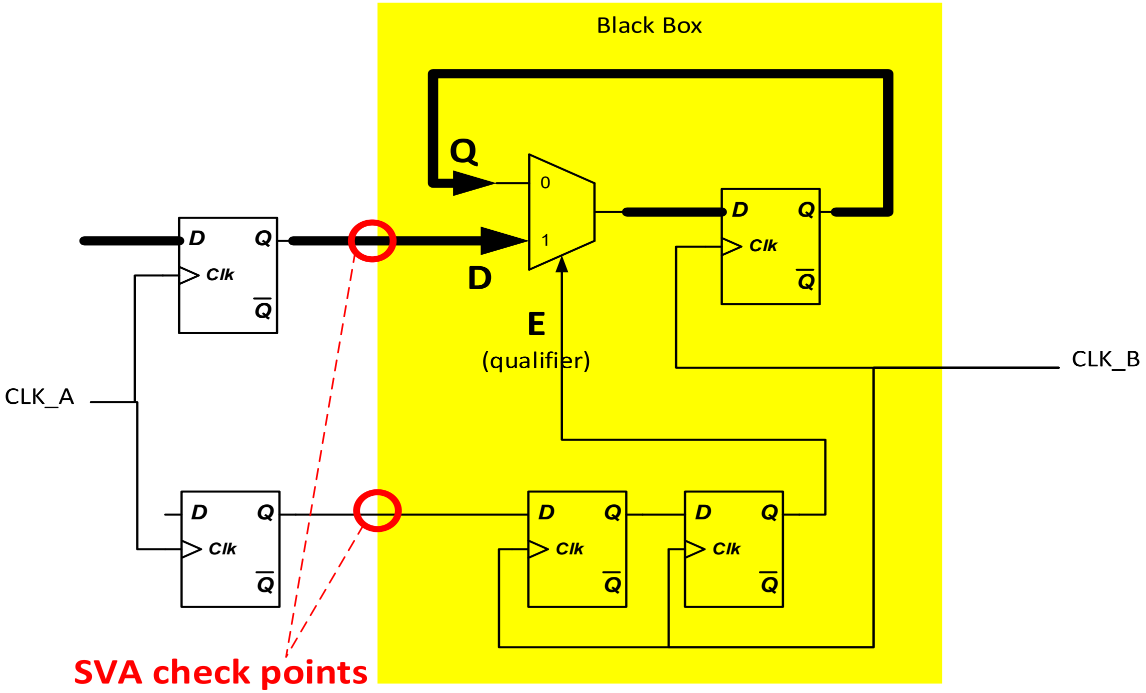
The assertion is applied at the black box boundary, leading to complexity in some cases



SVA check points

Less complexity in this scenario:

1. Signal path delay due to physical implementation

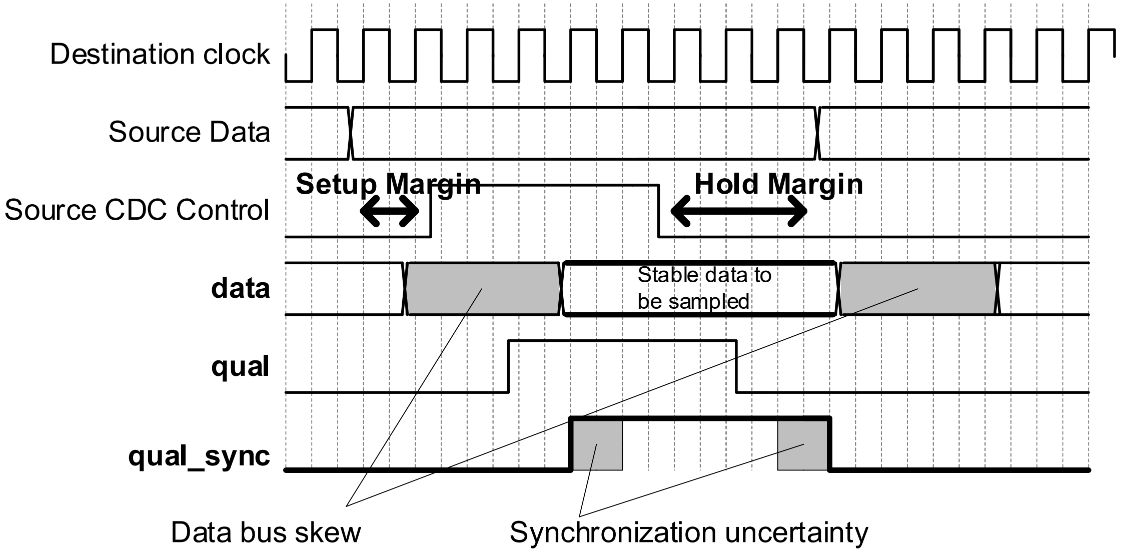


SVA check points

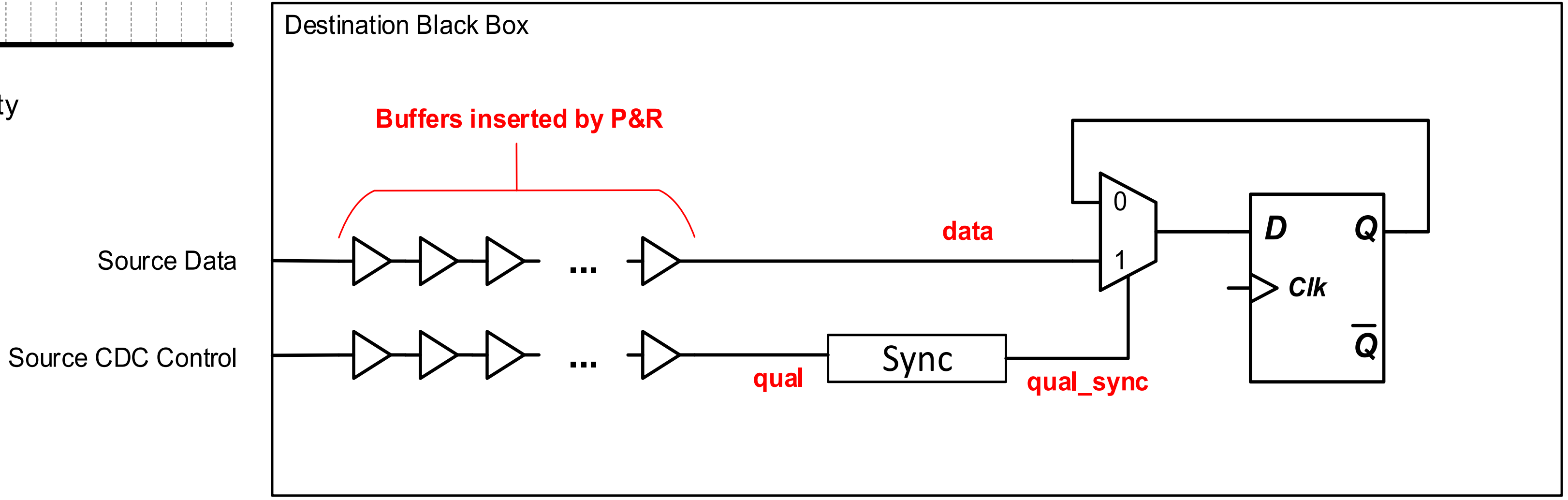
Complexity in this scenario:

1. We might not know the synchronizer’s structure since it is in the black box:
   a. Number of DFFs
   b. Active clock edges of each DFF
2. Signal path delay due to physical implementation

SVA limitation: Physical Implementation

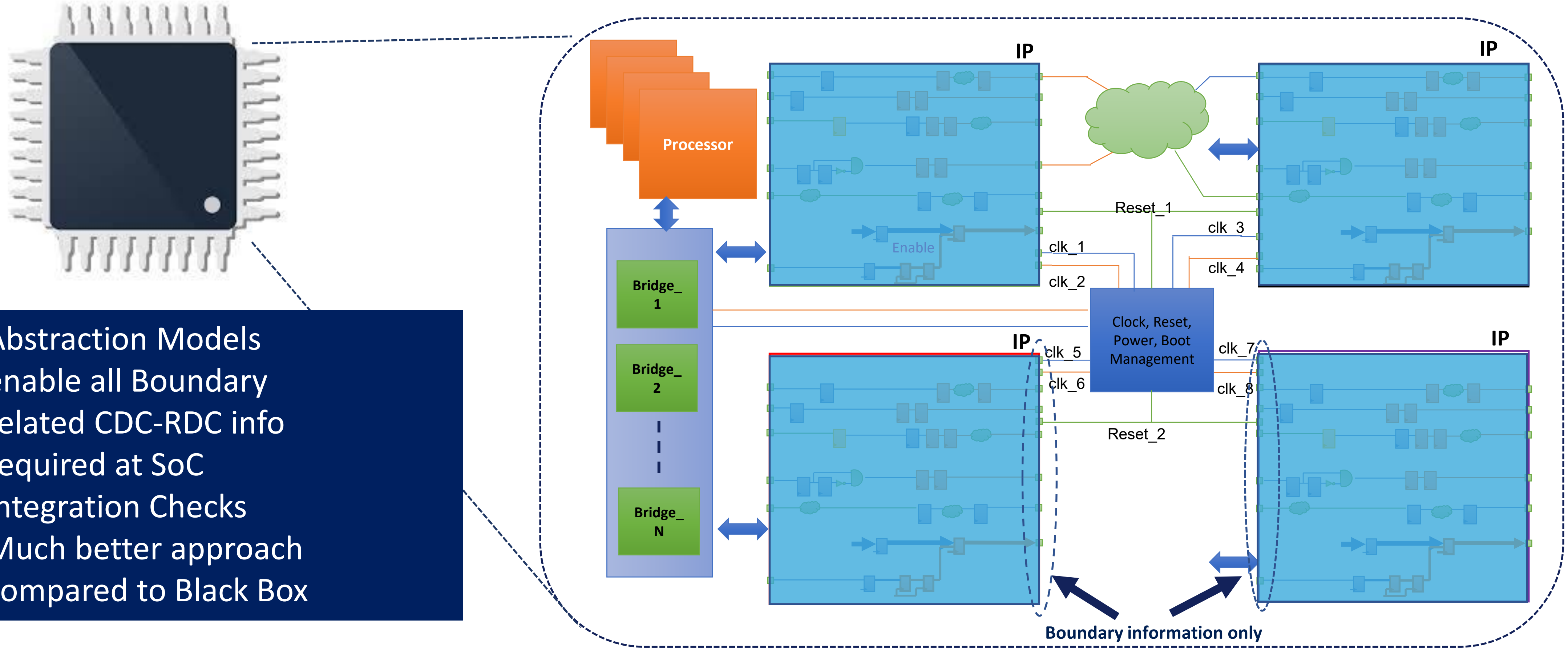


Failed silicon if we don't consider physical implementation up-front!



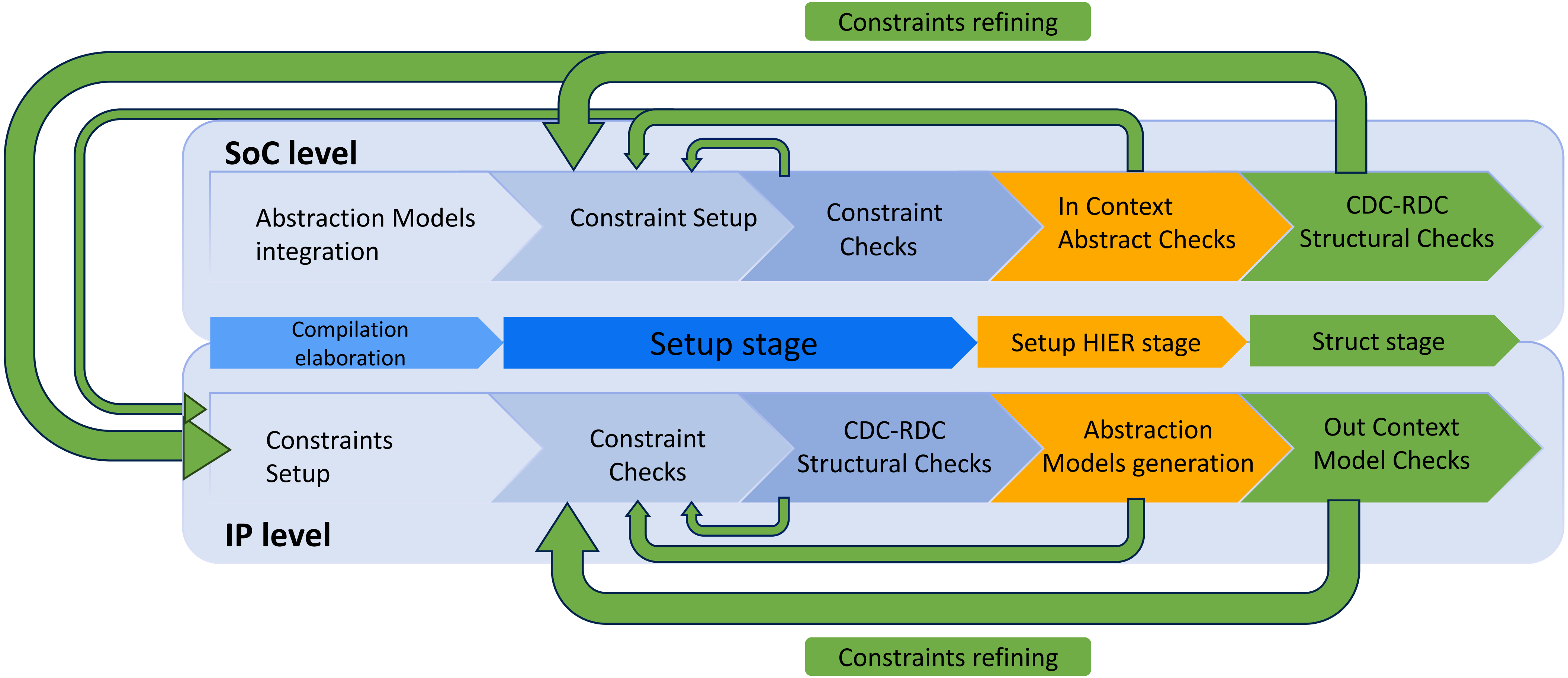
1.5 Hierarchical CDC/RDC

CDC-RDC Hierarchical Flow



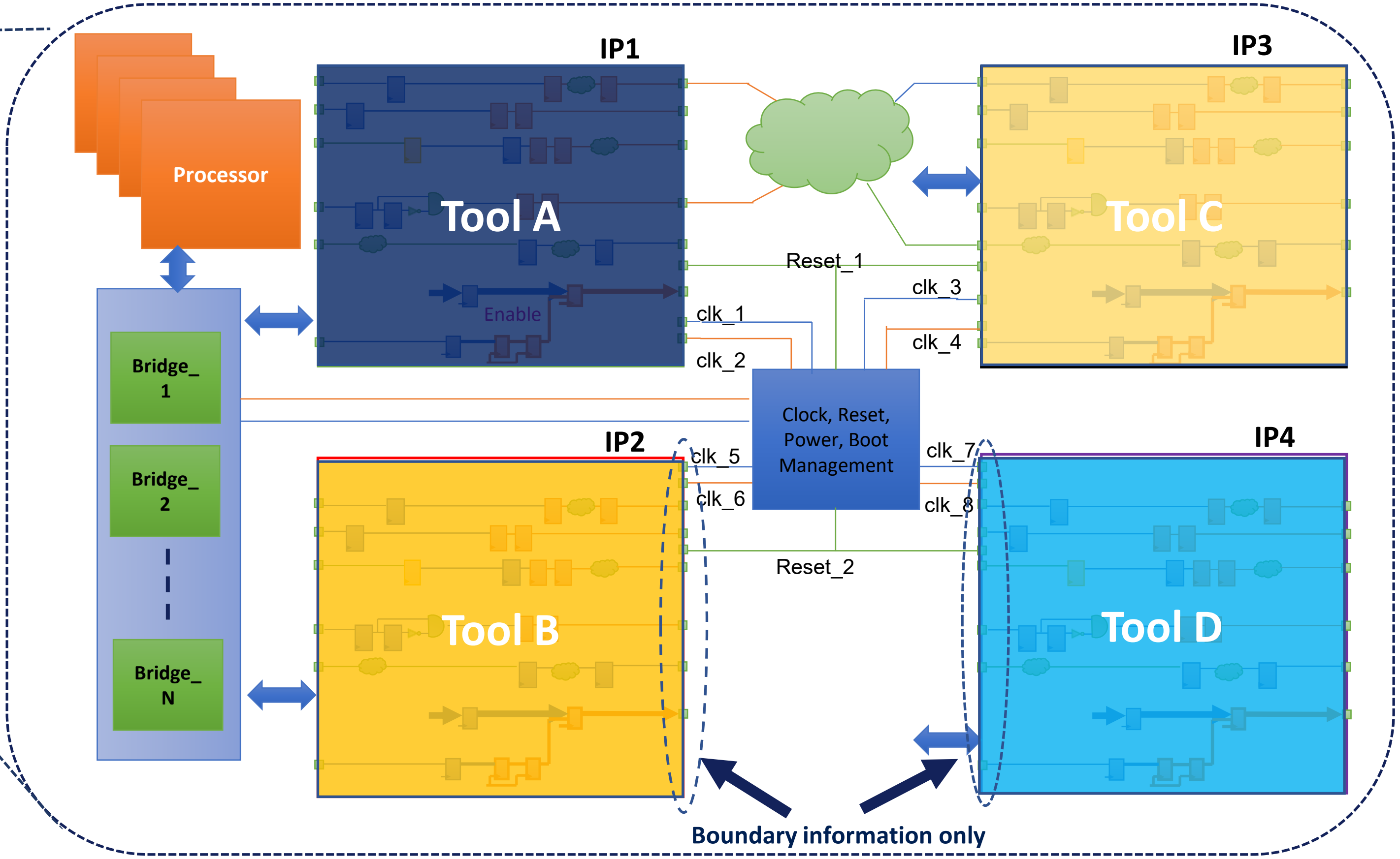
- Abstraction Models enable all Boundary related CDC-RDC info required at SoC integration Checks
- Much better approach compared to Black Box

CDC-RDC Hierarchical Flow



Hierarchical Model Standardization

- CDC models are currently lacking standardization
- CDC models from different tools are not compatible



2.1 Accellera CDC Working Group

Accellera CDC Working Group

- Presentation
- The five sub working groups
- Call for contribution

What was the problem?

As we move from monolithic designs … to IP/SOC with IPs sourced from a small/select providers … to sourcing IPs globally (to create differentiated products) …

We must maintain quality as we drive faster **time-to-market**

In areas where we have standards (SystemVerilog, OVM/UVM, LP/UPF), the integration is able to meet the above (**quality, speed**)

But in areas where we don't have standards (in this case, CDC), most options trade-off either quality, or time-to-market, or both :-(

Creating a standard for inter-operable collateral addresses this gap

Accellera CDC WG initiative

Pre-WG launched Sep ‘22 to evaluate need. WG launched Jan ’23

154 members from 24 companies (as of Sept 23 ‘25)

5 active sub-groups:

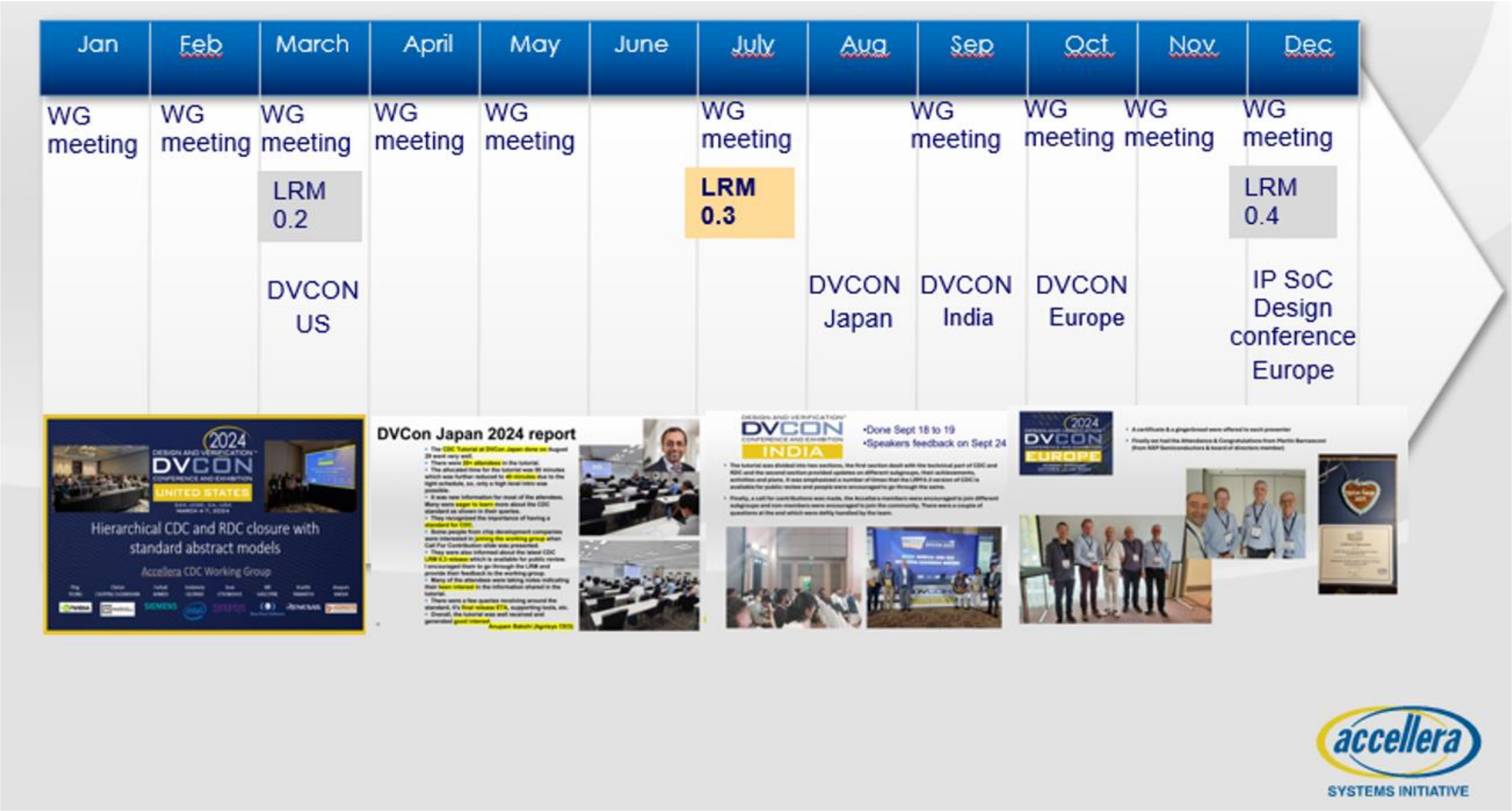
Output-Collateral, Format, Assertions, Testing, Training

V0.5 available for public review in April 2025

Ver	Focus	Timeline
v0.1	CDC	Oct 2023
v0.3	RDC & Assertions	July 2024
v0.5	Complexities & Extensions	April 2025
v1.0	Final LRM release	Nov 2025

Agnisys	AMD	Analog Devices	Apple	ARM	Arteris	Blue Pearl Solutions	Cadence
Google	Huawei	IBM	Infineon	Intel	Marvell	Microsoft	NVIDIA
NXP	Qualcomm	Renesas	Robert Bosch	Samsung	Siemens EDA	ST Microelectronics	Synopsys

Achievements 2024



Jan	Feb	March	April	May	June	July	Aug	Sep	Oct	Nov	Dec
WG meeting	WG meeting	WG meeting	WG meeting	WG meeting		WG meeting		WG meeting	WG meeting	WG meeting	WG meeting
		LRM 0.2				**LRM 0.3**					LRM 0.4
		DVCON US					DVCON Japan	DVCON India	DVCON Europe		IP SoC Design conference Europe

Hierarchical CDC and RDC closure with standard abstract models

Accellera CDC Working Group

DVCon Japan 2024 report

- The CDC Tutorial at DVCon Japan done on August 29 went very well.
- There were 20+ attendees in the tutorial.
- The allocated time for the tutorial was 90 minutes which was further reduced to 40 minutes due to the tight schedule, so, only a high level intro was possible.
- It was new information for most of the attendees. Many were eager to learn more about the CDC standard as shown in their queries.
- They recognized the importance of having a standard for CDC.
- Some people from chip development companies were interested in joining the working group when Call For Contribution slide was presented.
- They were also informed about the latest CDC LRM 0.3 release which is available for public review. I encouraged them to go through the LRM and provide their feedback to the working group.
- Many of the attendees were taking notes indicating their keen interest in the information shared in the tutorial.
- There were a few queries revolving around the standard, it's final release ETA, supporting tools, etc.
- Overall, the tutorial was well received and generated good interest.

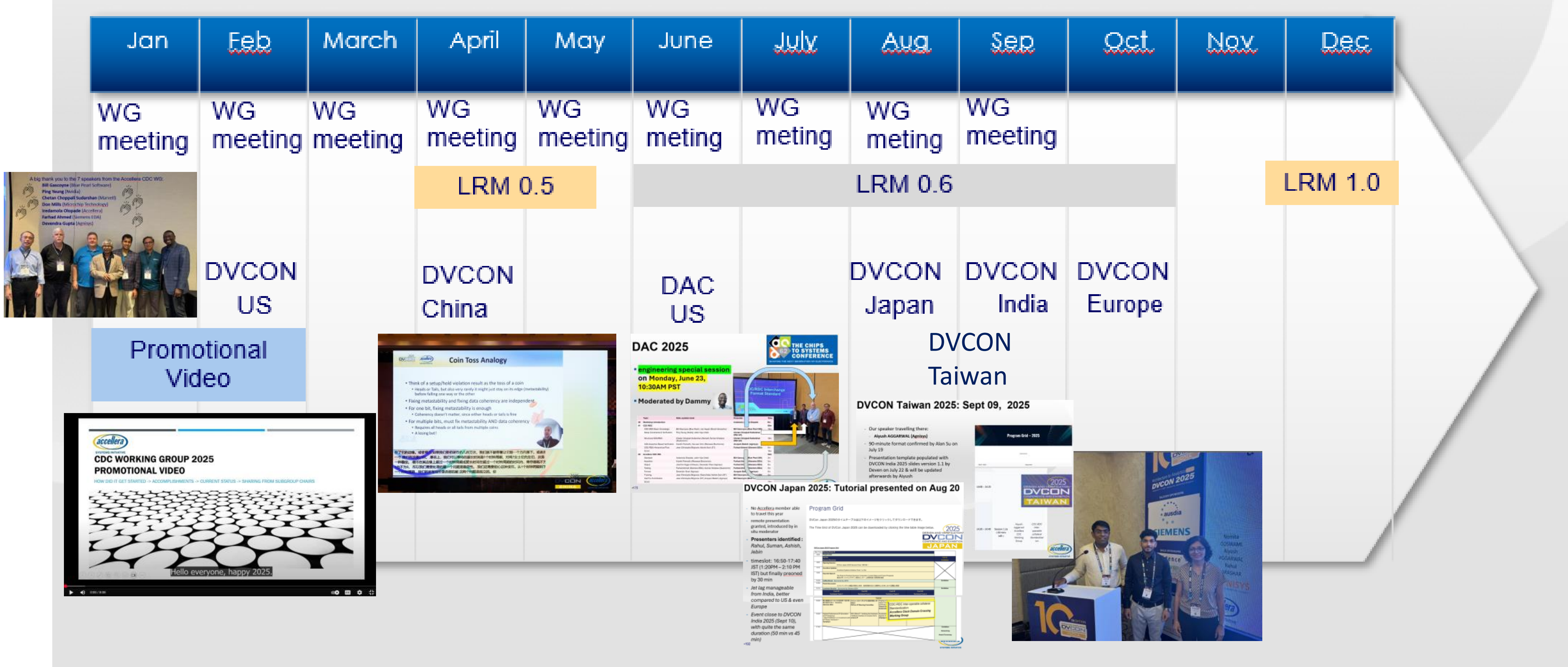
Anupam Bakshi (Agnisys CEO)

•Done Sept 18 to 19
•Speakers feedback on Sept 24

- The tutorial was divided into two sections, the first section dealt with the technical part of CDC and RDC and the second section provided updates on different subgroups, their achievements, activities and plans. It was emphasized a number of times that the LRM 0.3 version of CDC is available for public review and people were encouraged to go through the same.
- Finally, a call for contributions was made, the Accellera members were encouraged to join different subgroups and non-members were encouraged to join the community. There were a couple of questions at the end which were deftly handled by the team.

- A certificate & a gingerbread were offered to each presenter
- Finally we had the Attendance & Congratulations from Martin Barnasconi (from NXP Semiconductors & board of directors member)

Achievements 2025



A big thank you to the 7 speakers from the Accellera CDC WG:
Bill Gascoyne (Blue Pearl Software)
Ping Yeung (Nvidia)
Chetan Choppali Sudarshan (Marvell)
Don Mills (Microchip Technology)
Iredamola Olopade (Accellera)
Farhad Ahmed (Siemens EDA)
Devendra Gupta (Agnisys)

CDC WORKING GROUP 2025
PROMOTIONAL VIDEO
HOW DID IT GET STARTED -> ACCOMPLISHMENTS -> CURRENT STATUS -> SHARING FROM SUBGROUP CHAIRS
Hello everyone, happy 2025.

Coin Toss Analogy
- Think of a setup/hold violation result as the toss of a coin
  - Heads or Tails, but also very rarely it might just stay on its edge (metastability) before falling one way or the other
- Fixing metastability and fixing data coherency are independent
- For one bit, fixing metastability is enough
  - Coherency doesn't matter, since either heads or tails is fine
- For multiple bits, must fix metastability AND data coherency
  - Requires all heads or all tails from multiple coins
  - A losing bet!

DAC 2025
THE CHIPS TO SYSTEMS CONFERENCE
- engineering special session on Monday, June 23, 10:30AM PST
- Moderated by Dammy
CDC/RDC Interchange Format Standard

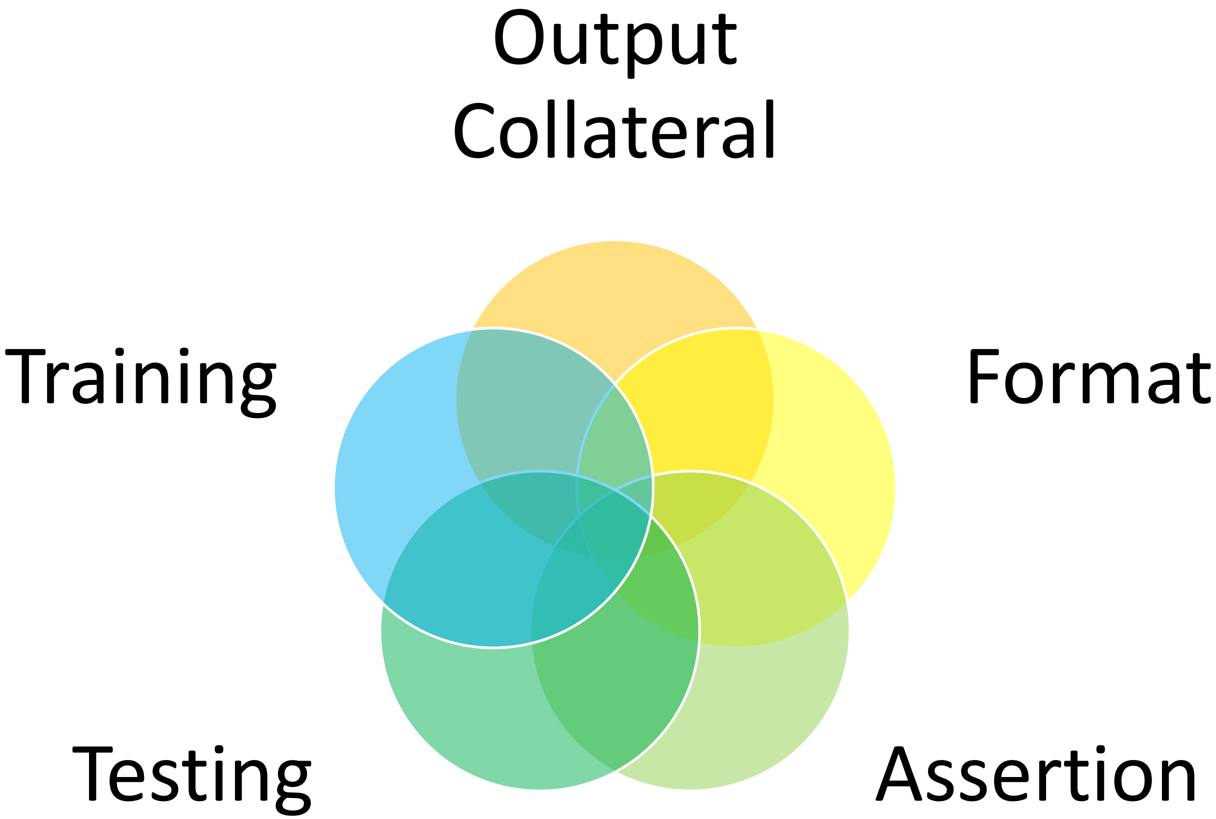
DVCON Japan 2025: Tutorial presented on Aug 20
- No Accellera member able to travel this year
- remote presentation granted, introduced by in situ moderator
- **Presenters identified :** *Rahul, Suman, Ashish, Jebin*
- timeslot: 16:50-17:40 JST (1:20PM – 2:10 PM IST) but finally preoned by 30 min
- *Jet lag manageable from India, better compared to US & even Europe*
- *Event close to DVCON India 2025 (Sept 10), with quite the same duration (50 min vs 45 min)*

Program Grid
DVCon Japan 2025のタイムテーブルは以下のイメージをクリックしてダウンロードできます。
The Time Grid of DVCon Japan 2025 can be downloaded by clicking the time table image below.
CDC-RDC inter-operable collateral Standardization
Accellera Clock Domain Crossing Working Group

DVCON Taiwan 2025: Sept 09, 2025
- Our speaker travelling there:
  - Aiyush AGGARWAL (Agnisys)
- 90-minute format confirmed by Alan Su on July 19
- Presentation template populated with DVCON India 2025 slides version 1.1 by Deven on July 22 & will be updated afterwards by Aiyush

Program Grid – 2025

The Five Sub Working Groups



Structure

- WG Leads / co-Leads
- Members

Meetings

- Leads / co-Leads monthly
- main WG monthly
- Sub WG weeklies

2.2 Assertion Subgroup

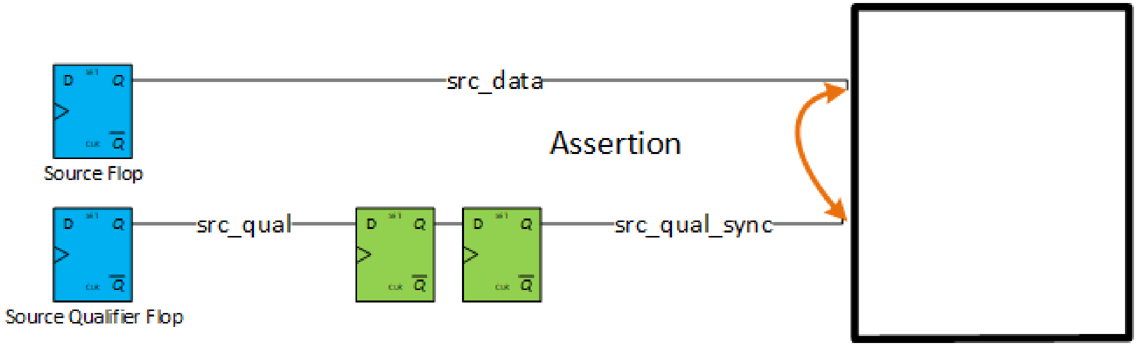
Assertion Subgroup Mission

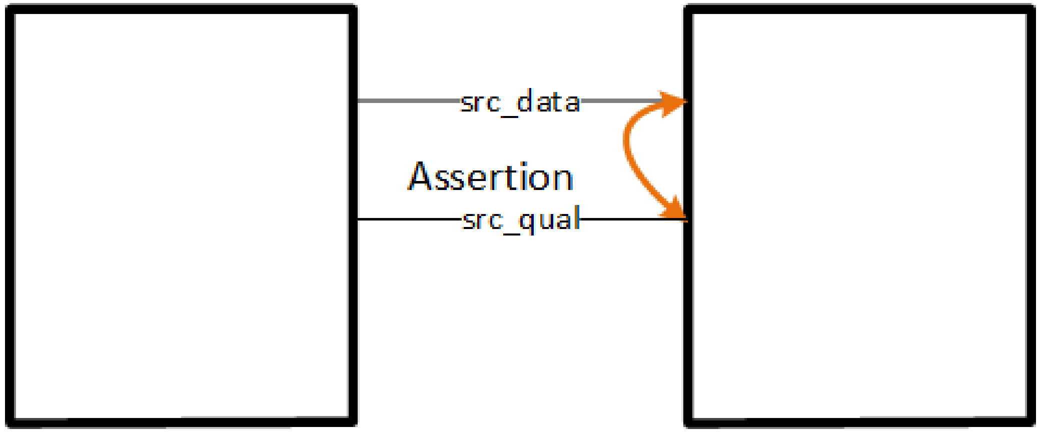
- Goal

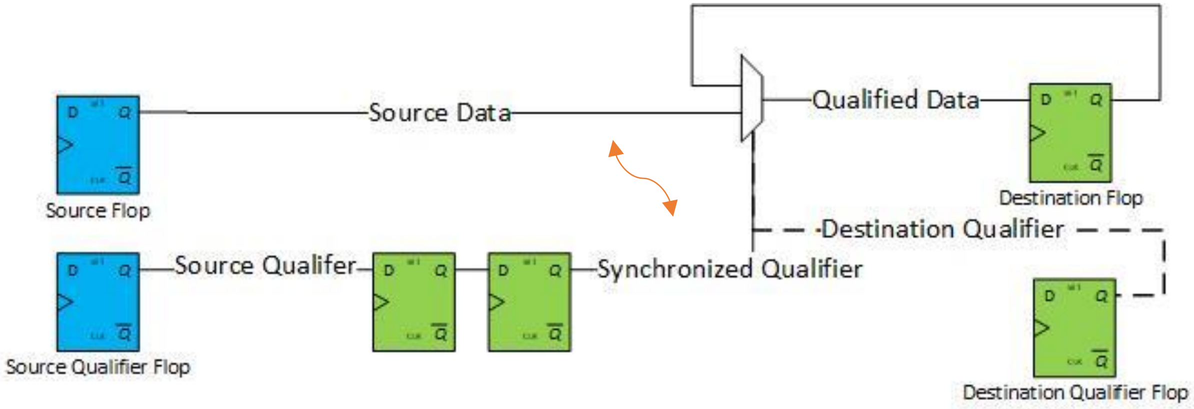
1. Produce Language Reference Manual (LRM) addendum for Assertions.
2. Enable all EDA vendors in developing tools that meet specification for generating System Verilog Assertions (SVA) along with collateral.
3. Enable Intellectual Property (IP) companies to generate SVA along with collateral using various vendors/tools.
4. Enable System On Chip (SOC) companies to consume generated SVA from any vendor/tool into their tool of choice.

Assertion Subgroup

- Integration Scenarios under consideration:
  - Blackbox IP to Blackbox IP at SOC level.
  - SOC level glue logic to Blackbox IP.
  - Blackbox to SOC level glue logic.

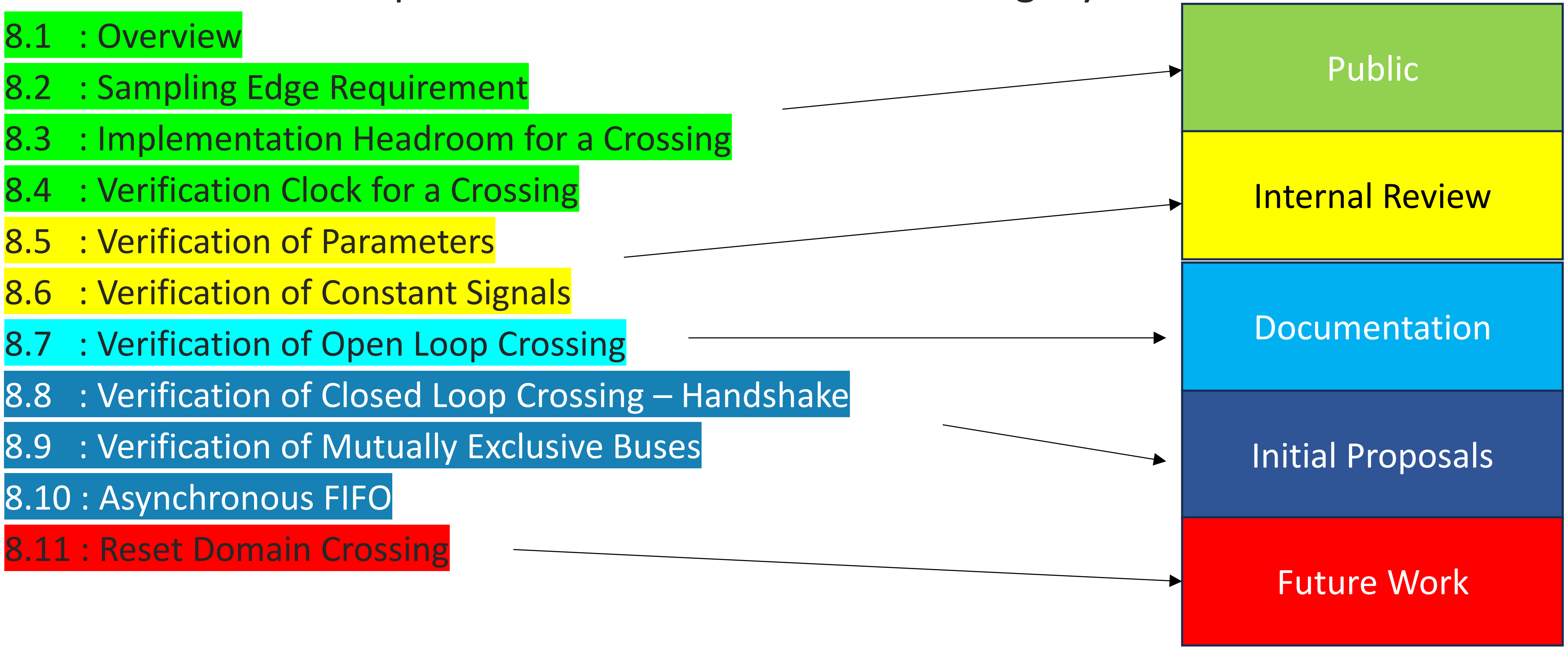






Assertion Subgroup

- LRM Clause 8 : SVA Requirements for black box CDC integrity verification



8.1 : Overview

8.2 : Sampling Edge Requirement

8.3 : Implementation Headroom for a Crossing

8.4 : Verification Clock for a Crossing

8.5 : Verification of Parameters

8.6 : Verification of Constant Signals

8.7 : Verification of Open Loop Crossing

8.8 : Verification of Closed Loop Crossing – Handshake

8.9 : Verification of Mutually Exclusive Buses

8.10 : Asynchronous FIFO

8.11 : Reset Domain Crossing

Public

Internal Review

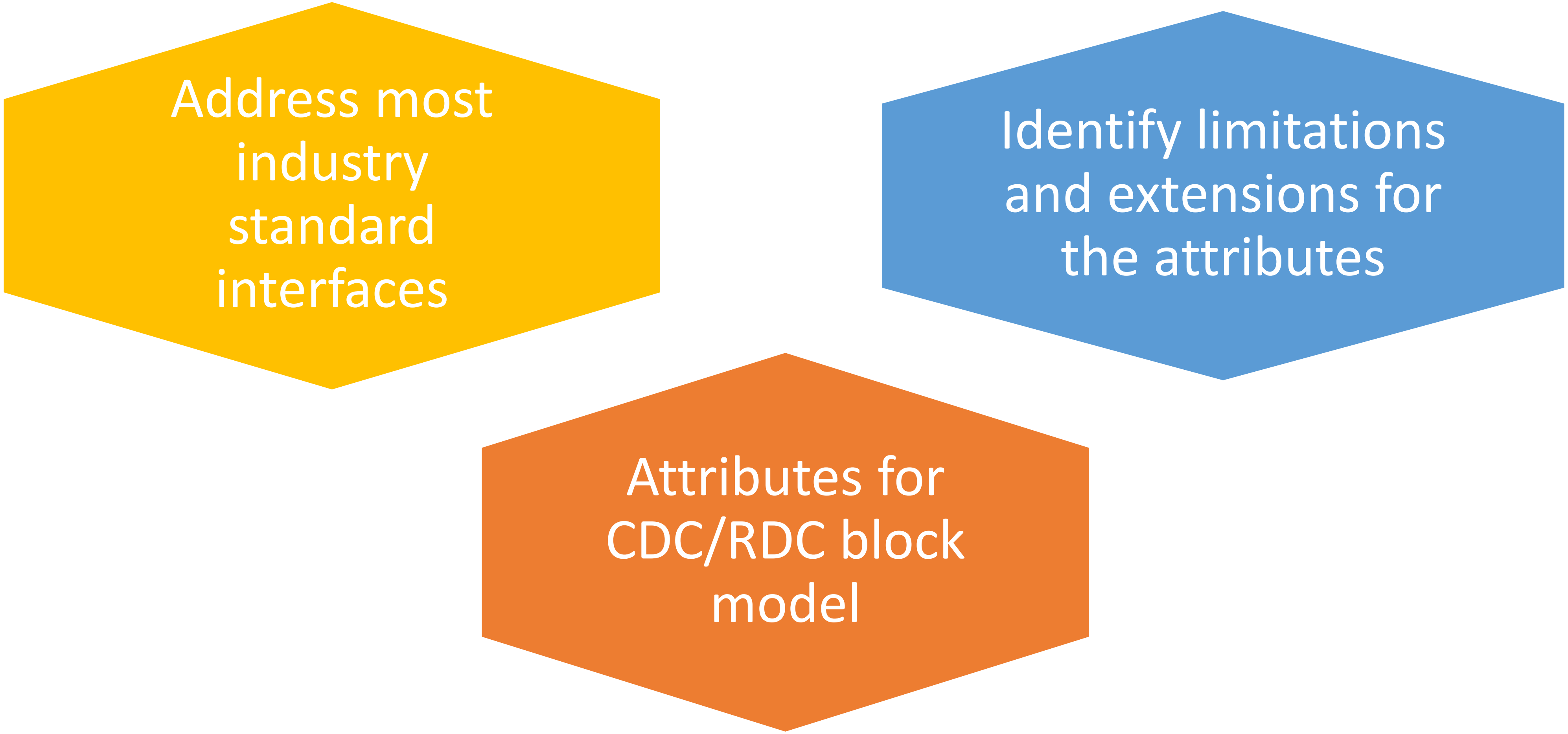
Documentation

Initial Proposals

Future Work

2.3 Output Collateral Subgroup

Output Collateral Subgroup



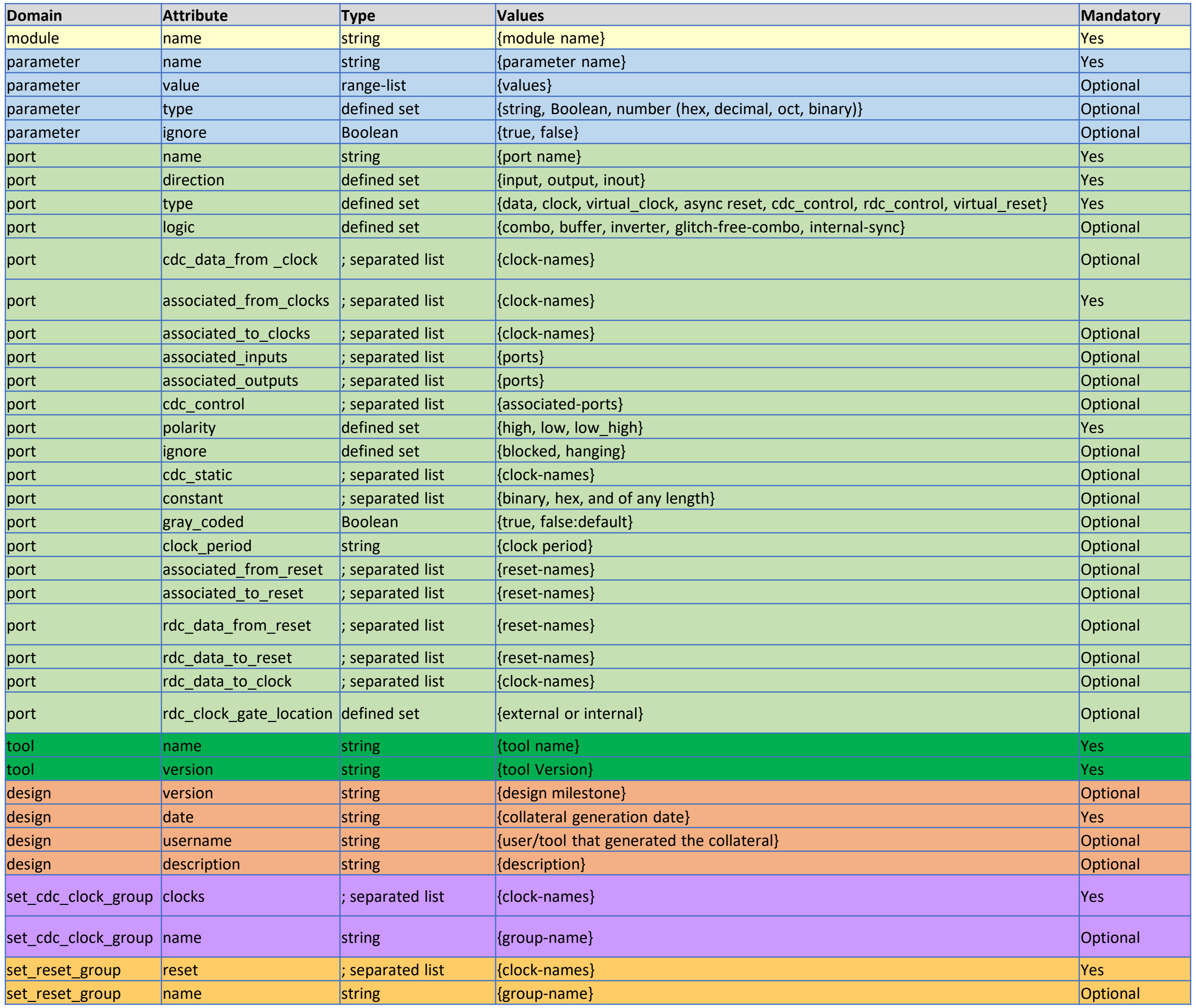
Address most industry standard interfaces

Identify limitations and extensions for the attributes

Attributes for CDC/RDC block model

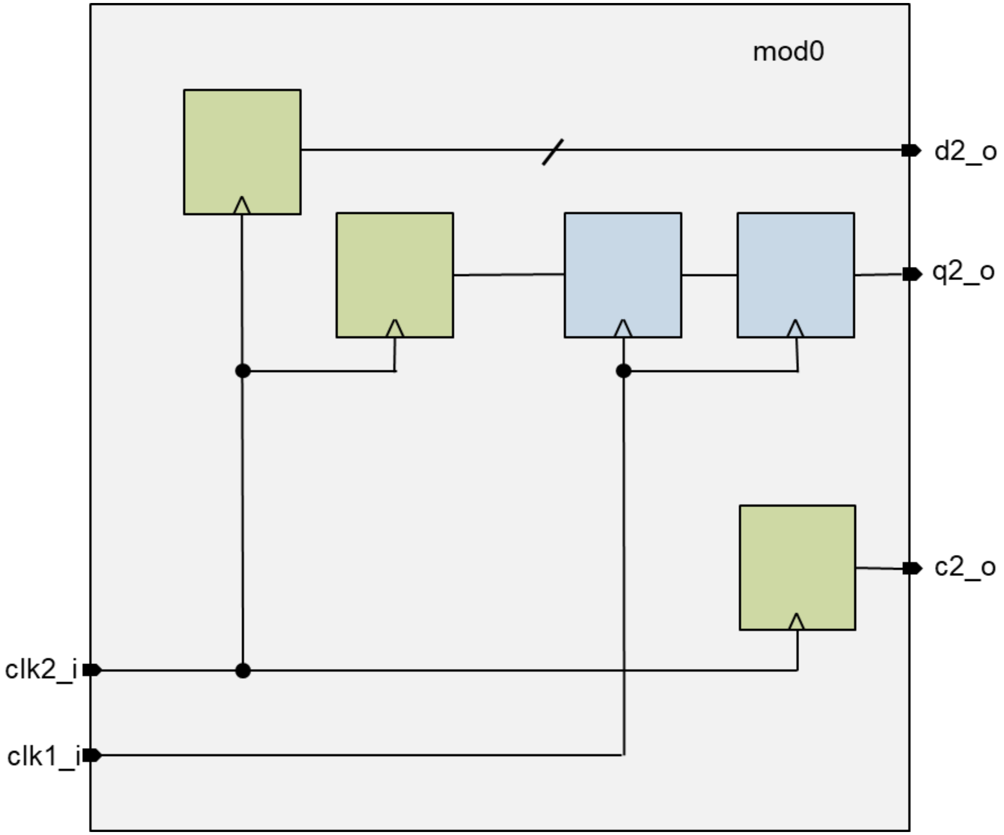
Attributes Table in LRM v0.5

- Attributes split into domains
  - Indicated by the color



Domain	Attribute	Type	Values	Mandatory
module	name	string	{module name}	Yes
parameter	name	string	{parameter name}	Yes
parameter	value	range-list	{values}	Optional
parameter	type	defined set	{string, Boolean, number (hex, decimal, oct, binary)}	Optional
parameter	ignore	Boolean	{true, false}	Optional
port	name	string	{port name}	Yes
port	direction	defined set	{input, output, inout}	Yes
port	type	defined set	{data, clock, virtual_clock, async reset, cdc_control, rdc_control, virtual_reset}	Yes
port	logic	defined set	{combo, buffer, inverter, glitch-free-combo, internal-sync}	Optional
port	cdc_data_from _clock	; separated list	{clock-names}	Optional
port	associated_from_clocks	; separated list	{clock-names}	Yes
port	associated_to_clocks	; separated list	{clock-names}	Optional
port	associated_inputs	; separated list	{ports}	Optional
port	associated_outputs	; separated list	{ports}	Optional
port	cdc_control	; separated list	{associated-ports}	Optional
port	polarity	defined set	{high, low, low_high}	Yes
port	ignore	defined set	{blocked, hanging}	Optional
port	cdc_static	; separated list	{clock-names}	Optional
port	constant	; separated list	{binary, hex, and of any length}	Optional
port	gray_coded	Boolean	{true, false:default}	Optional
port	clock_period	string	{clock period}	Optional
port	associated_from_reset	; separated list	{reset-names}	Optional
port	associated_to_reset	; separated list	{reset-names}	Optional
port	rdc_data_from_reset	; separated list	{reset-names}	Optional
port	rdc_data_to_reset	; separated list	{reset-names}	Optional
port	rdc_data_to_clock	; separated list	{clock-names}	Optional
port	rdc_clock_gate_location	defined set	{external or internal}	Optional
tool	name	string	{tool name}	Yes
tool	version	string	{tool Version}	Yes
design	version	string	{design milestone}	Optional
design	date	string	{collateral generation date}	Yes
design	username	string	{user/tool that generated the collateral}	Optional
design	description	string	{description}	Optional
set_cdc_clock_group	clocks	; separated list	{clock-names}	Yes
set_cdc_clock_group	name	string	{group-name}	Optional
set_reset_group	reset	; separated list	{clock-names}	Yes
set_reset_group	name	string	{group-name}	Optional

Port Attribute Modelling



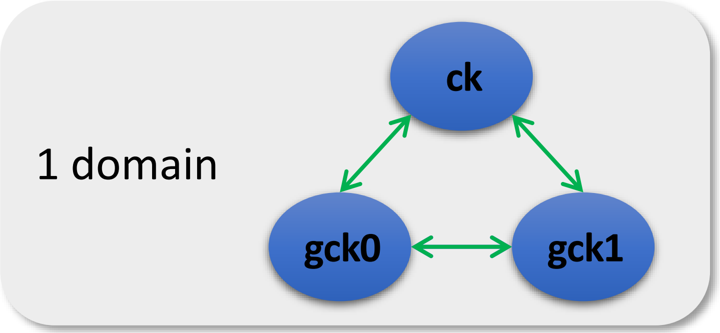
🟦 clk1_i clock domain

🟩 clk2_i clock domain

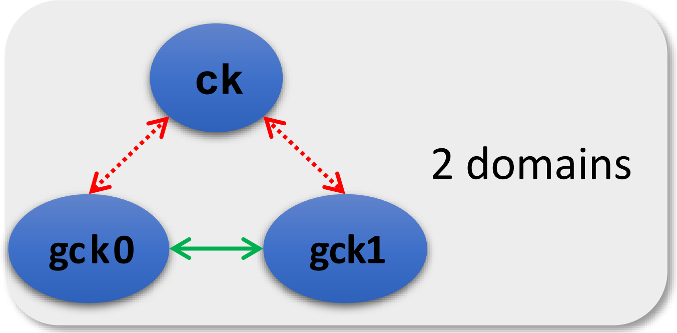
example in Tcl-format for output interface

```
cdc_set_module mod0

   cdc_set_port d2_o                          \
      -type                     data   \
      -direction                output \
      -associated_from_clocks clk2_i \
      -cdc_control              q2_o

   cdc_set_port q2_o                               \
      -type                     cdc_control \
      -direction                output      \
      -cdc_data_from_clock      clk2_i      \
      -associated_from_clock    clk1_i      \
      -associated_outputs       d2_o

   cdc_set_port c2_o                           \
      -type                     data    \
      -direction                output  \
      -associated_from_clock    clk2_i
```

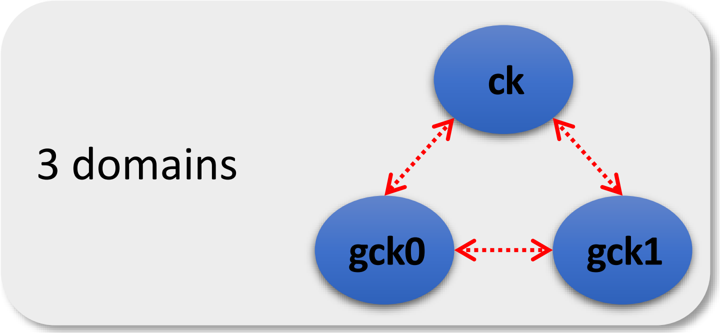
cdc_set_clock_group (Tcl format)



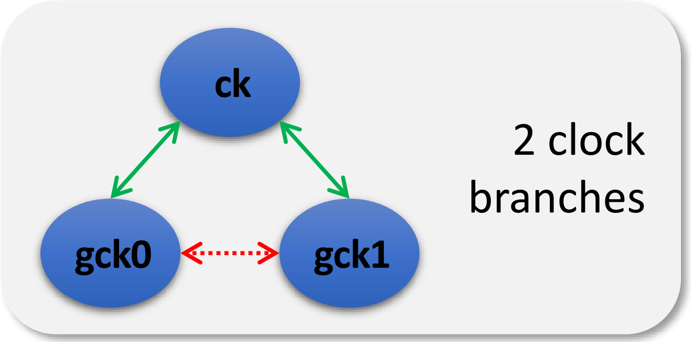
```
cdc_set_clock_group -name common_domain -clocks {ck gck0 gck1}
```



```
cdc_set_clock_group -name small_domain -clocks {ck}
cdc_set_clock_group -name large_domain -clocks {gck0 gck1}
```



```
cdc_set_clock_group -name domain_C -clocks {ck}
cdc_set_clock_group -name domain_0 -clocks {gck0}
cdc_set_clock_group -name domain_1 -clocks {gck1}
```



compatibility sets:
common members
allowed

```
cdc_set_clock_group -name left_branch   -clocks {ck gck0}
cdc_set_clock_group -name right_branch -clocks {ck gck1}
```

2.4 Testing Subgroup

Testing Subgroup Mission

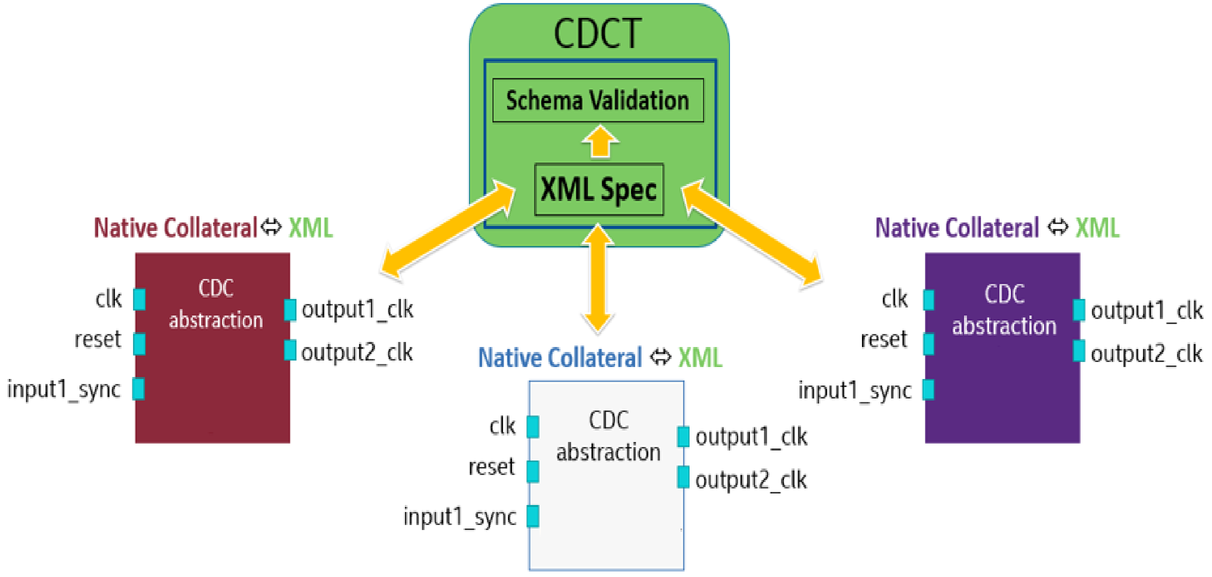
- Goal

1. **Evaluate** the set of Accellera CDC attributes and protocols for completeness using multiple tools from multiple vendors.
2. **Demonstrate** the use of the complete set of attributes and protocols as defined and formatted by other sub-groups.
3. **Provide RTL design examples** within which the defined attributes and protocols can be further qualified and evaluated
    - Review small examples provided in the latest LRM to create RTL test cases
    - Analyze the RTL test cases using various EDA tools
4. **Make the test cases available** for EDA vendors as first level QA testing

2.5 Format Subgroup

Format Subgroup Mission

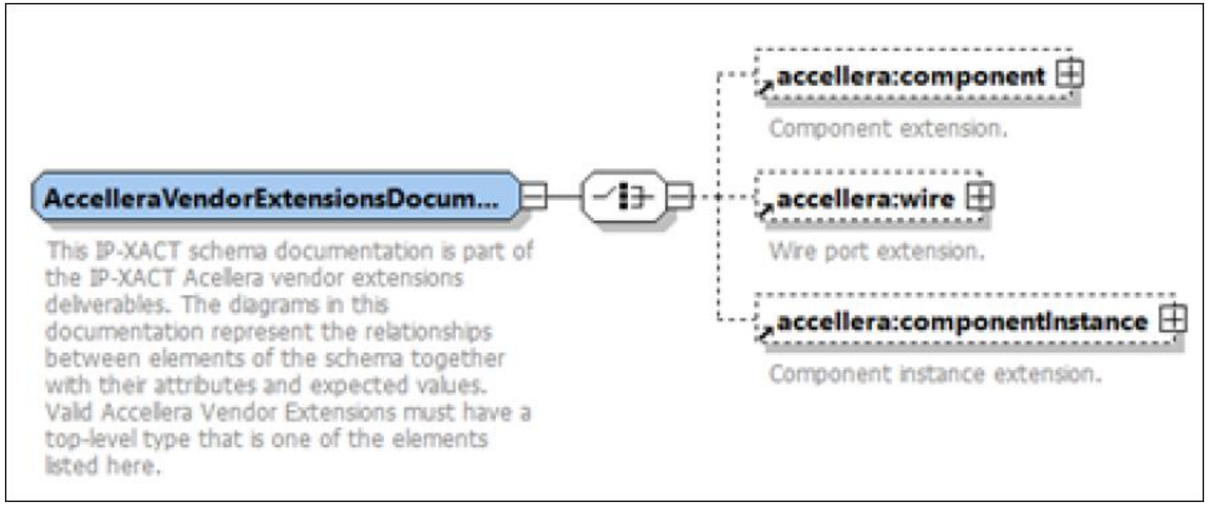
- **Goal:**
  - Determine exact format for domain specific language to capture the required attributes/data from input/output collaterals
- **Methodology:**
  - Evaluated different options like Excel, IP-XACT, TCL, JSON, etc.
  - Experimented with populating the formats to ascertain the ability to meet the requirement
  - Determined pros and cons for each option of format
  - The format should support easy translation to the formats of different EDA tools and vice-versa



- **Outcome:** **CDC Workgroup voted for a combination of IP-XACT and TCL as the chosen format for CDC**

IP-XACT Format for CDC (1/4)

- The IP-XACT standard already captures some attributes related to clock and reset
- IP-XACT allows extending the standard using vendor extensions
- Vendor extensions for CDC are defined as Accellera Vendor extensions at different elements in the design hierarchy
- Top level elements for the Accellera vendor extensions for CDC are:
  - accellera:component
  - accellera:wire
  - accellera:componentInstance



This IP-XACT schema documentation is part of the IP-XACT Accellera vendor extensions deliverables. The diagrams in this documentation represent the relationships between elements of the schema together with their attributes and expected values. Valid Accellera Vendor Extensions must have a top-level type that is one of the elements listed here.

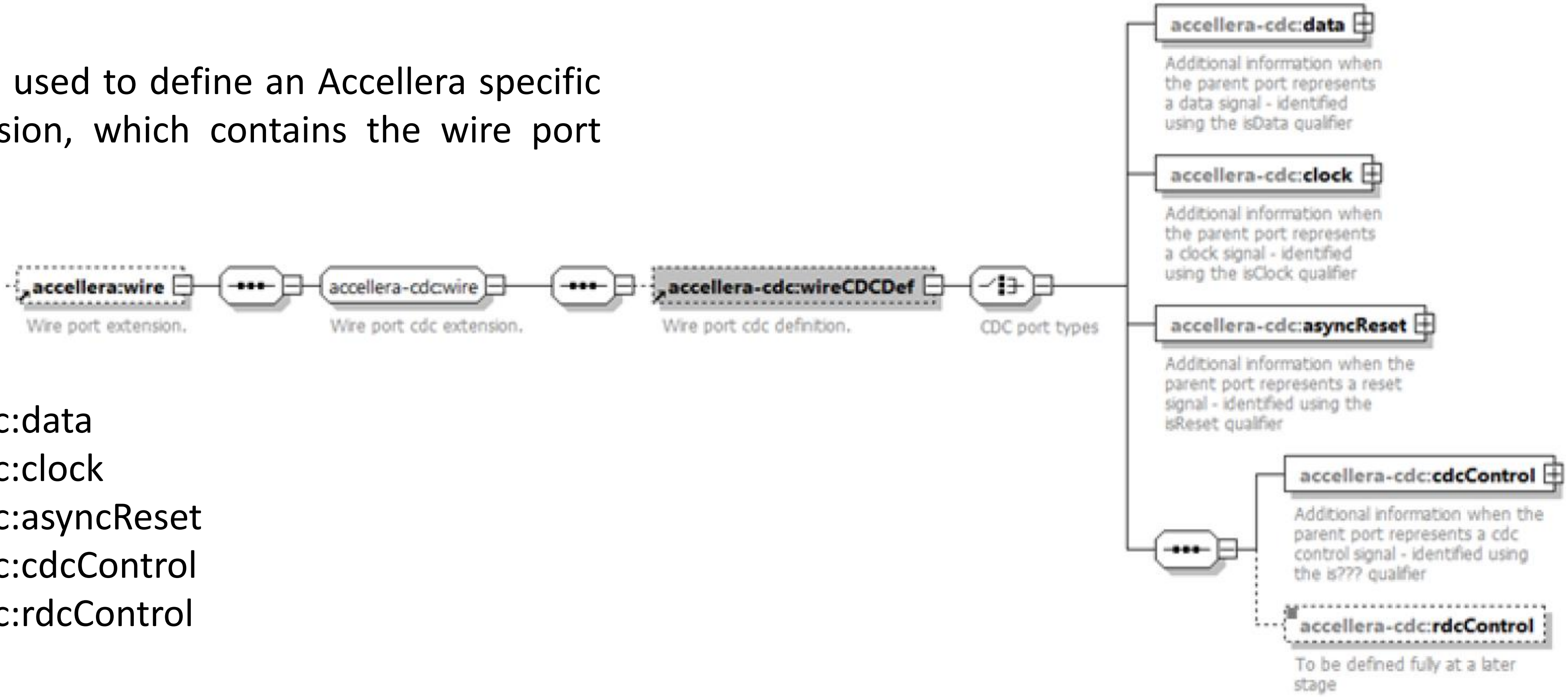
Component extension.

Wire port extension.

Component instance extension.

IP-XACT Format for CDC (2/4)

- accellera: wire is used to define an Accellera specific wire port extension, which contains the wire port CDC definition

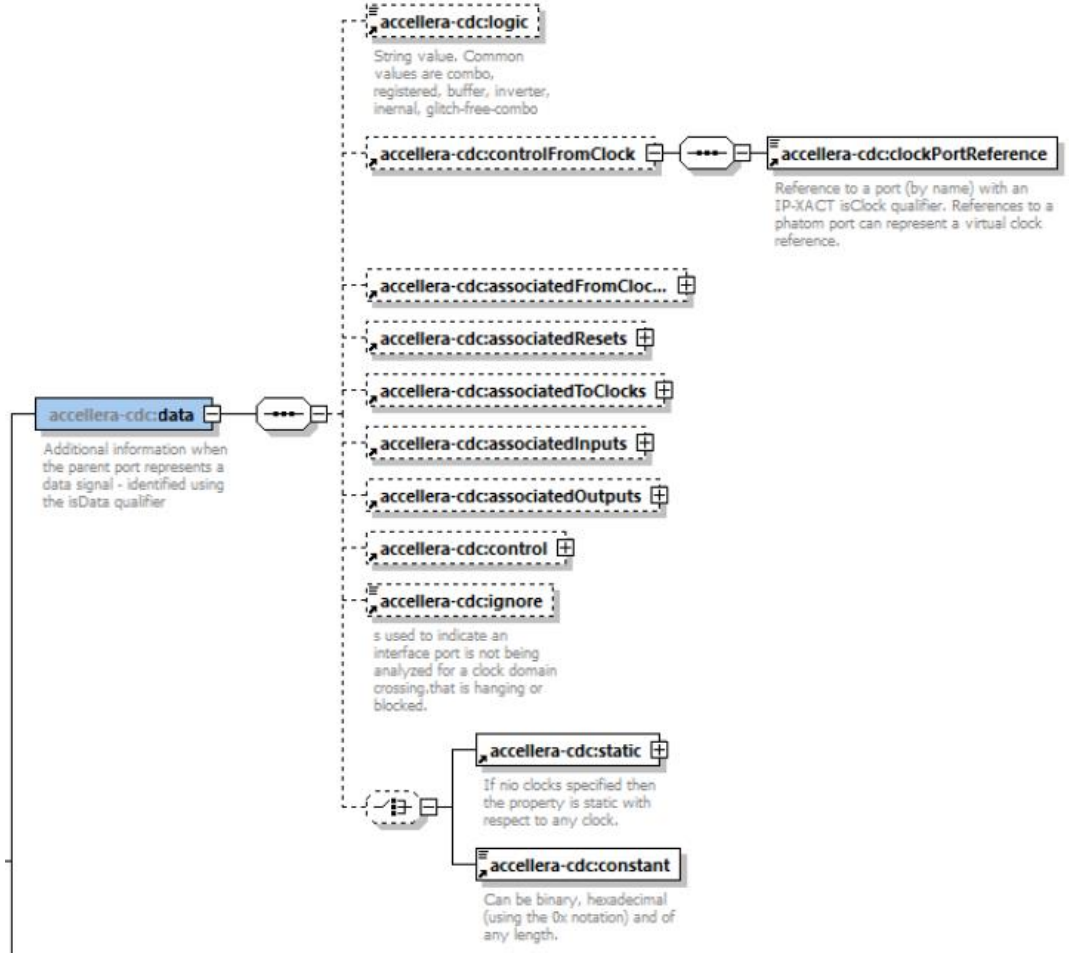

accellera:wire
Wire port extension.
accellera-cdc:wire
Wire port cdc extension.
accellera-cdc:wireCDCDef
Wire port cdc definition.
CDC port types
accellera-cdc:data
Additional information when the parent port represents a data signal - identified using the isData qualifier
accellera-cdc:clock
Additional information when the parent port represents a clock signal - identified using the isClock qualifier
accellera-cdc:asyncReset
Additional information when the parent port represents a reset signal - identified using the isReset qualifier
accellera-cdc:cdcControl
Additional information when the parent port represents a cdc control signal - identified using the is??? qualifier
accellera-cdc:rdcControl
To be defined fully at a later stage

- accellera-cdc:data
- accellera-cdc:clock
- accellera-cdc:asyncReset
- accellera-cdc:cdcControl
- accellera-cdc:rdcControl

IP-XACT Format for CDC (3/4)

- When a port represents a data signal, all attributes required for CDC are captured in this extension

- Similarly, the schema is defined for asyncReset, cdcControl, and rdcControl


accellera-cdc:data
accellera-cdc:logic
accellera-cdc:controlFromClock
accellera-cdc:clockPortReference
accellera-cdc:associatedFromCloc...
accellera-cdc:associatedResets
accellera-cdc:associatedToClocks
accellera-cdc:associatedInputs
accellera-cdc:associatedOutputs
accellera-cdc:control
accellera-cdc:ignore
accellera-cdc:static
accellera-cdc:constant

Additional information when the parent port represents a data signal - identified using the isData qualifier

String value. Common values are combo, registered, buffer, inverter, inernal, glitch-free-combo

Reference to a port (by name) with an IP-XACT isClock qualifier. References to a phatom port can represent a virtual clock reference.

s used to indicate an interface port is not being analyzed for a clock domain crossing.that is hanging or blocked.

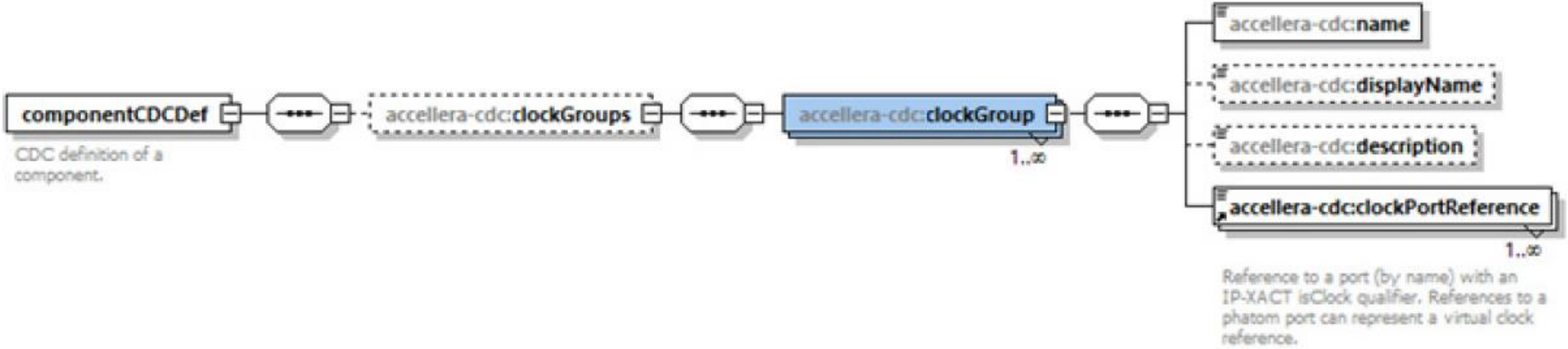
If nio clocks specified then the property is static with respect to any clock.

Can be binary, hexadecimal (using the 0x notation) and of any length.

IP-XACT Format for CDC (4/4)

- The extension accellera-cdc:componentCDCDef is defined to capture the clock groups of a component using the accellera-cdc:clockGroup extensions

- It contains references to clock ports or phantom ports (virtual clock) in addition to name, displayName, and description.



componentCDCDef

CDC definition of a component.

accellera-cdc:clockGroups

accellera-cdc:clockGroup

1..∞

accellera-cdc:name

accellera-cdc:displayName

accellera-cdc:description

accellera-cdc:clockPortReference

1..∞

Reference to a port (by name) with an IP-XACT isClock qualifier. References to a phatom port can represent a virtual clock reference.

TCL Format for CDC

- TCL Format for CDC specification is a set of API commands
- One cdc file per block/module
  - users specify the CDC attributes for ports of that module
  - users can also specify clock groups
- EDA tools should process the CDC specification in TCL format and generate corresponding IP-XACT collateral
- Similarly, there could be a requirement for generating TCL specification of CDC from IP-XACT

API Commands

- **cdc_set_module** : indicates the block/module name for which cdc specification is being provided in a file
- **cdc_set_port** : sets attributes of a port
- **cdc_set_clock_group** : set clock groups of synchronous clocks
- **cdc_set_param** : defines parameters within the scope of a module

2.6 Training Subgroup

Training Subgroup Mission

- Goal

1. **Raising awareness of** the importance of defining **a standard CDC-RDC model**
2. **Provide generic documentation** to let the CDC-RDC IP model user understand :

   1.1 CDC-RDC basic knowledge

   1.2 List of attributes & definition (related to IP CDC-RDC features/properties) as defined and agreed by the main CDC WG

3. Presentation of the **hierarchical flow**

   2.1 tool dependency issue

   2.2 necessity to create an inter operational CDC-RDC model

4. Inter operational CDC-RDC model **integration manual**

Conferences

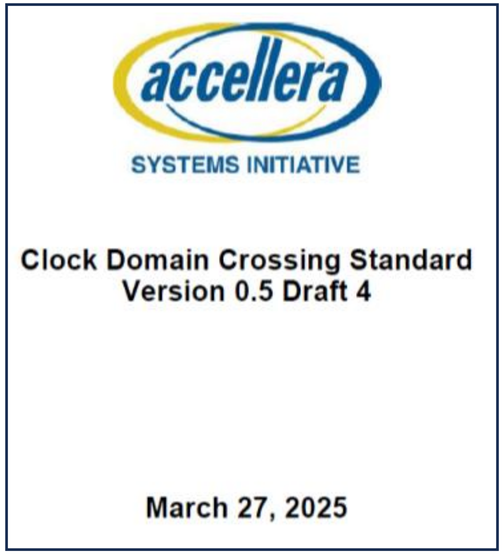
- Accellera CDC WG work promotion through conferences
  - Past/current conferences
    - DVCON Europe 2023, 2024, 2025
    - DVCON US 2024, 2025
    - DVCON Japan 2024, 2025
    - DVCON India 2024, 2025
    - IP-SoC Design Reuse conference Europe 2024
    - DVCON China 2025
    - DAC 2025
    - DVCON Taiwan 2025
  - Targeted conferences (To Be Confirmed)
    - DVCON Japan / India / Europe / Taiwan 2026
    - IP-SoC Design Reuse conference Europe 2025
    - DATE 2026
    - VLSI 2026
    - DAC 2026
    - DVCON China 2026

2.7 Call For Contribution

Language Reference Manual (LRM)

Version 0.5 of the CDC LRM has been released for public review on 14 April 2025

- [CDC 0.5 Public Review Draft 2025.04.14]()
- Download the CDC Draft Standard 0.5: https://bit.ly/3tdwMpe
- Forum: https://bit.ly/42vYdb4



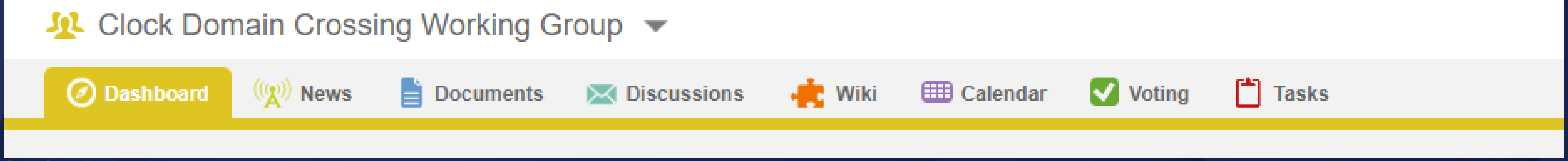
accellera
SYSTEMS INITIATIVE

Clock Domain Crossing Standard
Version 0.5 Draft 4

March 27, 2025

Call for Contribution !

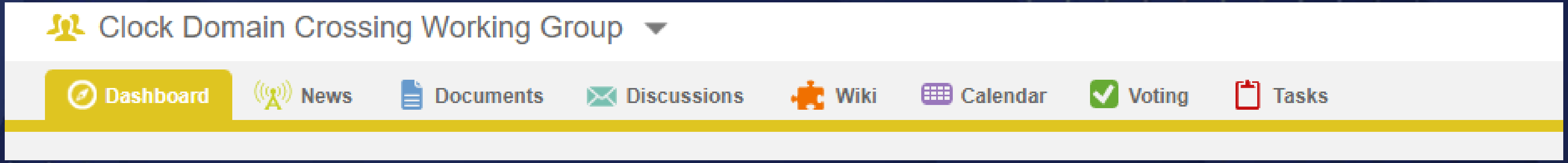
Accellera CDC Working Group



https://workspace.accellera.org/wg/CDC

Call for Contribution !

Accellera CDC Working Group



accellera.org/activities/working-groups/clock-domain-crossing

Non-Accellera members can join and provide feedback on the standard: forums.accellera.org

Questions?