

2022
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
UNITED STATES
SAN JOSE, CA, USA
FEBRUARY 28 - MARCH 3, 2022

CAMEL – A Flexible Cache Model for Cache Verification

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Outline

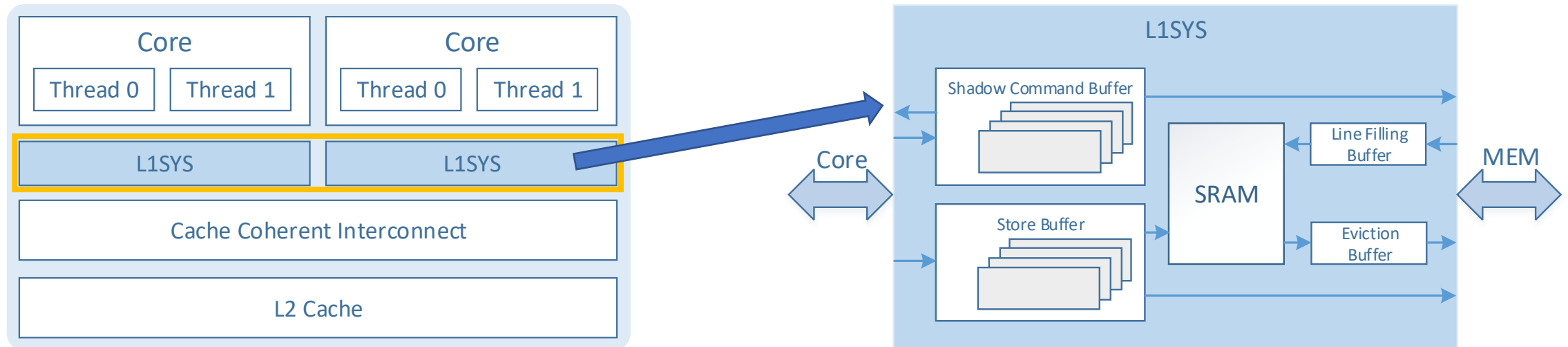
- Design overview
- CAMEL model structure
- Attributes for precise check
- Summary

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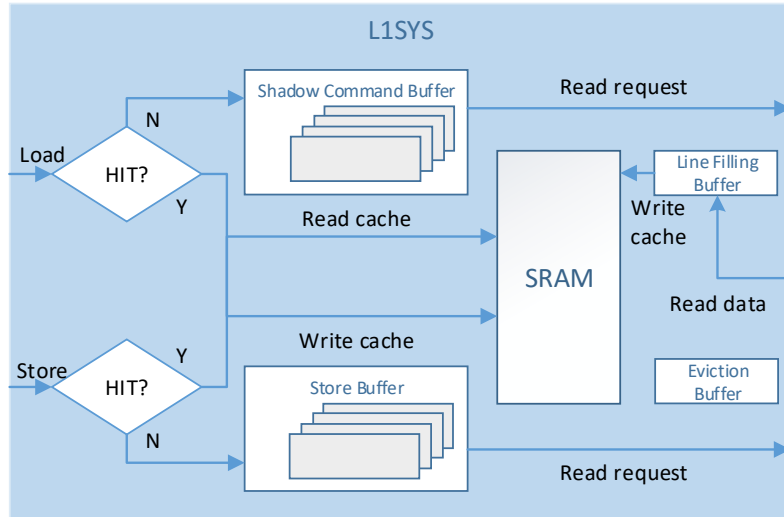
Design Overview

- Level 1 Cache(L1SYS)
- Multi thread
- Complex buffers for efficiency



Design Overview

- Multi thread characteristic
 - Each thread is independent
 - One thread's cache miss not stall other threads
 - Multi threads influence each other by sharing common buffers
- Basic data flow



Shadow command buffer(SCB):

preserve miss command and fetch data in background

Store buffer(STB):

preserve store data and fetch data in background

LineFilling buffer(LFB):

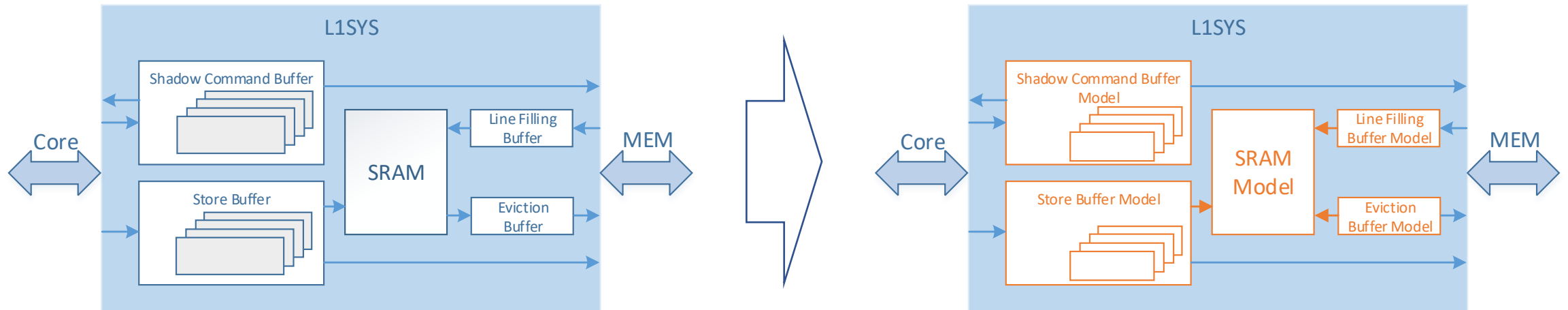
preserve read data from external bus

Eviction buffer(EB):

preserve data been victimed

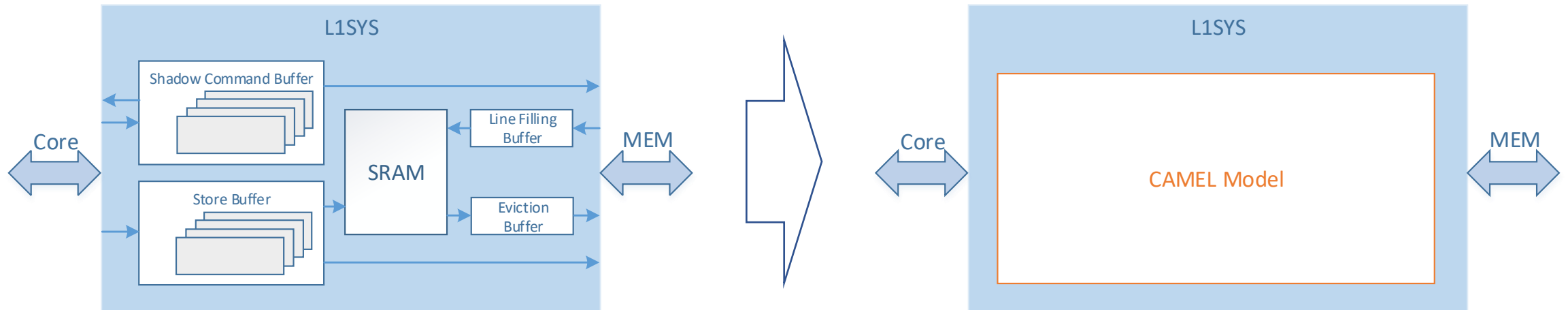
Design scope from verification view

- Before



Design scope from verification view

- Now

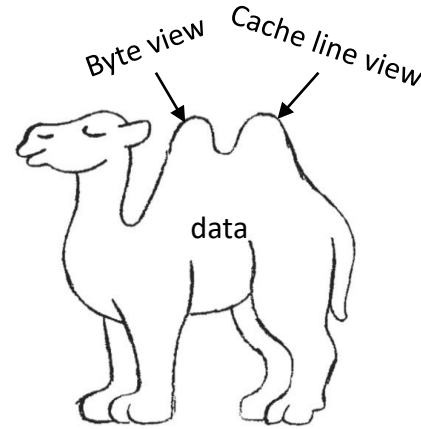


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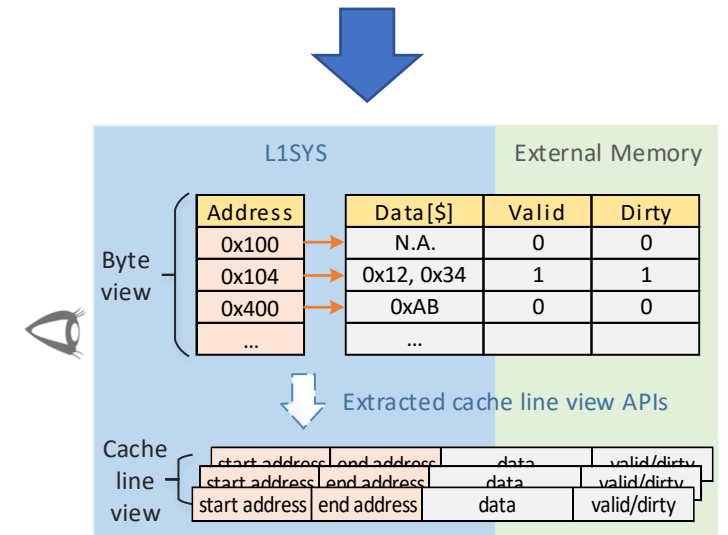
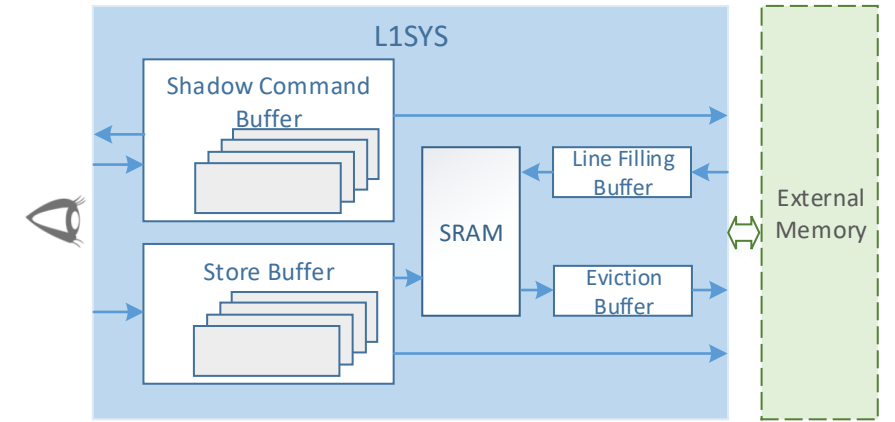
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- **CAMEL model structure**
- Attributes for precise check
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CAMEL model structure

- Definition and goal
 - CAMEL: **CA**che **MO**dE**L**
 - Data correctness
 - > compare read data



- Structure
 - Address vs. {data + attributes}
 - Two views of data in model
 - Byte view -- CAMEL's basic storage unit
 - Cache line view -- APIs base on byte unit



CAMEL model structure

- Example

CAMEL predicts read data result

Address	Data[\$]	Valid	Dirty
0x104	N.A	0	0
0x104	0x12	1	0
0x104	0x12, 0x34	1	1

Load miss

Send read request to Ext. mem

Receive read data from Ext. memory

Core get the load data

Thread 0

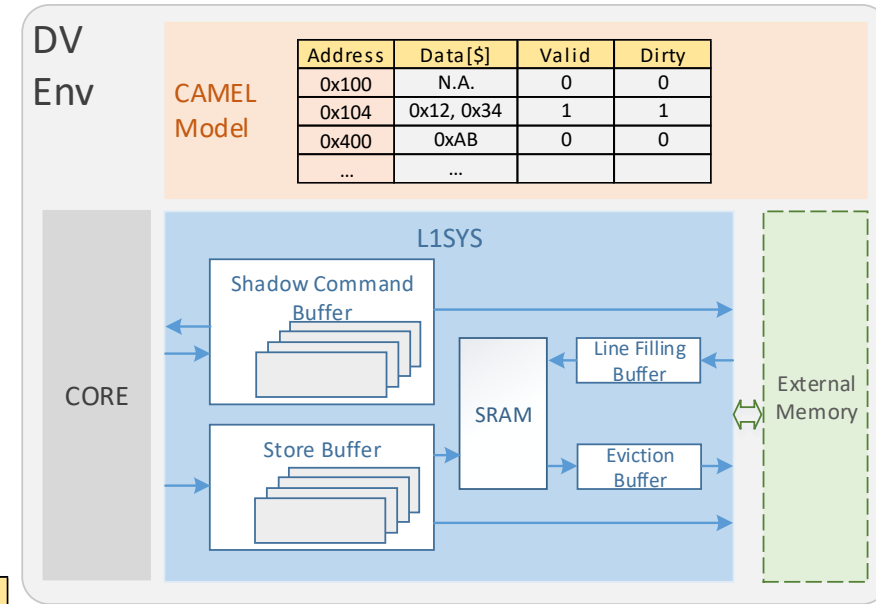
Thread 1

Time A Time B

Time C

Store data

Address	Data[\$]	Valid	Dirty
0x104	0x34	0/1	1

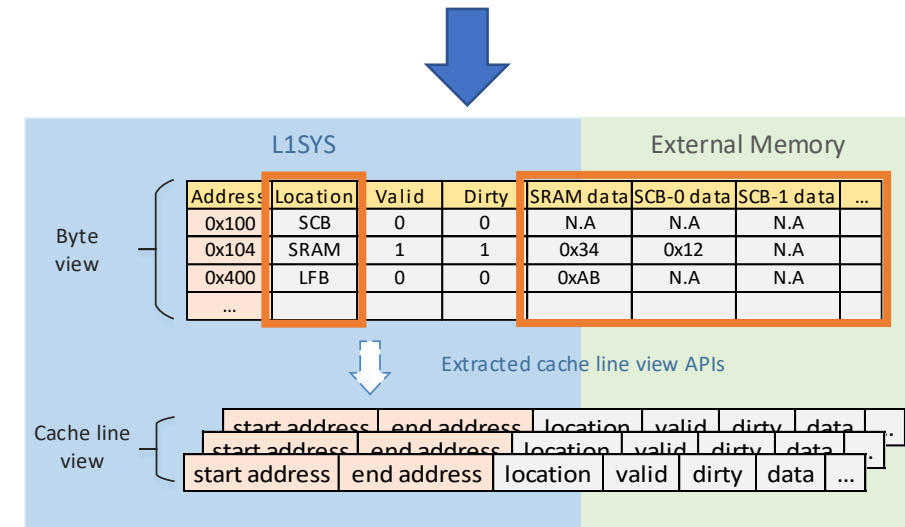
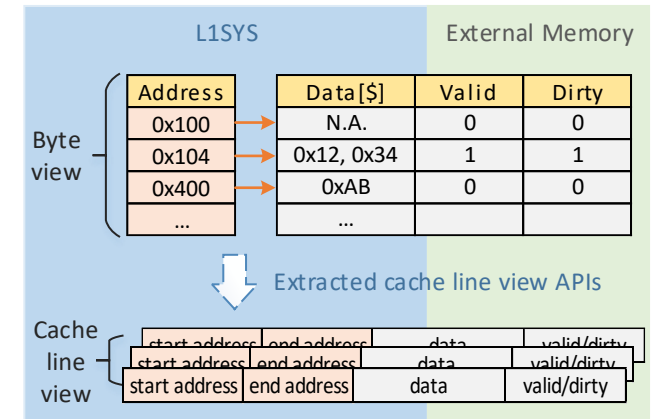


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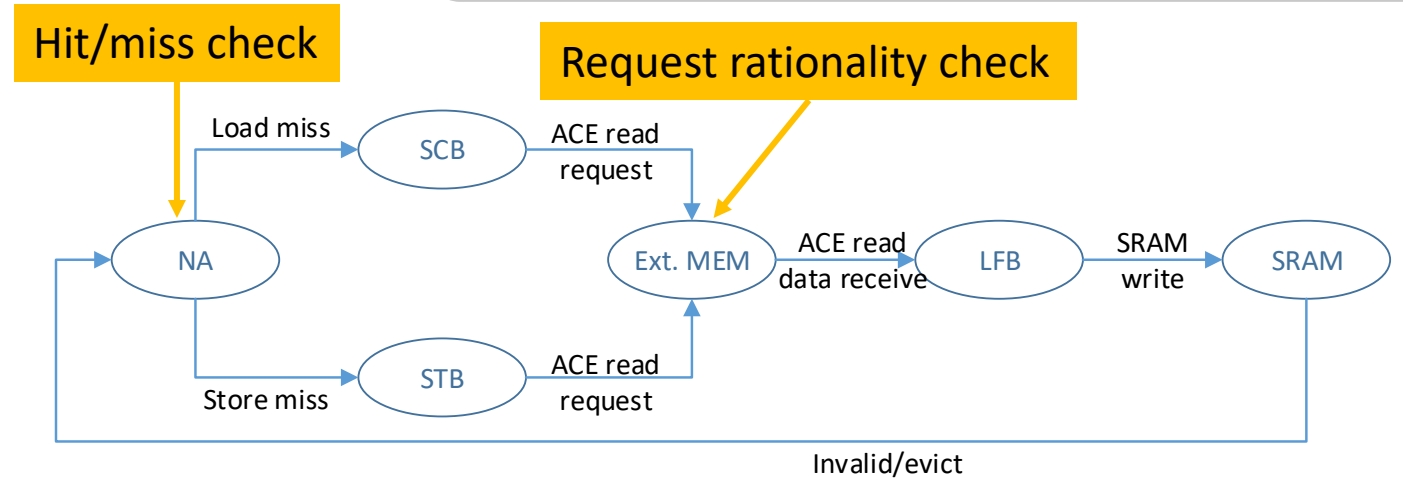
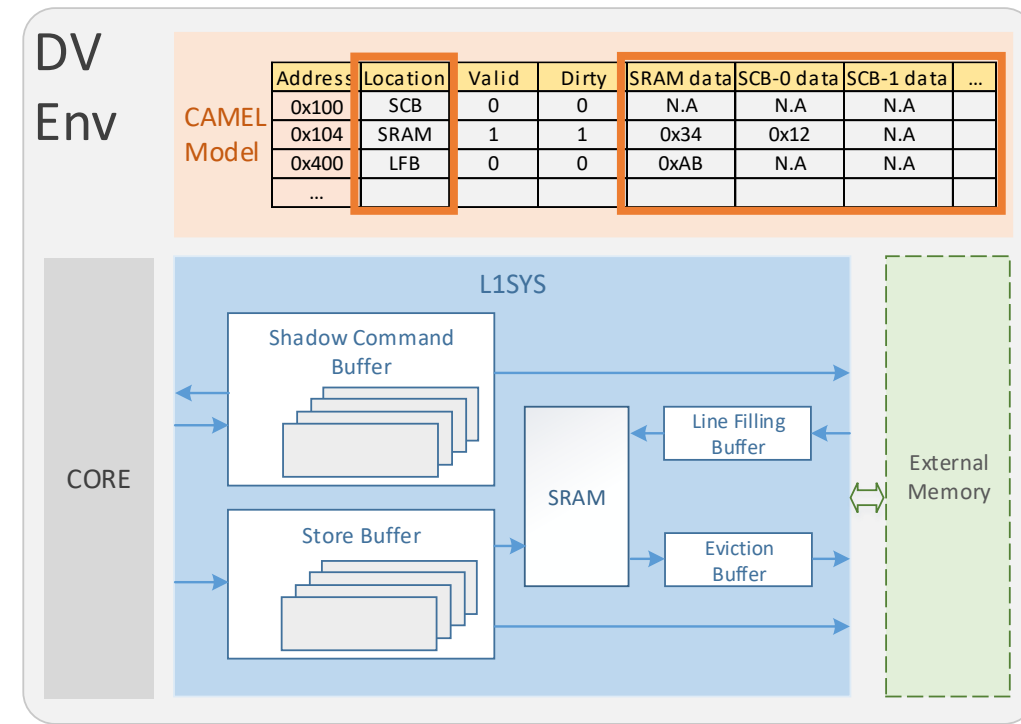
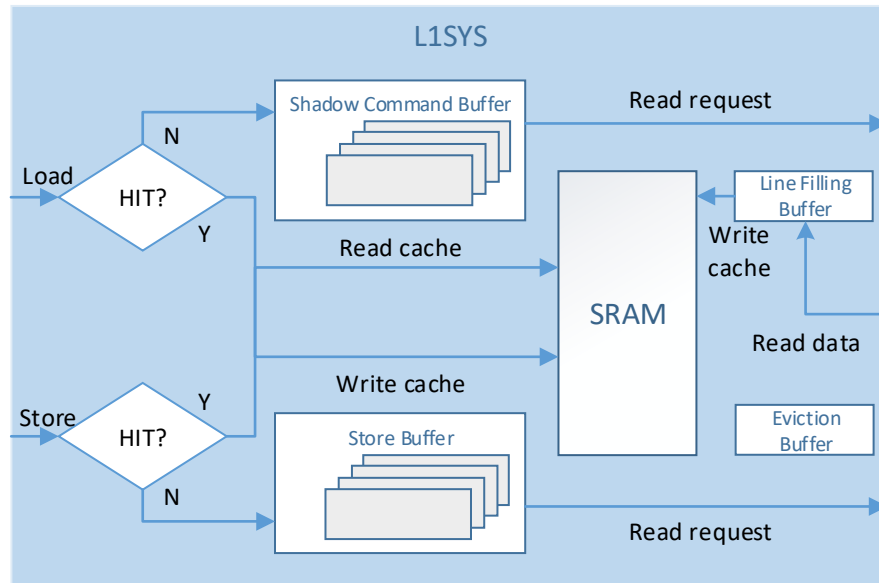
Attributes for precise check

- Precise data check
 - Read data range -> smaller data range/a certain data
- Rationality check of request to external memory
 - Output of L1SYS
- Hit/miss check
 - Load instruction performance
 - Store instruction earlier bug trace



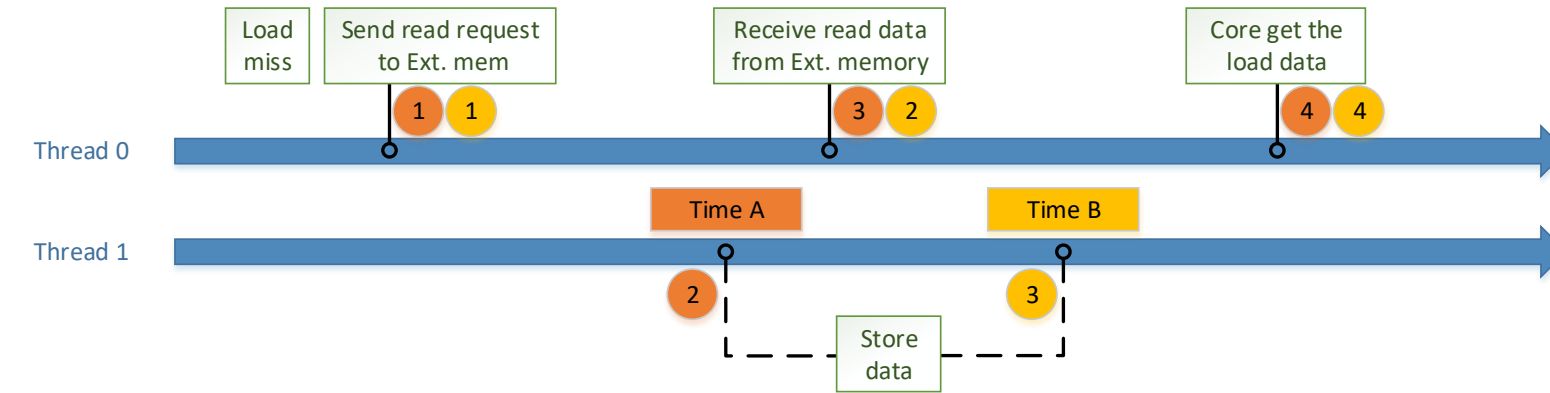
Attributes for precise check

- Location: where the data is locating
- SCB-x data: extra info for data check
- ...



Attributes for precise check

- Example after using 'location' and extra info

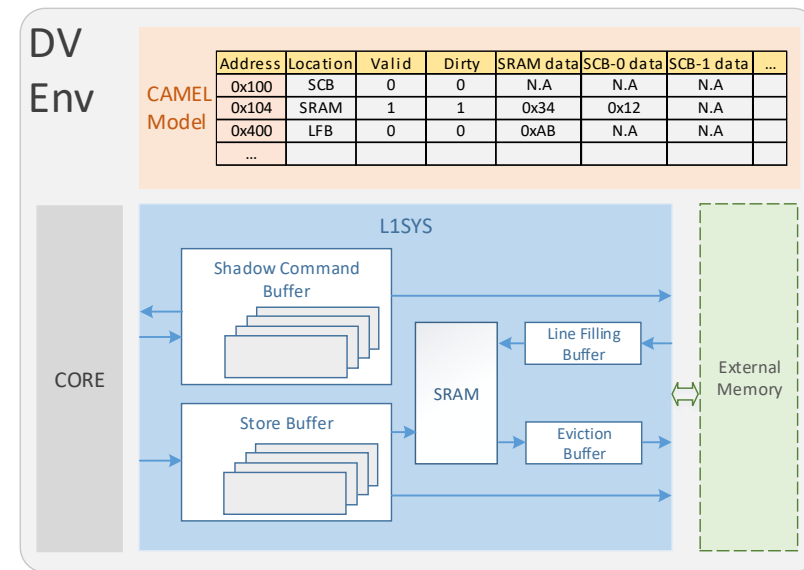


	Address	Location	Valid	Dirty	SRAM data	SCB-0 data	SCB-1 data
1	0x104	Ext. Mem	0	0	N.A	N.A	N.A
2	0x104	Ext. Mem	0	1	0x34	N.A	N.A
3	0x104	LFB	0	1	0x34	0x34	N.A
4	0x104	SRAM	1	1	0x34	0x34	N.A

Store comes at time A

	Address	Location	Valid	Dirty	SRAM data	SCB-0 data	SCB-1 data
1	0x104	Ext. Mem	0	0	N.A	N.A	N.A
2	0x104	LFB	0	0	0x12	0x12	N.A
3	0x104	SRAM	1	1	0x34	0x12	N.A
4	0x104	SRAM	1	1	0x34	0x12	N.A

Store comes at time B



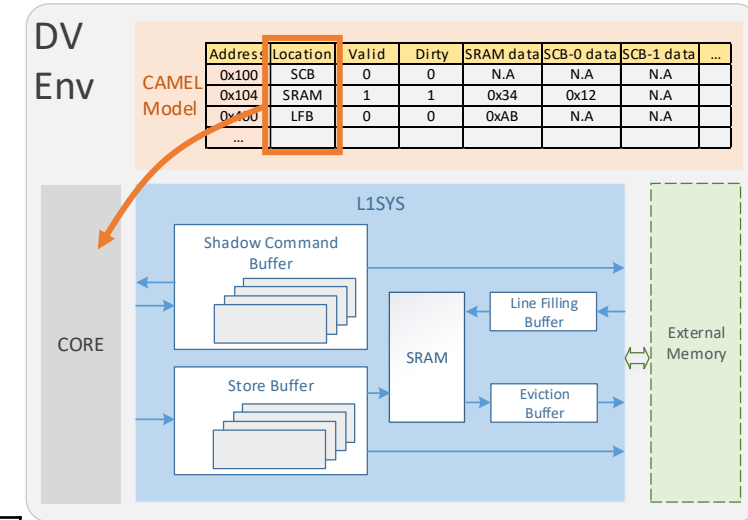
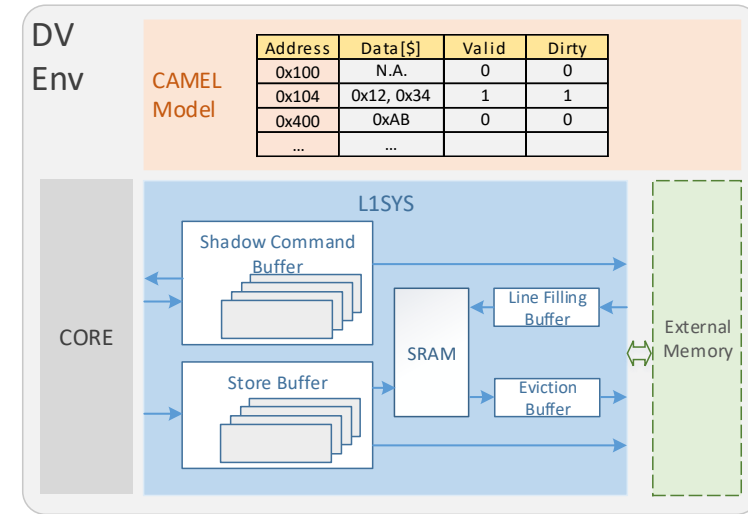
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- Basic CAMEL model
 - Simple structure, acceptable for basic data check
- CAMEL model with extra attributes
 - More complex, but can support more precise checkers
- Stimulus feedback by 'location'
 - More effective stimulus
- CAMEL model vs. buffer behavior model
 - More general, able to reuse
 - Code lines

	Previous	Current	
		CAMEL model	Other models
VIP number	5	3	
model number	6	1	2
model code lines	8513	1915	622



Questions