CAMEL – A Flexible Cache Model for Cache Verification

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Outline

• Design overview
• CAMEL model structure
• Attributes for precise check
• Summary
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Design Overview

- Level 1 Cache (L1SYS)
- Multi thread
- Complex buffers for efficiency
Design Overview

- Multi thread characteristic
  - Each thread is independent
  - One thread’s cache miss not stall other threads
  - Multi threads influence each other by sharing common buffers

- Basic data flow

Shadow command buffer (SCB):
  - preserve miss command and fetch data in background

Store buffer (STB):
  - preserve store data and fetch data in background

LineFilling buffer (LFB):
  - preserve read data from external bus

Eviction buffer (EB):
  - preserve data been victimed
Design scope from verification view

• Before
Design scope from verification view

• Now
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CAMEL model structure

• Definition and goal
  • CAMEL: CAnche M odEEL
  • Data correctness
    -> compare read data

• Structure
  • Address vs. {data + attributes}
  • Two views of data in model
    • Byte view -- CAMEL's basic storage unit
    • Cache line view -- APIs base on byte unit
CAMEL model structure

- Example

<table>
<thead>
<tr>
<th>Address</th>
<th>Data($)</th>
<th>Valid</th>
<th>Dirty</th>
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<tr>
<td>0x104</td>
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<td>0</td>
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<td>0x12, 0x34</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0x104</td>
<td>0xAB</td>
<td>0</td>
<td>0</td>
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<tr>
<td>...</td>
<td>...</td>
<td>...</td>
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CAMEL predicts read data result

Thread 0
- Load miss to Ext. mem
- Receive read data from Ext. memory
- Core get the load data

Thread 1
- Time A
- Time B
- Store data

<table>
<thead>
<tr>
<th>Address</th>
<th>Data($)</th>
<th>Valid</th>
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CAMEL Model Structure

- DV Enviroment
- CORE
- L1SYS
- SRAM
- Shadow Command Buffer
- Store Buffer
- Line Filling Buffer
- Eviction Buffer
- External Memory

Data[()] Valid Dirty
N.A. 0 0
0x12, 0x34 1 1
0xAB 0 0
...
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Attributes for precise check

- Precise data check
  - Read data range -> smaller data range/a certain data
- Rationality check of request to external memory
  - Output of L1SYS
- Hit/miss check
  - Load instruction performance
  - Store instruction earlier bug trace
Attributes for precise check

- Location: where the data is locating
- SCB-x data: extra info for data check
- ...

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<th>SRAM data</th>
<th>SCB-0 data</th>
<th>SCB-1 data</th>
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![Diagram showing the flow of memory operations and data requests](image-url)
Attributes for precise check

• Example after using ‘location’ and extra info
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Summary

• Basic CAMEL model
  • Simple structure, acceptable for basic data check

• CAMEL model with extra attributes
  • More complex, but can support more precise checkers

• Stimulus feedback by ‘location’
  • More effective stimulus

• CAMEL model vs. buffer behavior model
  • More general, able to reuse
  • Code lines

<table>
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Questions