Bringing Reset Domains and Power Domains together – Confronting issues due to UPF Instrumentation.

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Abstract – The Unified Power format (UPF) standard enables designers to add power intent for the design. For power management designers typically partition design into power domains. Interactions between these power domains are done through various power control logics like retention logic, isolation logic, level shifters, etc. Designers need to validate that the power control logic does not introduce new multi-clock and multi-reset issues into the design. This paper specifically talks about the issues encountered in Reset Domain Crossing introduced by UPF instrumentation. UPF instrumentation may lead to higher number of new Resets which are not part of the design specification leading to huge verification turnaround time. This paper also explores the possibilities of enhancing the features of a static verification tool by proposing new rulesets for the tool.

Keywords: Reset Domain Crossing (RDC), Clock Domain Crossing (CDC), Power Aware RDC (PA-RDC), Unified Power Format (UPF), Power Instrumentation, Active Power Management (APM), Dynamic Voltage Frequency Scaling (DVFS).

I. INTRODUCTION

Today's complex SoC design introduces new challenges. Complex SoCs have many independent functional blocks. The blocks may be having different boot and clocking protocols leading to the introduction of the reset domains and clock domains. Interactions between the reset domain leads to reset domain crossing (RDC) issues. Similarly, interactions between different clock domains leads to clock domain crossing (CDC) issues. Both RDC and CDC are the non-trivial issues which designers must verify. Also, there can be the power domains that may further lead to an increase in verification complexity. When it comes to power domains one of the challenges faced by designers is active power management (APM).

Active Power Management (APM) is the application and control of power reduction techniques to minimize power consumption, especially static leakage. Various power reduction techniques like clock gating, power gating, multi-voltage design, voltage/frequency scaling are used by designers. Designers partition the design into multiple power domain regions that can be selectively powered on/off based on the application requirements. Interactions between these power domains are done through various power control logics like retention logic, isolation logic, level shifters, etc. Alongside the reset, supply and connectivity to different blocks operating in different power domains may vary from one power domain to another thus adding complexity in verification. Ignoring such cases will have a huge impact during the re-initialization of registers. This prevents the design to reset to a known good state as it cannot sample the retained values on power-up. It becomes crucial to understand the data interactions between different power domains along with RDC paths to make sure that the design does not go into an unknown/corrupted state.

The Unified Power Format (UPF) standard enables us to describe the power management architecture of the design also known as "power intent". Though UPF specification assists in the design and verification process, UPF instrumented elements may pose different challenges in clock and reset domains crossings. Along with low power verification for functional correctness, designers also need to validate that the power control logic does not introduce new multi-clock and multi-reset issues into the design. One such example of typical problem designers may encounter is through instrumented isolation cells. If there is data interaction between two power domains isolation logic is inserted at the power domain boundaries to ensure correct electrical and logical operation. Adding isolation logic may introduce new resets leading to new RDC paths. This may introduce new challenges in design and verification efforts.

UPF instrumentation may lead to a higher number of new resets that are not part of the design specification. Resets that are not part of a design specification may lead to increasingly complex RDC results which in turn may increase the verification effort because of the higher number of violations encountered in a static verification tool. Consider a scenario where top-level resets drive different blocks/IPs in the design in a defined sequence to make sure all the blocks are brought to the normal state. All the registers resettable in the design should be reset when the global reset is asserted. A missing connection or reset signal blocked during propagation due to newly introduced/inferred resets between different power domains can easily go undetected.

To achieve both higher performance and lower power usage design teams incorporate advanced power management techniques through the power management logic which is described in a unified power format file (UPF) and is described outside the RTL logic. A UPF specification normally details, the names and number of power domains, their constituent elements in terms of HDL instances, the power distribution network for the system, and the corresponding power states. This power architecture specification though UPF is valid and applicable in the entire design process right from abstract functional specification to actual physical implementation. Hence the UPF which specifies the abstract logic can be considered both a functional specification and a physical implementation.

As more power strategies are incorporated RDC errors are found in design. Since the power control logic is implemented late in the design cycle, these RDC errors get missed by traditional RDC techniques. When RDC analysis is run only on the RTL design the RDC crossings generated by the power control logic will not be analyzed. With the addition of power control logic, new RDC paths may get introduced or existing RDC paths may get disrupted. Designers must verify that the design and power elements together does not introduce an unexpected metastability into the design. For example, a design without power logic might have a reset domain crossing that is properly synchronized. But, adding power control logic adds combinational logic to the crossing, which makes the crossing unsynchronized.

Designers use dynamic voltage and frequency scaling (DVFS) techniques to lower the power consumption. The maximum operating frequency is dependent on the voltage. When a design is operating in a power saving mode at a lower frequency, the lower frequency allows reduction of voltage thereby reduction of power consumed. Research has shown that a small reduction in voltage results in large power savings.

But there is a downside to dynamic voltage scaling. Studies have shown that synchronous clocks on a voltage domain using dynamic voltage scaling will behave asynchronously relative to all other clocks in other voltage domain. This means any synchronous crossing to or from the voltage domains will cause metastability (Fig. 1). These voltage domain crossing paths must be treated in the same way as clock domain crossing paths and must be synchronized in the receiving voltage domain [1]. Similarly, all the synchronized reset domain crossings will become unsafe crossings if there is a data interaction happening in voltage crossing domains.

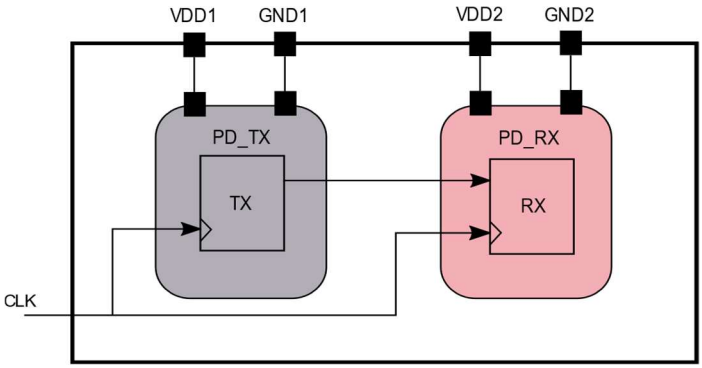

Figure 1. Same clock reaching different Voltage domain treated asynchronous

II. STATIC ANALYSIS WITH AND WITHOUT UPF INSTRUMENTATION

We now discuss typical issues encountered during static analysis in a UPF instrumented multi-million gate design. Large SoCs typically have many primary and inferred clocks/resets. Inferred clocks/resets are the one derived by the static analysis tool while primary clocks/resets are given by the designer. The effort on the static analysis of the design having signals crossing various domains largely depend on the number of clocks and resets. Larger the inferred clocks

and resets more will be the effort in signing off the RTL. Verification engineers may have to add new waivers for noisy or false violations leading to an extra waiver management effort. A robust solution is to identify potential cases upfront which may occur due to UPF instrumentation. Consider Table I which depicts a scenario where UPF instrumentation led to an increased number of inferred clocks and resets.

Table I
Change in Resets and Clocks numbers after UPF instrumentation

	Type	SoC Design without UPF	SoC Design with UPF
Clocks	User-Specified	5	5
	Inferred	1405	1507
Resets	User-Specified	113	113
	Inferred	599	717

We found that the rise in inferred Clocks and Resets was mainly due to addition of extra combinational circuitry in reset and clock paths. The tool labelled these extra clock and resets as “gated mux” or “gated combo” as these are generated either through a MUX or a combinational logic which got instrumented through UPF. Change in number of clocks and resets led to some safe crossings marked as unsafe by the tool. For example, safe crossings which were marked ordered reset crossings by the tool got changed to unsafe “asynchronous reset to asynchronous reset” crossings. This disrupted the reset ordering sequence. Extra “combinational logic before synchronizer” crossings were also reported. Overall, we saw a 23.6 % rise in violation count. Most of the extra violations were result of instrumentation of isolation logic cell whose select was driven from a different clock or reset domain. Adding synchronizer structures in the select signal may reduce lot of violations, but this may not suffice. Design and verification engineers must also consider some special cases. We have investigated some scenarios which need designer/verification engineers’ attention and must be resolved for a healthy design. Next section discusses some of the common scenarios which we have encountered during UPF instrumentation.

III. PROBLEMATIC SCENARIOS LEADING TO RDC ISSUES

Power control logic typically involves isolation logic, retention logic, level shifters, etc. Below are some scenarios of instrumented power control logics which lead to RDC issues.

A. ISOLATION LOGIC

Scenario 1 - Consider Fig. 2 schematic. Initially there is no reset domain crossing between u_f4 and u_f2 as they are both in same reset domain (rst1). Also, u_f4 and u_f2 are in same power domain. Insertion of Isolation cell brings in another reset domain (rst3) via isolation_enable signal. This creates an additional RDC path in the design.

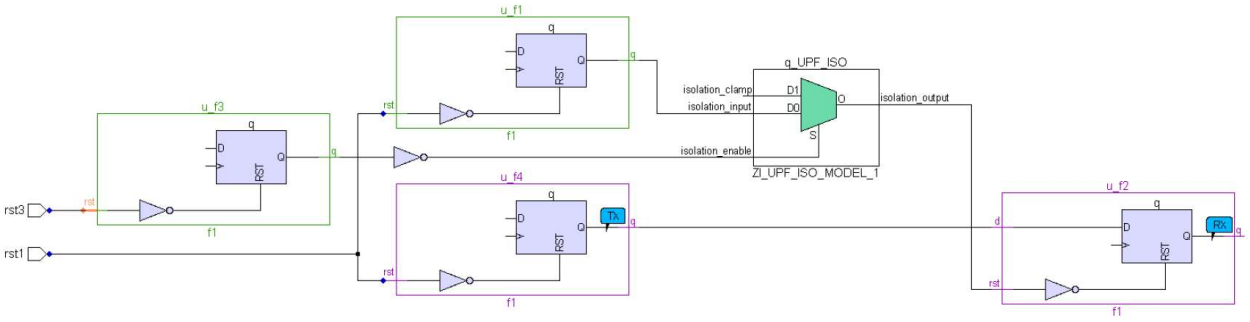

Figure 2. Isolation Enable in different reset domain

Scenario 2 - Consider Fig. 3 schematic. Before UPF instrumentation flops u_f1 and u_f2 are in different reset domains, but the crossing is safe if a reset ordering sequence is provided between rst1 and rst2. After UPF instrumentation rst3 disrupts the ordering and there is a crossing between rst3 and rst2.

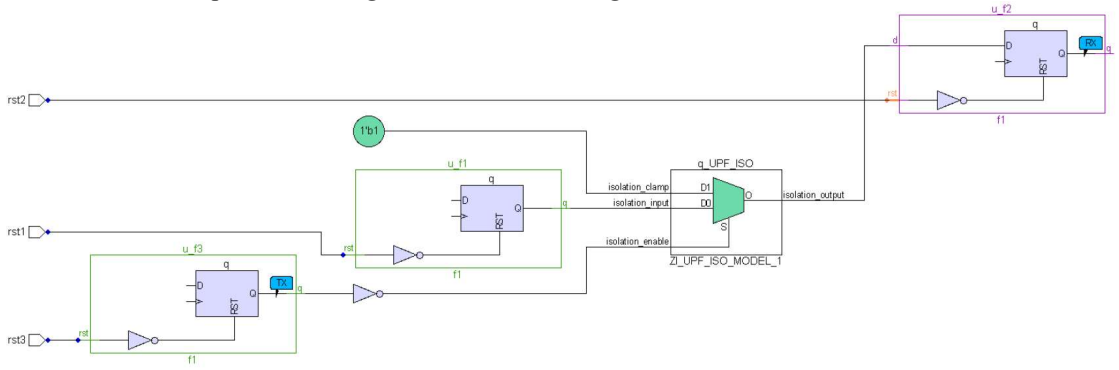

Figure 3. Isolation cell disrupts reset ordering

Scenario 3 – Consider schematic of Fig. 4. Here reset of flop u_f3 is controlled by an AND gate. The control signal at the input of AND gate is driven by a latch and u_f3 is in rst1 domain. After instrumentation, an isolation cell is placed between the latch, u_en_lat, and the and gate. Since "isolation_enable" is in rst2 domain, "isolation_output" will be multiple reset domain signal. Input to the AND gate will have conflicting domains making its output as a new inferred reset domain. This adds an additional RDC path.

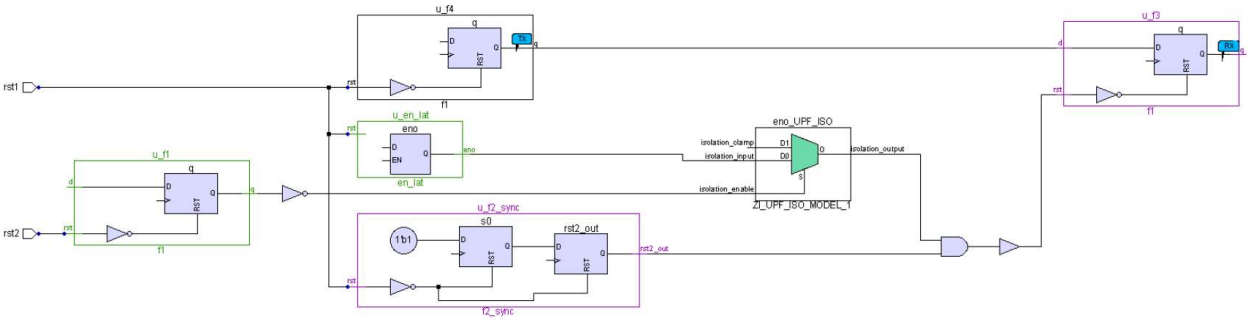

Figure 4. Isolation Cell placed in control path of reset

Scenario 4 – Consider schematic of Fig. 5. Without UPF instrumentation the crossing between Tx (u_f2) and Rx (u_f3) is safe because of flop u_f4 whose reset is same as of u_f2. With UPF instrumentation of isolation control logic in reset path and clock path we see change in the Tx (u_f2) reset and change in Rx clock of u_f3 and u_f4.

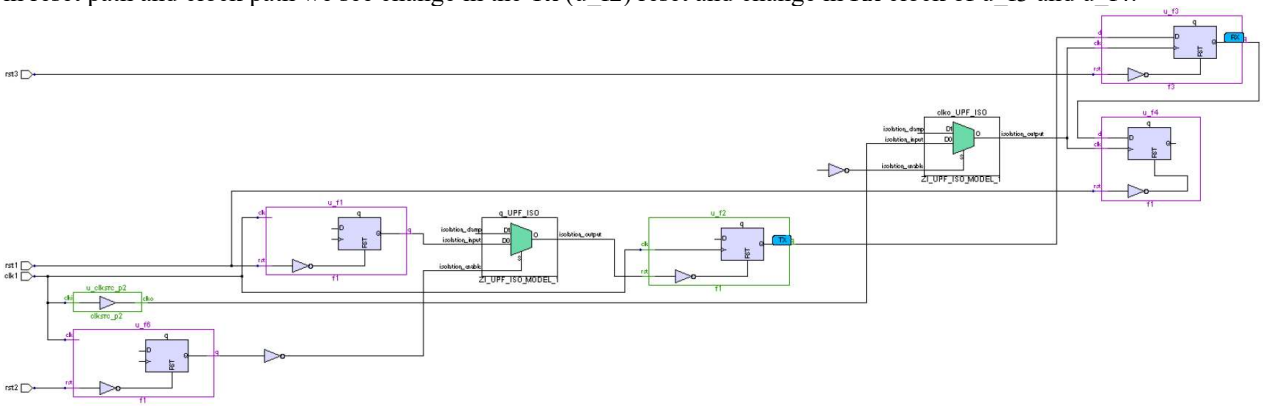

Figure 5. Isolation cell placed in both reset and clock path

Scenario 5 – In Fig. 6 schematic, without UPF instrumentation there was an ordered assertion sequence between u_f1 flop reset (rst1) and u_f2 flop reset (rst2). Insertion of isolation cell in u_f2 brings in multiple resets thereby disrupting the assertion sequence. There is an additional problem. Since isolation_enable is driven by different reset domain, isolation cell can pass the wrong clamp value such that it makes u_f2.rst de-asserted putting u_f2 in a non-reset state.

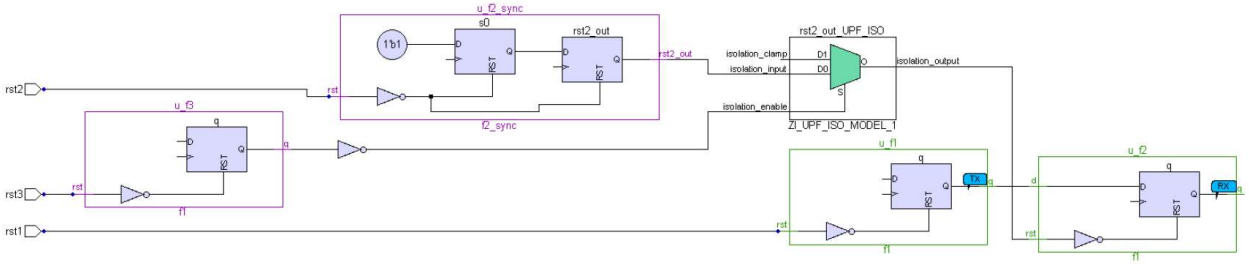

Figure 6. Isolation Cell placed in reset path passing wrong clamp value

Scenario 6 – In Fig. 7, when TX (u_f3) reset, rst3, asserts asynchronously, this will cause isolation cell mux to pass the data to RX (u_f2) flop. There is a high chance that isolation_enable is changing in setup and hold window of u_f2 thereby putting it in metastable state. To resolve specify isolation_enable signal as stable/static or specify reset ordering between rst3 and rst1. A control synchronizer structure in the isolation_enable path can also be added.

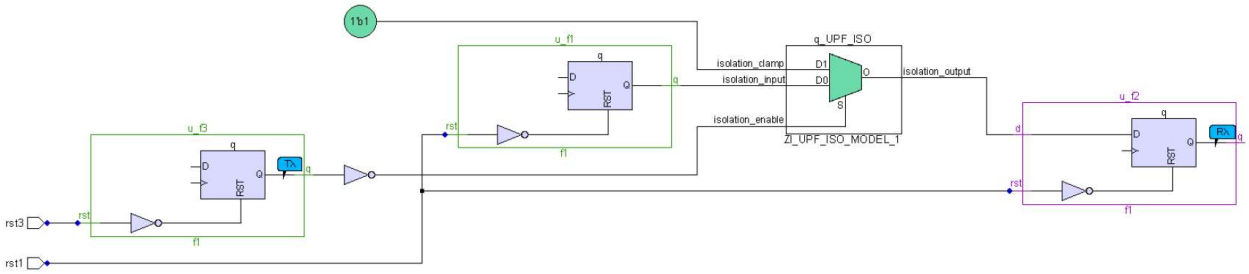

Figure 7. Isolation cell creating a new RDC path

Scenario 7 – Consider Fig. 8 schematic. Asynchronous reset, rst1 is driving data path which can cause metastability in u_f2. u_f2 is reset with rst2 and there is an ordering between rst1 and rst2 so this can be considered a safe crossing. With UPF instrumentation, isolation_enable is in different reset domain, rst3. This disrupts the actual ordering between rst1 and rst2 and hence makes the crossing unsafe. Also, isolation cell being a combination logic will bring in potential glitch issue in the reset path.

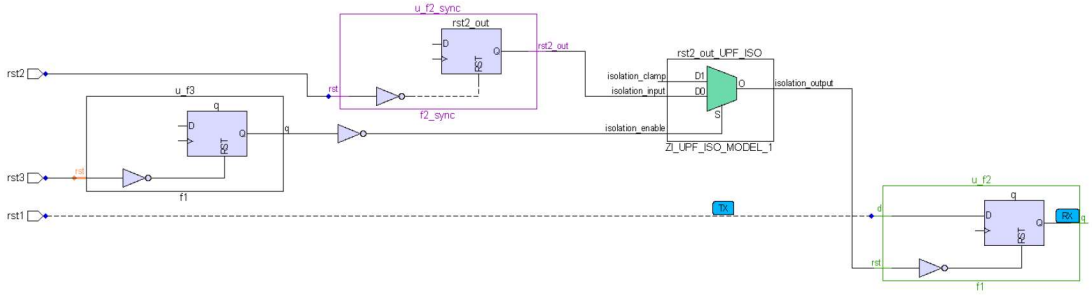

Figure 8. Safe reset ordered crossing changed to unsafe reset crossing

Scenario 8: In the schematic of Fig. 9, clock gating isolation RDC paths which are safe in RTL are no longer safe with UPF instrumented RTL. Clock gating isolation is a special technique to stop metastability issues from occuring on a RDC path. This technique anticipates u_f1.rst domain asynchronous reset activation and preemptively isolates the u_f2 domain logic by deactivating the receive logic clock u_f2.clk thereby avoiding metastability propagation to u_f2 logic. With UPF instrumentation as shown in Fig. 9, the isolation cell is inserted in the clock gating enable path. u_lat is in different power domain and controls the clock gating enable logic. If u_lat powers down and since the isolation clamp value is 1'b1, u_lat will no longer be able to de-activate the reciever register clock u_f2.clk and this will lead to unsafe crossing between u_f1.q and u_f2.q as both the registers are in different reset domains, rst1 and rst2 respectively.

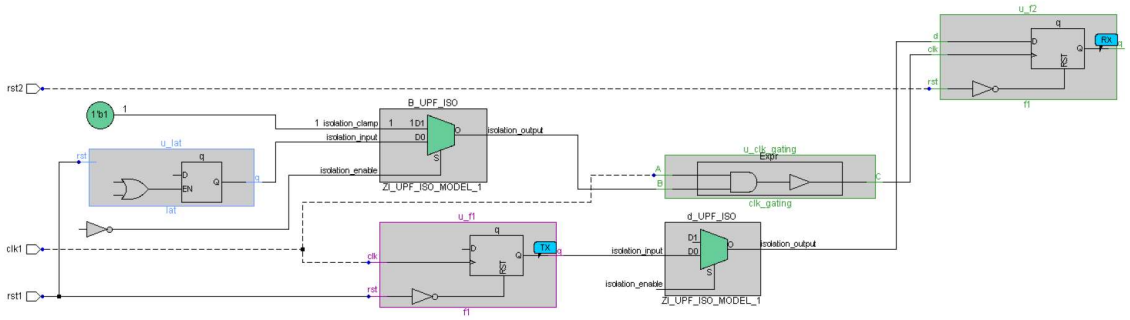

Figure 9. Isolation cell instrumented in clock gating isolation signal

B. LEVEL SHIFTER LOGIC:

Scenario 9: Consider Fig. 10 schematic. Here u_f2_sync and u_f2 are in different voltage domains. This scenario depicts the issues in designs that implement DVFS techniques. Here path between u_f2_sync and u_f2 behave asynchronously as now the clock "clk1" will loose its phase relationship to its attenuated/amplified version (u_f2.clk) reaching u_f2 through level shifter. Reset, rst1 de-assertion will no longer be in sync with u_f2.clk. To resolve this one more synchronizer on reset path is needed in u_f2.clk domain.

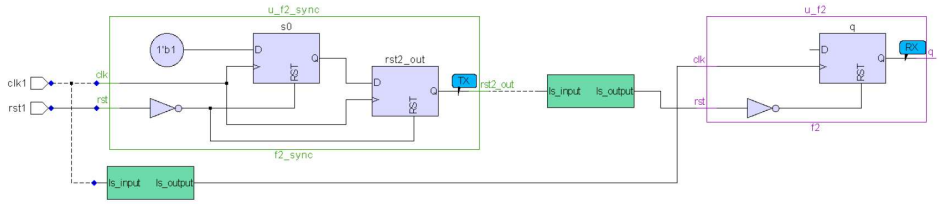

Figure 10. DVFS technique making synchronous path to an asynchronous path

Scenario 10: Consider Fig. 11 schematic. There is already a RDC crossing from rst1 to rst2. With level shifter getting instrumented u_f2.clk will be treated as different asynchronous clock as it will lose phase relationship with clk1. Static tool will report a different violation (reset domain crossing from asynchronous reset to asynchronous reset spanning different clock domains) for the same path. There can be many such violation changes which will add to an extra effort in static verification.

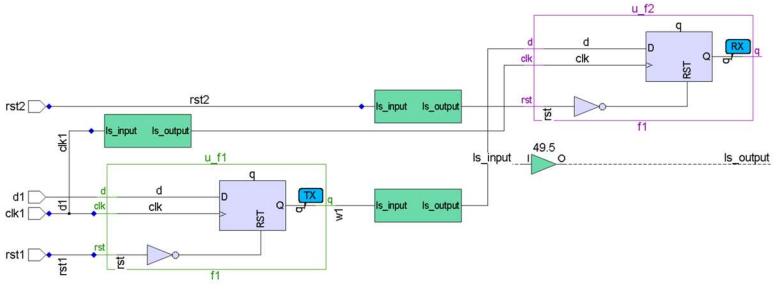

Figure 11. Violation type change because of DVFS

C. RETENTION CELL LOGIC:

Scenario 11: Consider schematic of Fig. 12. Retention save and restore signals are coming from different reset domain, rst3. Metastability issue can occur if u_f2 samples transition values for save and restore signals when rst3 is asserting asynchronously whereas rst2 is de-asserted. Solution is to synchronize save and restore signals in u_f2.clk clock domain or provide an assertion sequence between rst3 and rst2.

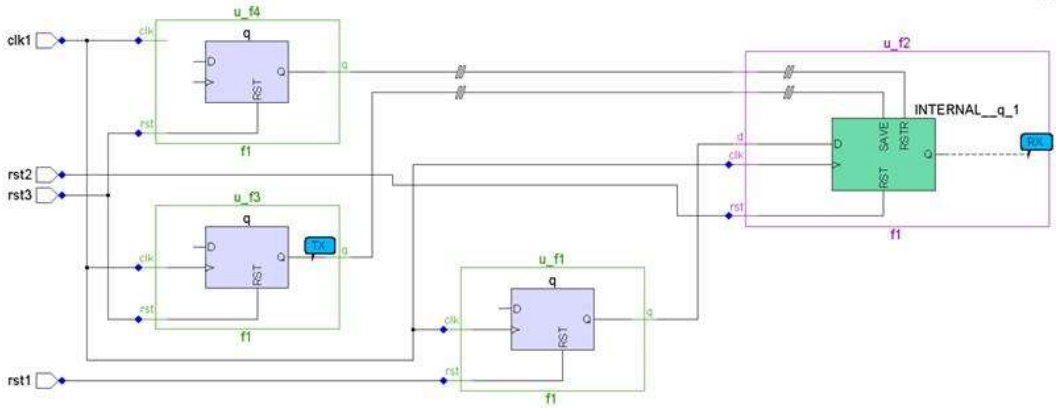

Figure 12. Save and Restore driven by different Reset

Scenario 12: In the schematic of Fig. 13, it seems that both Tx (u_f2) and Rx (u_f3) are driven by rst1 only. But Tx is driven by a source (u_f1) which is in different clock domain, clk2. This leads to a metastability issue as the change at input of source to Tx, i.e. u_f1, can cause an asynchronous assertion of Tx (u_f2). Thus, new RDC crossing is formed between Tx (u_f2) and the newly instrumented retention logic (u_f3).

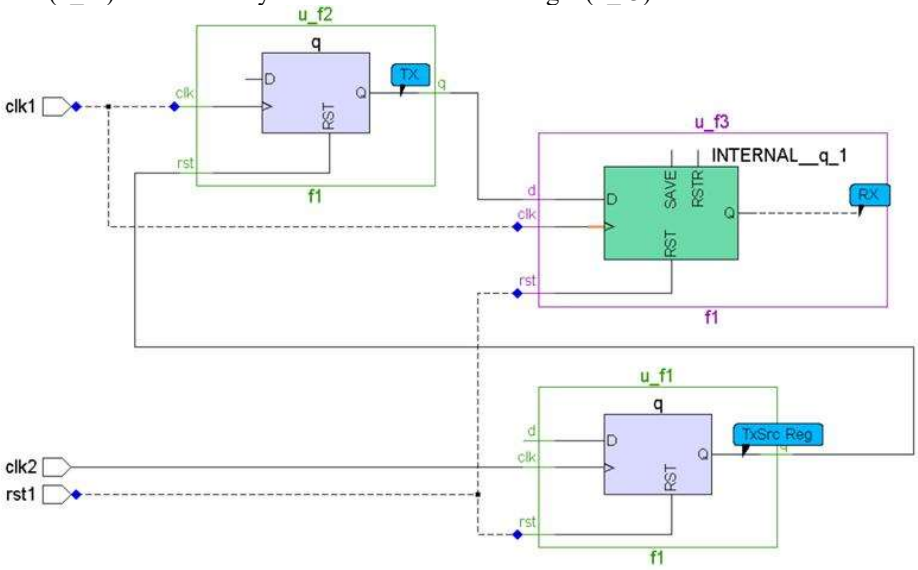

Figure13. Source to Tx driven by different clock leading to metastability in Retention logic

IV. PROPOSED NEW RULE SETS

From our experiments, we have observed that when low power elements are used in the design, there is a strong need to define some of the new rulesets for reset verification to ensure the correct propagation of resets and reset connectivity to blocks which are in on/off power state. Following are the scenarios which depict the strong need for these new checks.

Check 1: Asynchronous reset signal driven by isolation logic is always active due to clamp value.

In Fig. 14 schematic, the asynchronous active low reset signal u_f1.rst is driven by isolation cell logic whose clamp value is a constant 1'b0 that prevent the flop u_f1 from getting out of its reset state.

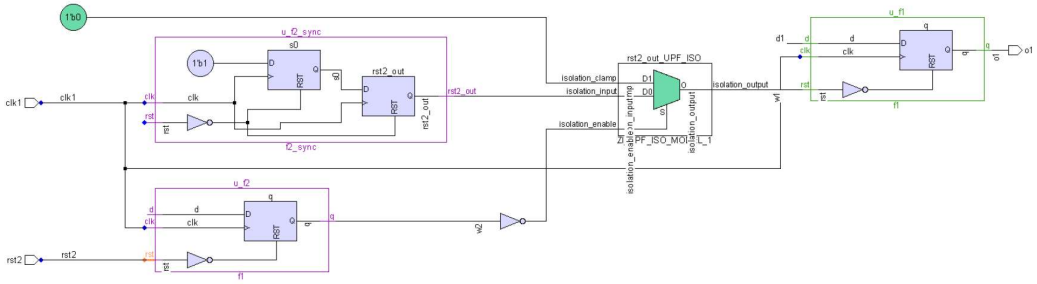

Figure 14. Isolation cell driving constant 0 making flop remain in reset state

Check 2: Isolation Enable is driven by a different reset group.

In Fig. 2 schematic, we have shown that isolation_enable is driven by a different reset group (rst3). As explained in scenario 1 this will lead to an additional RDC path in the design. To resolve this either specify the correct reset groups for the isolation signal such that it belongs to Tx domain or Rx domain or specify the correct reset orderings. The check ensures that designers resolve the new inferred resets due to isolation cells.

Check 3: Reset is driven by power-off domain

This check violates on reset connectivity when resets are driven by a power off domain. Consider Fig. 16 where resets are genrated in u_rst_gen which is in power off domain as evident from its UPF specification, Fig. 15. Designers have to ensure that all resetable registers in all the power domains have a functional reset.

```
create_power_domain PD_VDD1 -elements {u_f1 u_f2 } -supply {primary SS_VDD1}
create_power_domain PD_VDD2 -elements {u_rst_gen } -supply {primary SS_VDD2}
create_supply_net VDD2_sw -domain PD_VDD2
add_port_state VDD1 -state {ON_10 1.0}
add_port_state VDD2 -state {OFF off}
add_port_state VSS -state {ON_00 0.0}
create_pst PST1 -supplies {VDD1 VDD2 VSS}
add_pst_state NORMAL -pst PST1 -state {ON_10 OFF ON_00}
```

Figure 15. UPF Specification

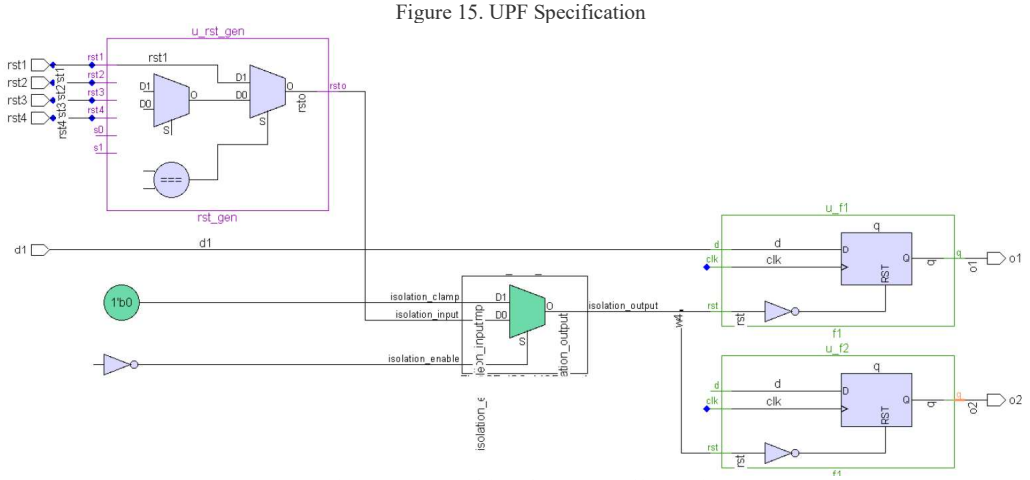

Figure 16. Reset driven by Power-off Domain

V. AN EFFICIENT METHODOLOGY FOR POWER AWARE RDC

The conventional RDC methodology still holds good for power aware designs but there is a need to refine the methodology to incorporate certain issues which may creep in due to power instrumentation. Fig. 17 depicts an efficient methodology for power aware RDC analysis. We feel following steps can help design and verification engineers in RDC analysis of a power instrumented design.

1) Adding power control logic may lead to higher number of resets. All the new resets must be resolved before doing RDC analysis.
2) Adding power control logic may lead to higher number of clocks leading to higher reset domain crossings spanning different clock domains as well as reset de-assertion issues. All the new such clocks must be resolved before doing RDC analysis.
3) Adding power control logic may disrupt existing Reset ordering. Review the newly created resets by examining the reset tree report and check if the newly created reset has in its fan-in a reset which is a part of an existing reset order.
4) If possible, ensure that the control signals of the power control logic are from the Rx reset power domain.
5) Incorrect clamp values of power control strategies can reset the fan-out logic incorrectly. Ensure correct clamp values are defined in the UPF.

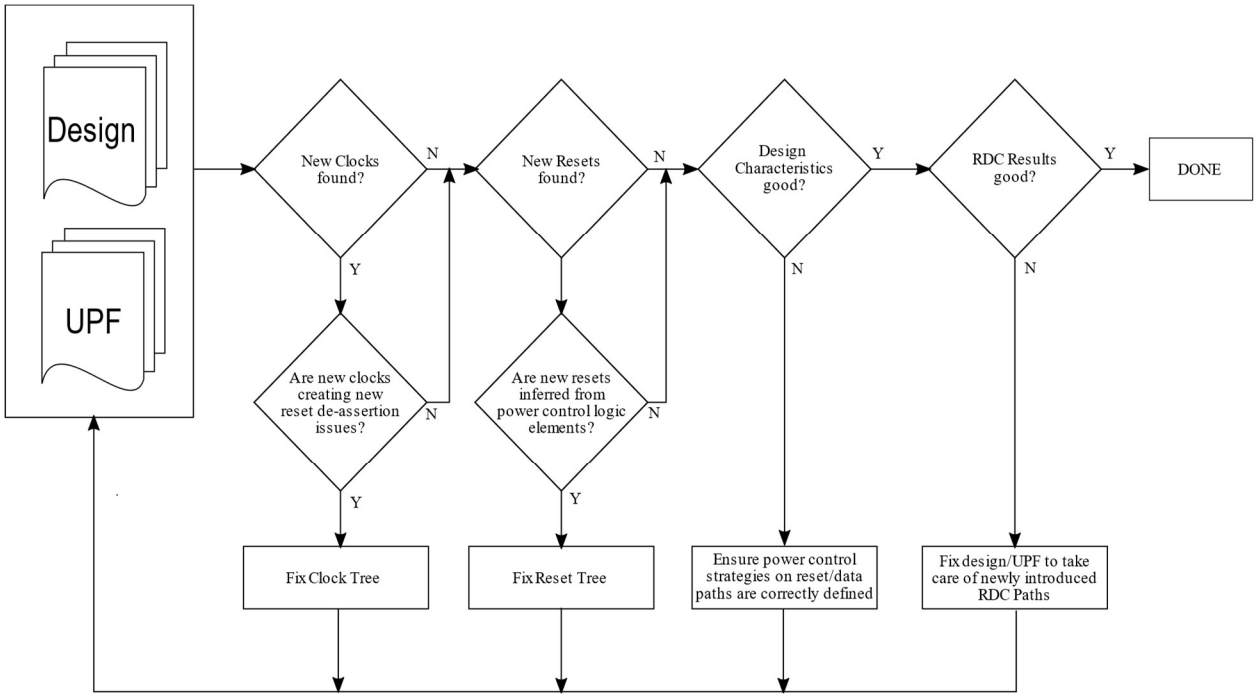

Figure 17 Methodology for Power-Aware RDC

VI. CONCLUSION

In this paper we have shown how metastability can be introduced by UPF instrumentation in reset domain crossing space. We described the challenges designers encounter while working with Power Aware RDC analysis. In this paper we have investigated how newly introduced resets due to UPF instrumentation can affect the data interactions between reset domain paths crossing various power domains. We depicted issues in various valid scenarios from a real life SoC. We showed how low power UPF strategies like the insertion of isolation cells can have a huge impact on the reset strategy as the number of new resets increase dramatically. These issues if undetected, may result in a higher verification turnaround time and unnecessary ECOs resulting in costly re-spins. We also suggested few RDC checks which are otherwise missing in static verification tools. These checks ensure the correct propagation of resets and reset connectivity to the blocks which are in on/off power state. We have explored an efficient methodology to deal with these new RDC issues.

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