BREKER™ THE LEADER IN PORTABLE STIMULUS

2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES
SAN JOSE, CA, USA
FEBRUARY 27-MARCH 2, 2023

Getting Beyond ISA Compliance: Advanced Core/SoC Verification for RISC-V and other Beasts

DVCon 2023 Workshop

Adnan Hamid, CTO, Breker Verification Systems

Agenda

- RISC-V Core and SoC Verification Challenges
- AI Planning Algorithm Techniques for RISC-V Test Synthesis
- RISC-V Ariane/CVA6 Core & OpenPiton SoC
- RISC-V Core Integrity Test Synthesis
- RISC-V SoC Integrity Test Synthesis
- Conclusion

RISC-V Core and SoC Verification Challenges

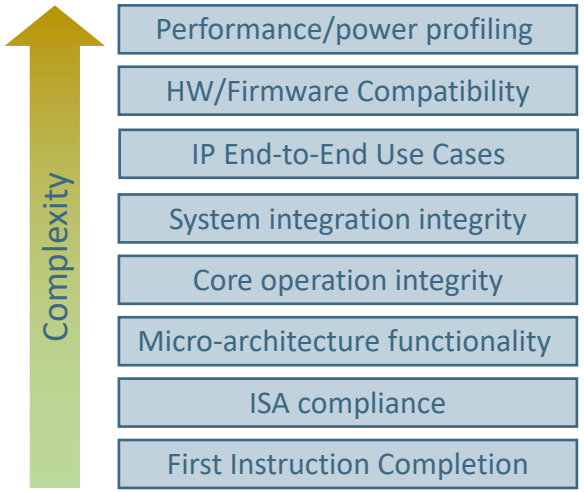
A Look At RISC-V

- Open Instruction Set Architecture (ISA) creating a discontinuity in the market
- Appears to be gaining significant traction in multiple applications
- Significant verification challenges
  - Arm spends $150M per year on 10^{15} verification cycles per core
  - Hard for RISC-V development group to achieve this same quality
  - Lots of applications expands verification requirements
  - Requires automation, reuse and other new thinking

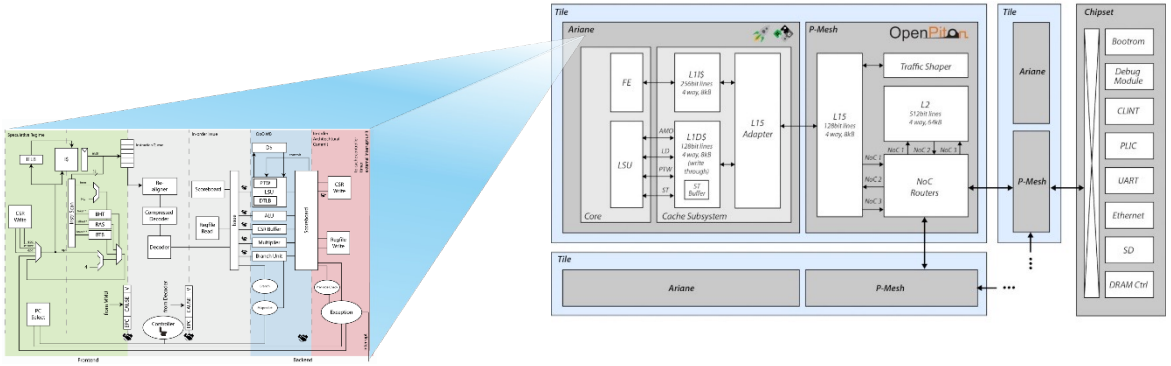
RISC-V Verification Challenges

- Processors are hard to verify
  - Consider Arm and Intel verification investments
- Automation is the answer
  - Number of diversified test generators, etc.
- RISC-V special requirements
  - Custom instruction verification
  - Compliance assurance
  - Broad range of architectures
- Different processors have different needs
  - Embedded cores
  - Processor clusters
  - Application processors

Suggested RISC-V verification "stack"



RISC-V Core vs SoC Verification Challenges



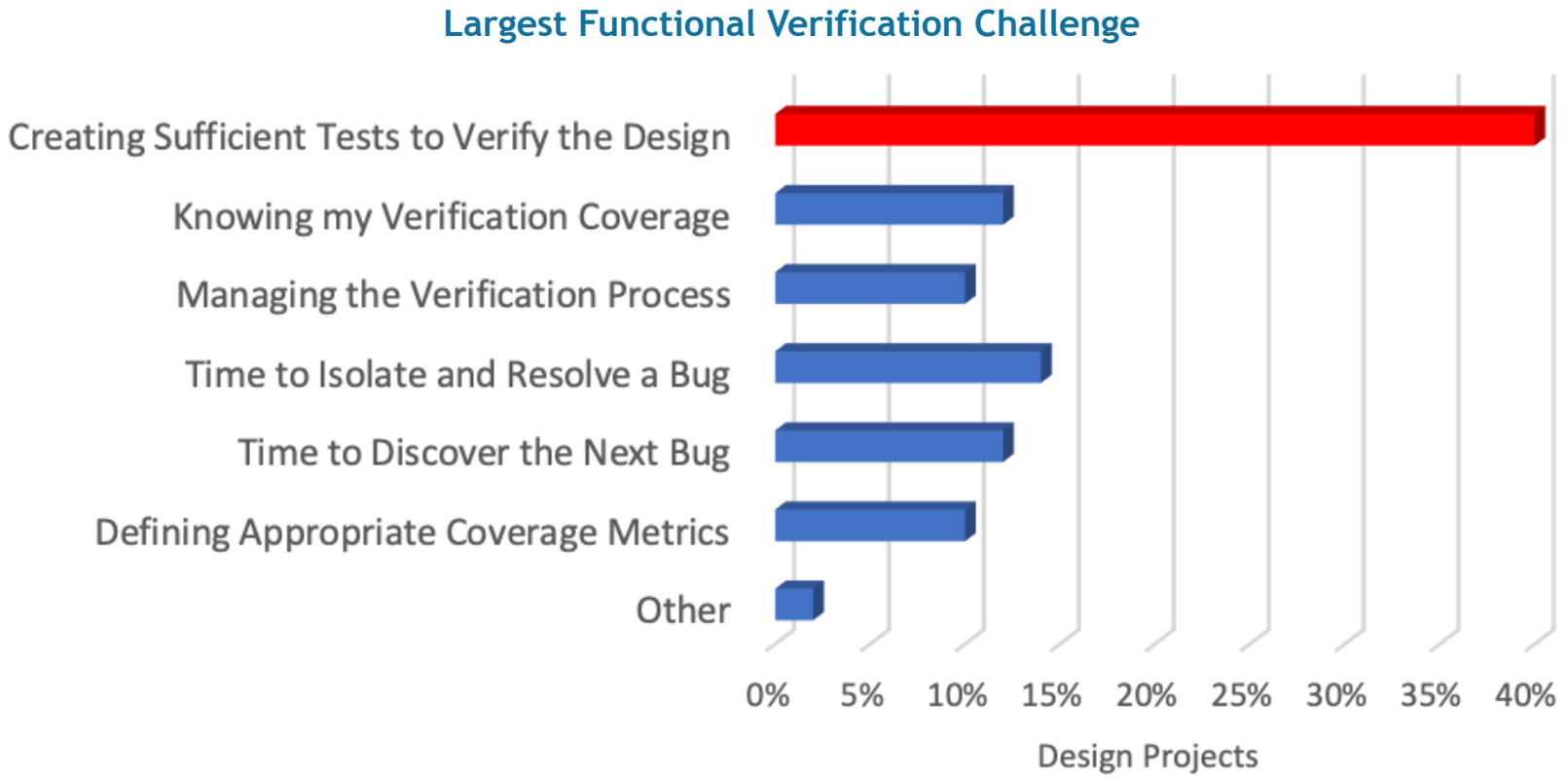
RISC-V Core Verification Challenges

Random Instructions	Do instructions yield correct results
Register/Register Hazards	Pipeline perturbations dues to register conflicts
Load/Store Integrity	Memory conflict patterns
Conditionals and Branches	Pipeline perturbations from synchronous PC change
Exceptions	Jumping to and returning from ISR
Asynchronous Interrupts	Pipeline perturbations from asynchronous PC change
Privilege Level Switching	Context switching
Core Security	Register and Memory protection by privilege level
Core Paging/MMU	Memory virtualization and TLB operation
Sleep/Wakeup	State retention across WFI
Voltage/Freq Scaling	Operation at different clock ratios
Core Coherency	Caches, evictions and snoops

RISC-V SoC Verification Challenges

System Coherency	Cover all cache transitions, evictions, snoops
System Paging/IOMMU	System memory virtualization
System Security	Register and Memory protection across system
Power Management	System wide sleep/wakeup and voltage/freq scaling
Packet Generation	Generating networking packets for I/O testing
Interface Testing	Analyzing coherent interfaces including CXL & UCIe
Random Memory Tests	Test Cores/Fabrics/Memory controllers across DDR, OCRAM, FLASH etc
Random Register Tests	Read/write test to all uncore registers
System Interrupts	Randomized interrupts through CLINT
Multi-core Execution	Concurrent operations on fabric and memory
Memory Ordering	For weakly order memory protocols
Atomic Operation	Across all memory types

Test Content Is The Number 1 Issue



Source: Wilson Research 2022

How can we improve this? Encapsulated, reusable, portable test libraries?

System Verification Tasks

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Complexity

Core Integrity

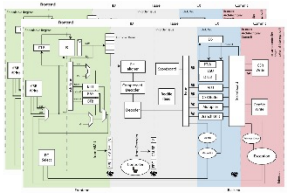
- Interrupts/Paging/Memory Order
- Micro-architecture functionality
- ISA compliance
- First Instruction Completion

Complexity

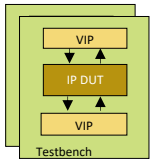
IP Integrity

- End-to-End Use Cases
- Concurrency Testing
- IP Configuration

CPU Cores



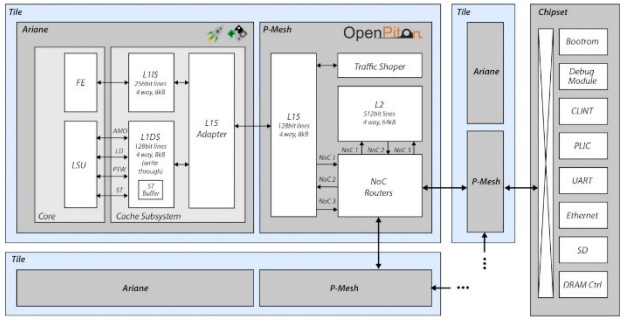
Uncore IPs



Complexity

SoC Integrity

- Power/Performance Profiling
- Security
- Power Management
- Interrupts/Paging/Memory Order
- Cache Coherency



Firmware

Firmware Integrity

- End-to-End Use Cases
- Concurrency Testing
- HW/Firmware Compatibility

Complexity

Breker SystemVIP Portfolio

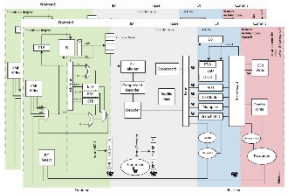
SVIPs for SoC Integrity

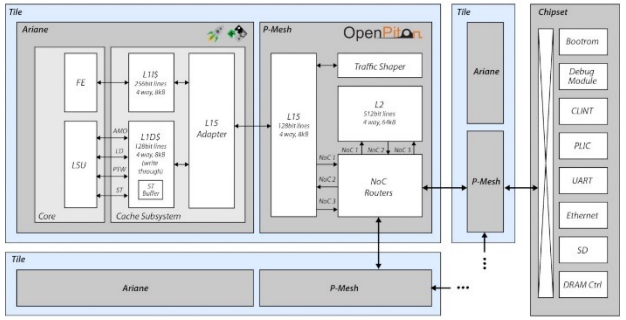
- SoC Cache Coherency
- Memory Ordering
- Power Management
- System Interrupts
- …

SVIPs for Core Integrity

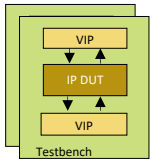
- Register Hazards
- Load/Store
- Core Cache Coherency
- Core Interrupts
- …

CPU Cores





Uncore IPs



Firmware

SVIPs for Firmware Integrity

- Mem2Mem (dma)
- IO Offload (PCIE/Eth)
- WQ Servicing
- …

SVIPs for IP Integrity

- Mem2Mem (dma)
- IO Offload (PCIE/Eth)
- WQ Servicing
- …

Enabling Modern Methodologies

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SVIPs for IP Integrity

- Mem2Mem (dma)
- IO Offload (PCIE/Eth)
- WQ Servicing
- …

SVIPs for Core Integrity

- Register Hazards
- Load/Store
- Core Cache Coherency
- Core Interrupts
- …

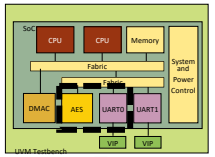
SVIPs for SoC Integrity

- SoC Cache Coherency
- Memory Ordering
- Power Management
- System Interrupts
- …

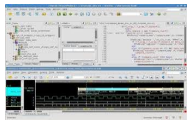
SVIPs for FW Integrity

- Mem2Mem (dma)
- IO Offload (PCIE/Eth)
- WQ Servicing
- …

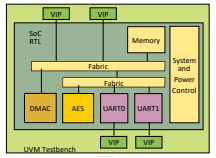
Test Suite Synthesis



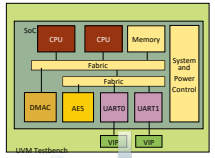
Virtual Platform Environment



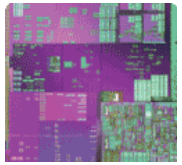
UVM Block Environment



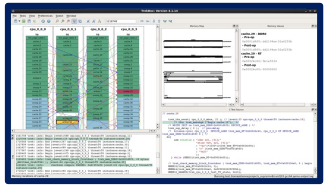
Simulation Acceleration



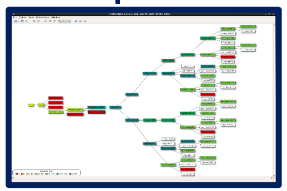
Hybrid Emulation Environment



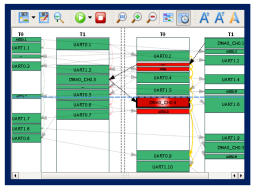
Silicon / Prototyping Environment



High Level Debug

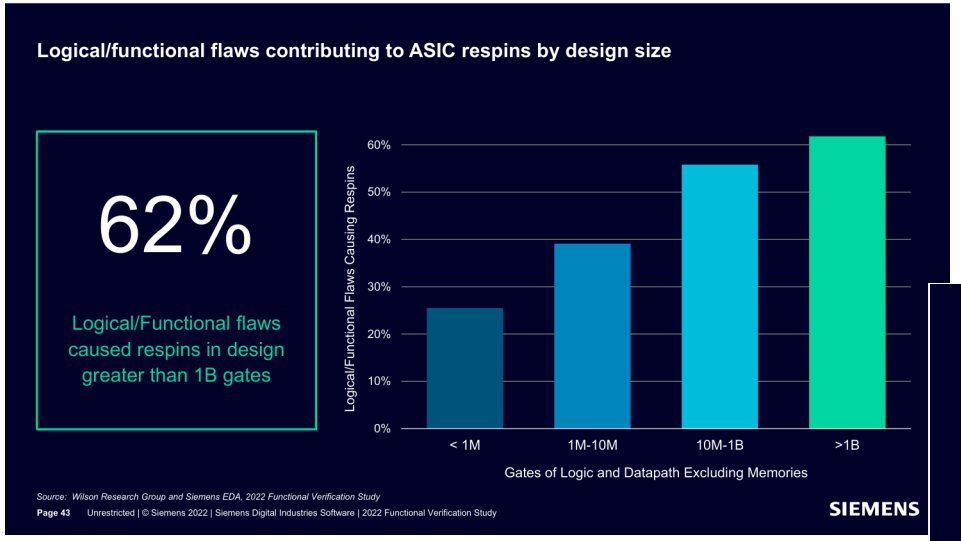


Coverage Analysis

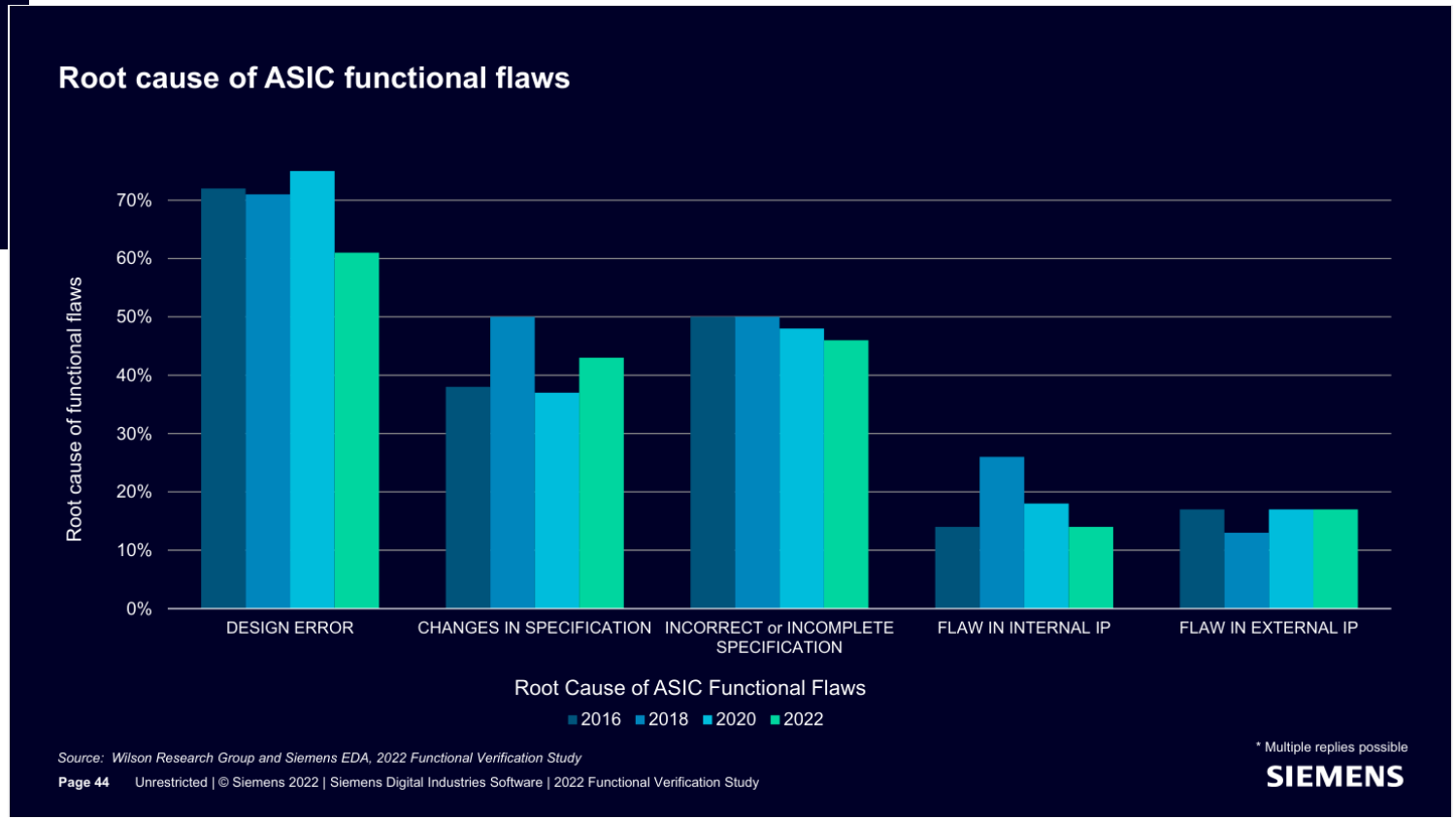


Performance Profiling

Do I Haaafta… ? What is the Business Risk ?

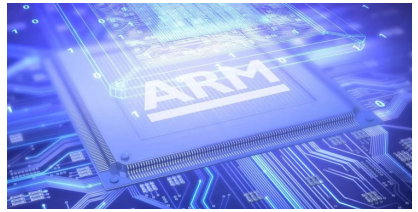


I've verified every block to exhaustion…

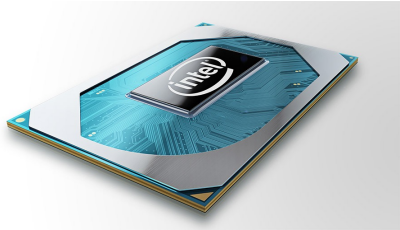


… how could the system possibly break?

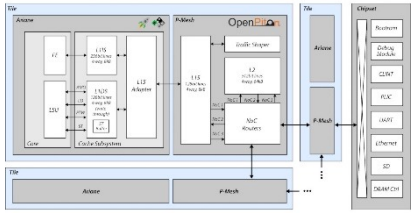
Why Breker ?



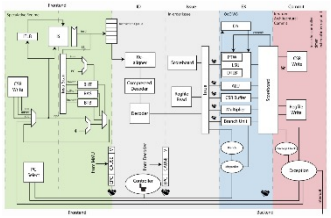
ArmV8 SoC



X86 SoC



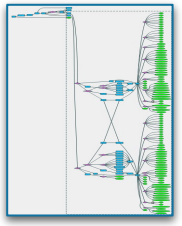
RISC-V SoC



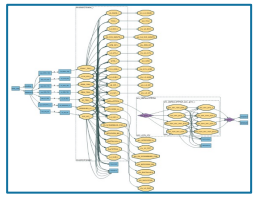
RISC-V Core

2011 — 2015 — 2019 — 2022

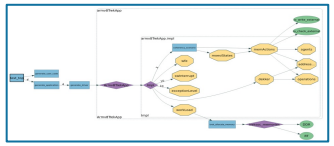
Breker Coherency TrekApp



Breker SoC TrekApps



Breker RISC-V FastApps



AI Planning Algorithm Techniques for RISC-V Test Synthesis

Test Suite Synthesis… Analogous to Logic Synthesis

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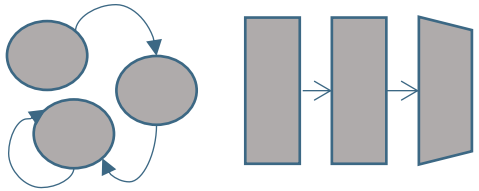
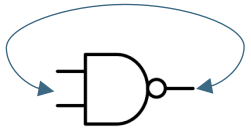
Design Synthesis

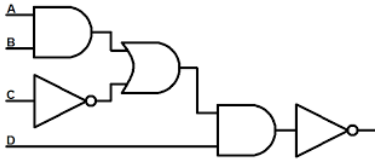


Constrain

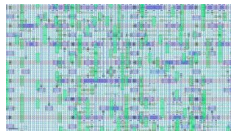


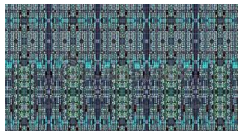
Timing/Area Constraints

Synthesize



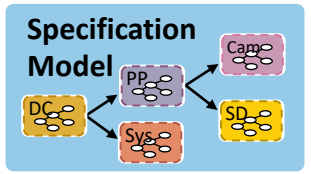
Optimize





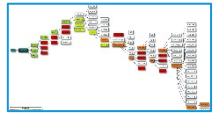
Test Suite Synthesis

Describe intent



Constrain

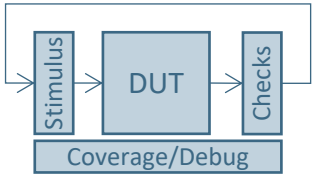
Specify goals



Coverage Constraints

Synthesize

Generate implementation



Optimize

Map to platform

Breker Core Technology

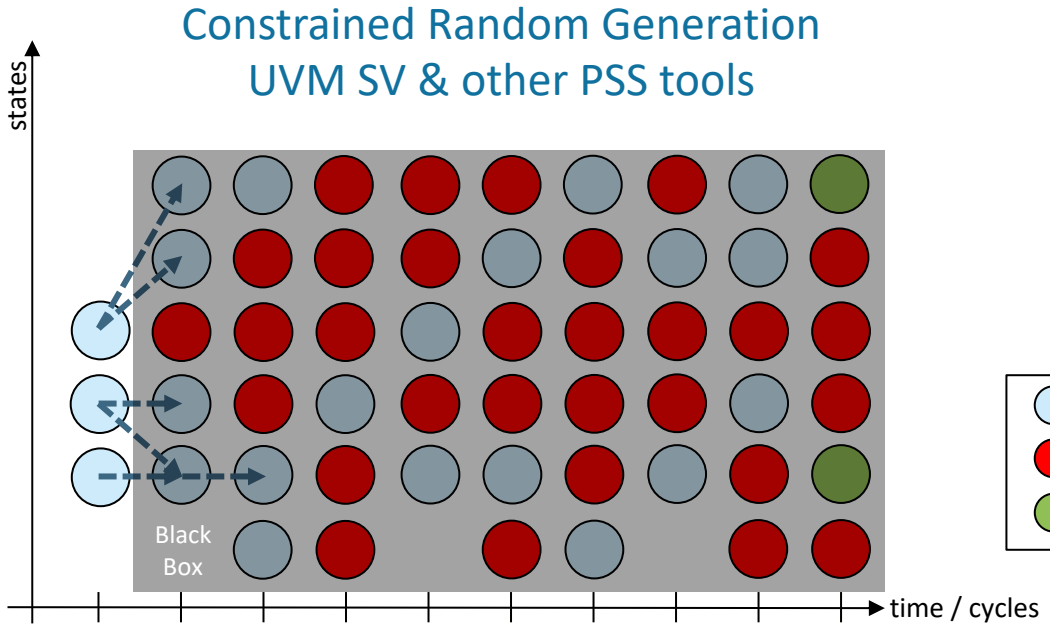
AI Planning Algorithms

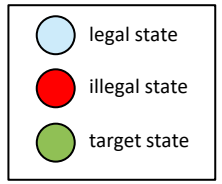
3D Coverage Closure

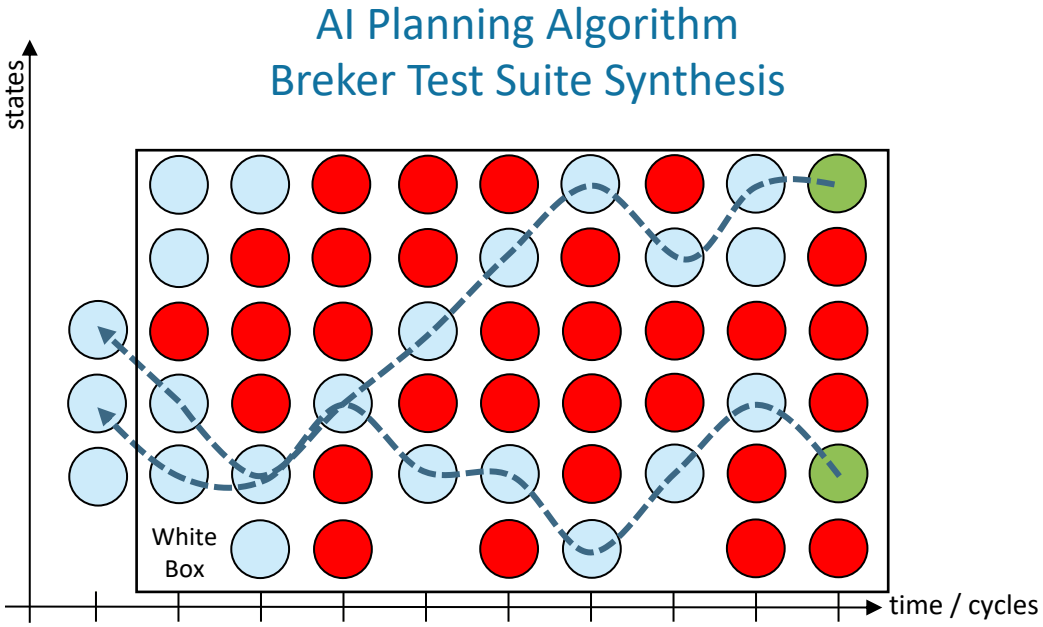
Synthesizable VerificationOS

AI Planning Algorithms

Constrained Random vs AI Planning Algorithm Synthesis







Design black box, shotgun tests to search for key state

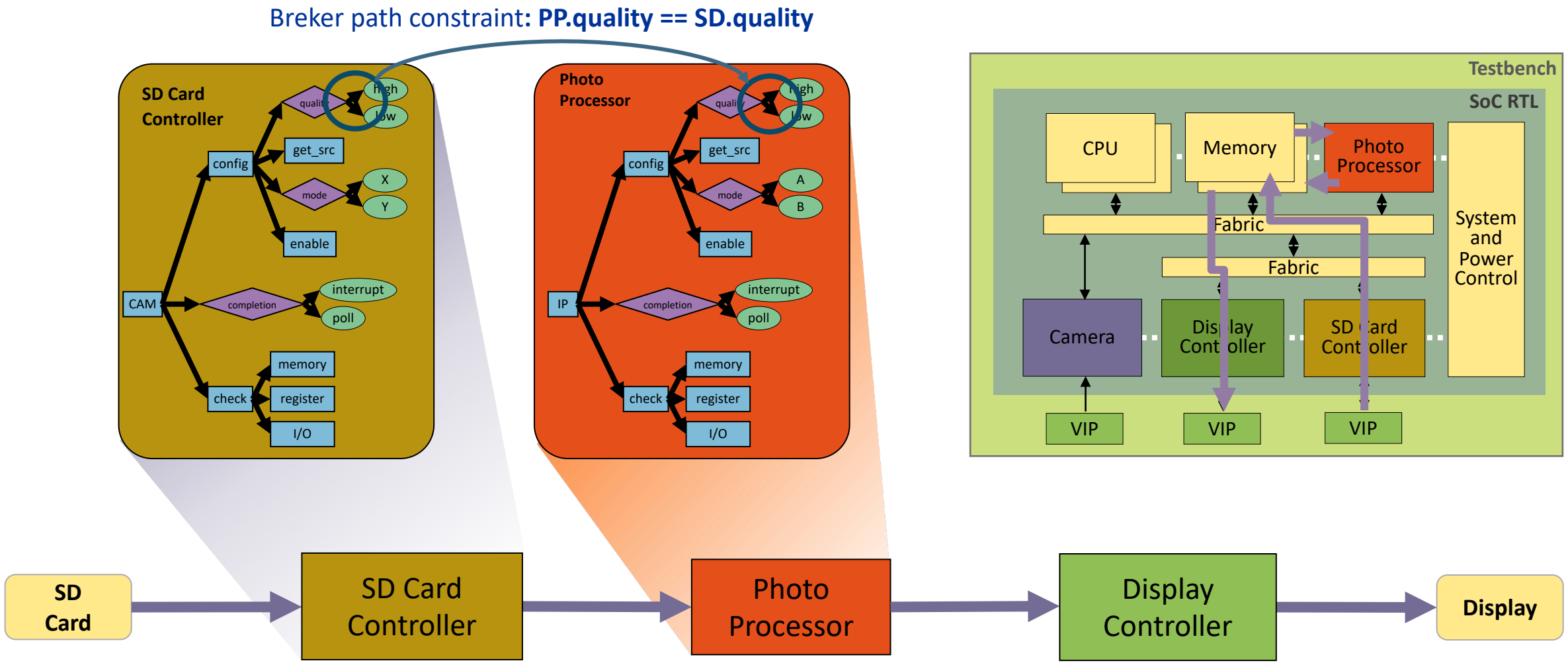
Low probability of finding complex bug

Starts with key state and intelligently works backward through space

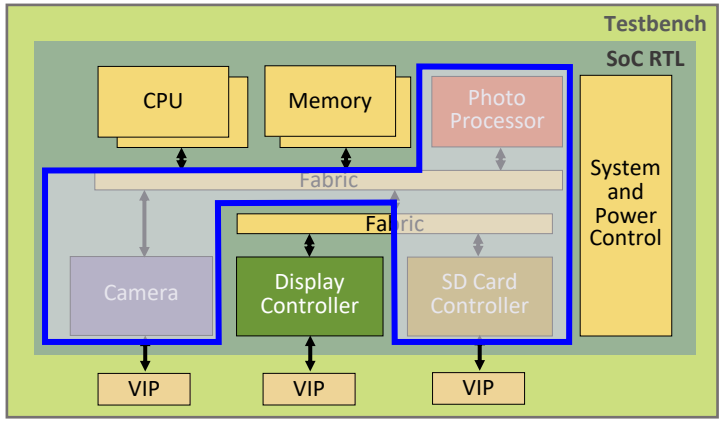
Deep sequential, optimized test discovers complex corner-cases

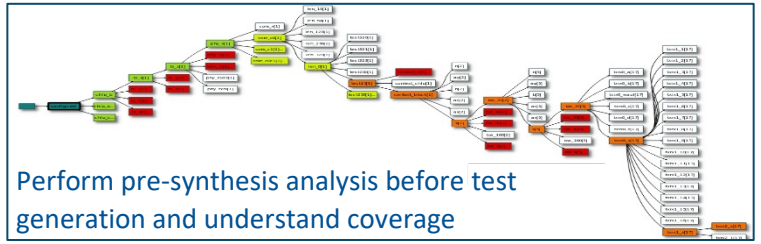
White Paper Discussing AI Planning Algorithm Test Generation on Breker Website

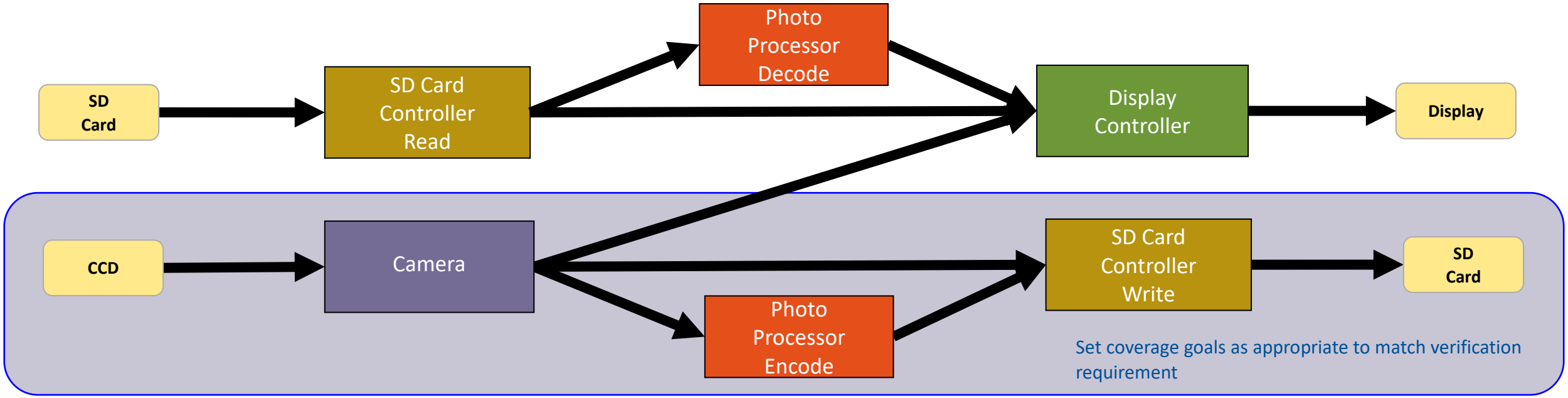
Digital Camera Application: Single Test Example



Digital Camera Application: Multiple tests

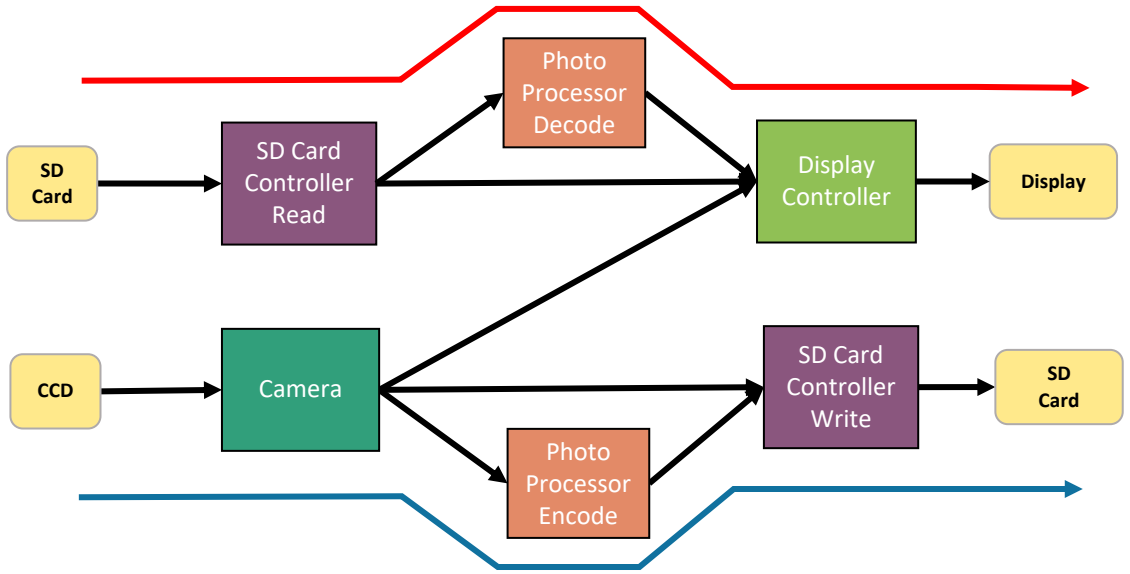


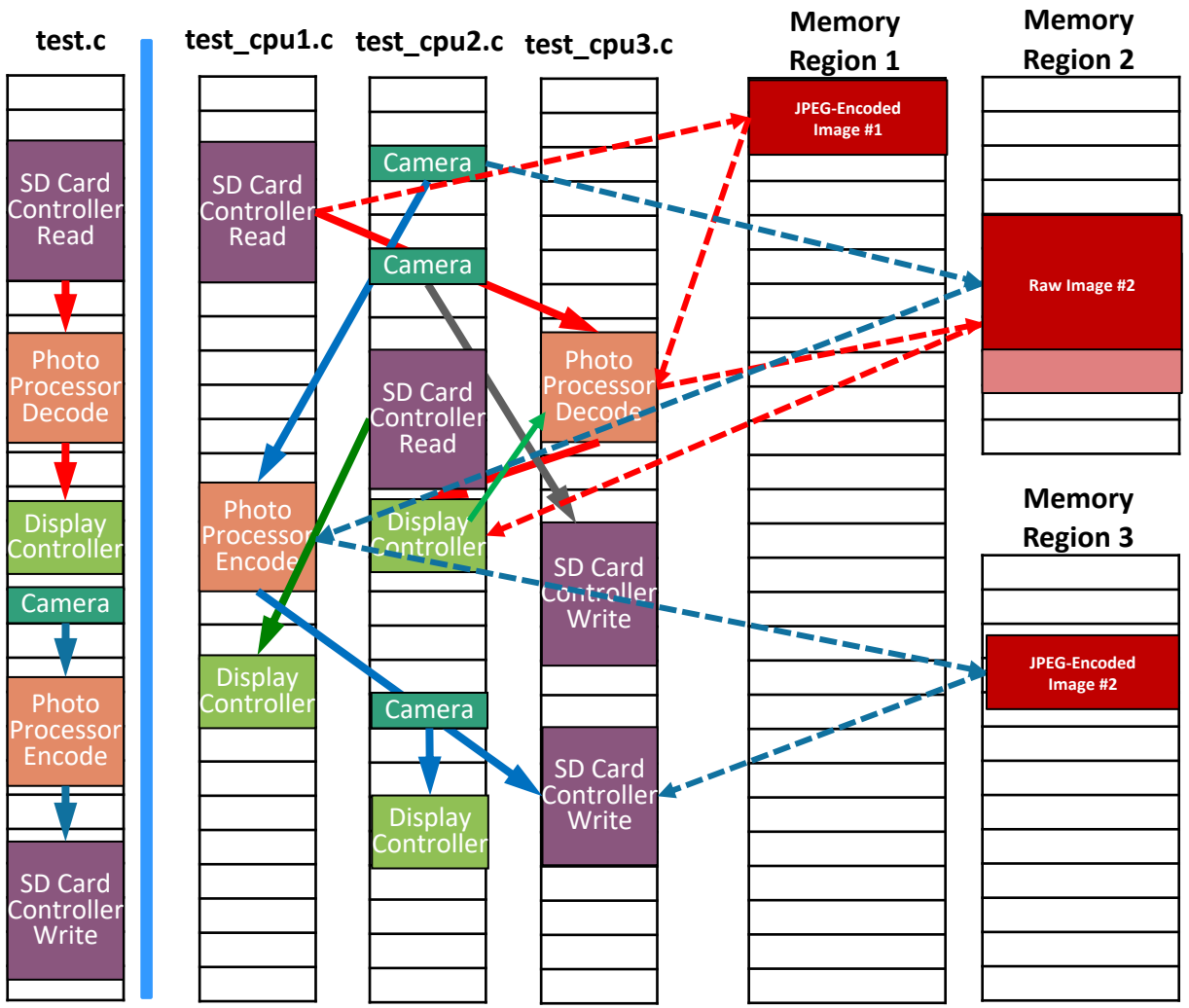




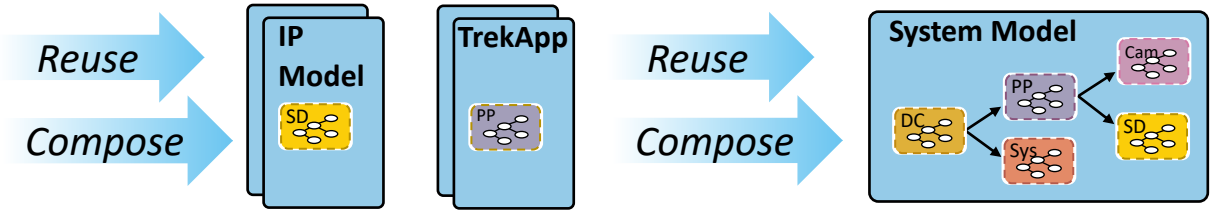
Tasks and Resource Scheduling

- Breker patented scheduling synthesis interleaves tests across resources
- Multi-memory scheduling and allocation uncovers complex SoC bugs
- Provides comprehensive SoC and UVM verification coverage, bug hunting

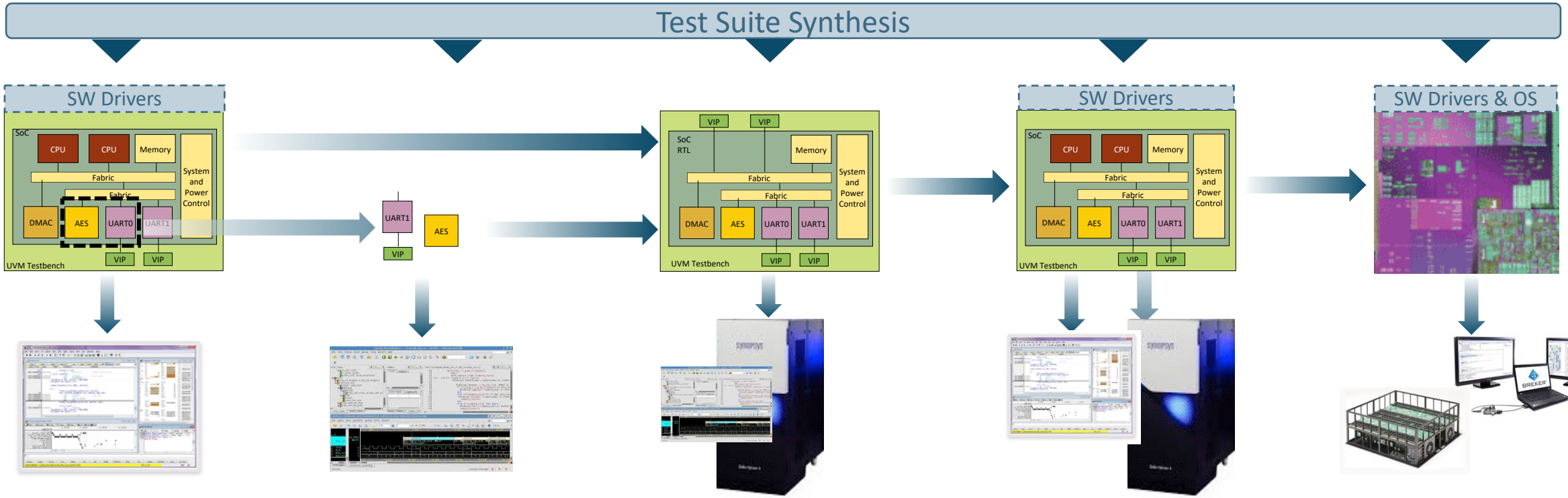




Target Platform Aware Test Suite Synthesis



Shift Left



Virtual Platform Environment

UVM Block Environment

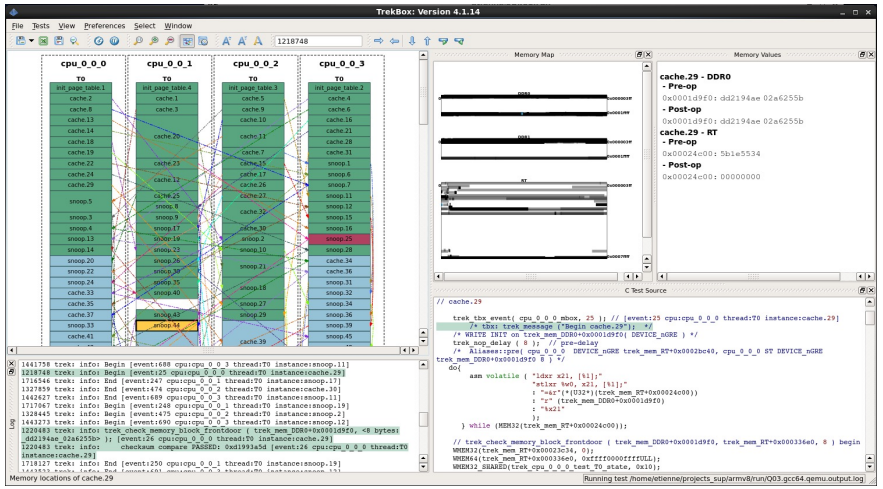
Simulation Acceleration

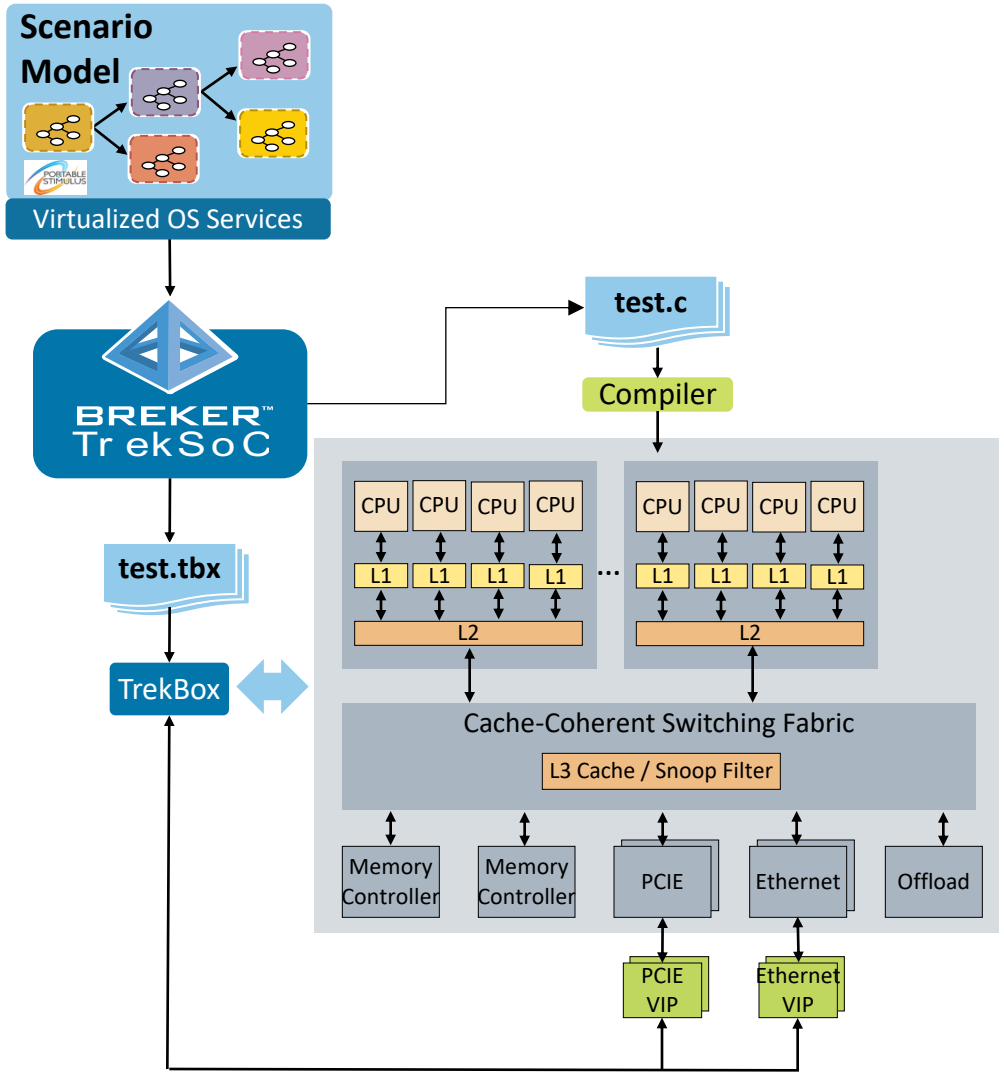
Hybrid Emulation Environment

Silicon / Prototyping Environment

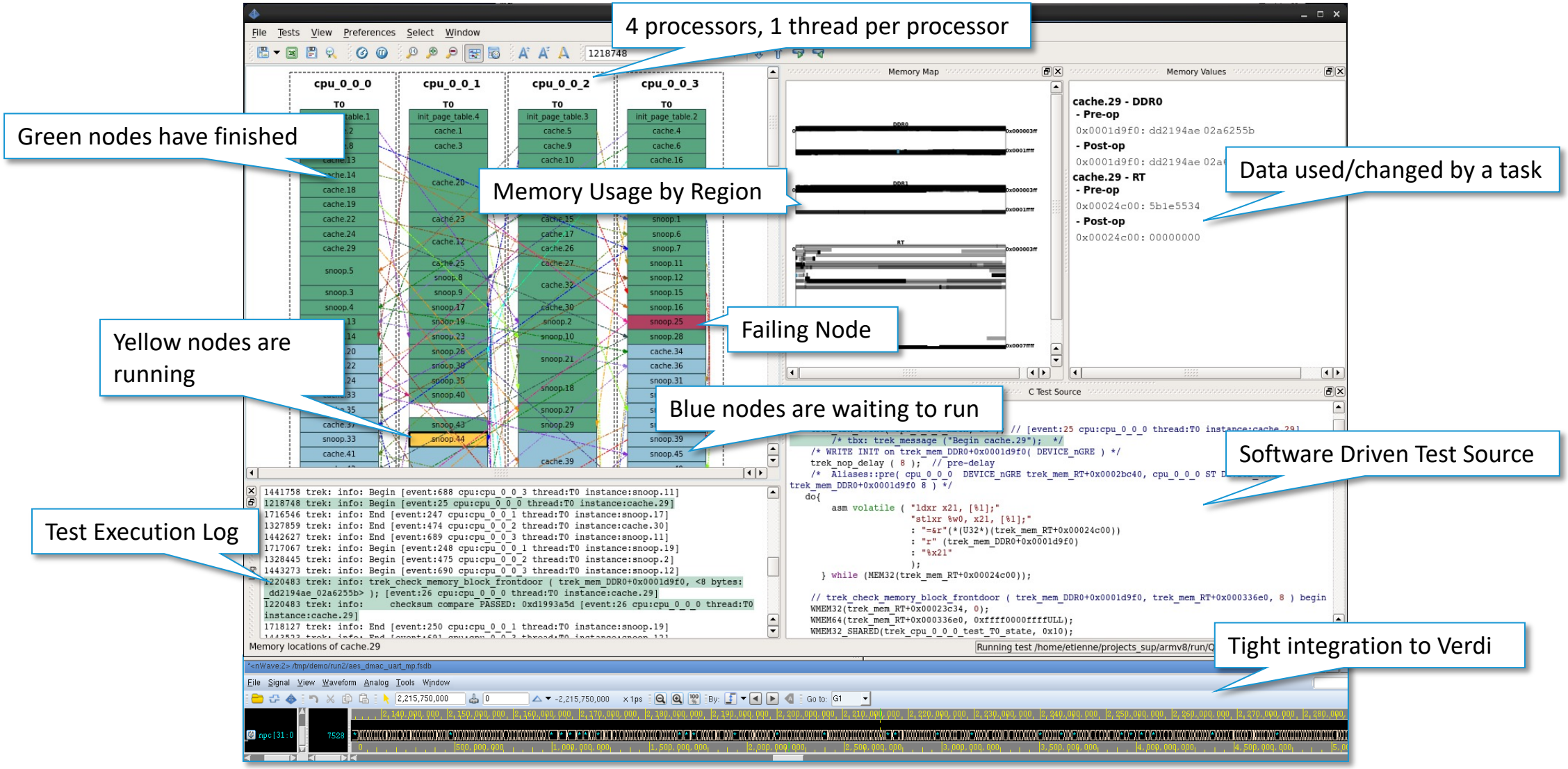
Software Driven Verification Flow

- Comprehensive tests synthesized from easy to understand spec to find corner-cases
- System services & apps save time, complexity: Memory mngt, hw/sw interface
- Verification, debug, profiling transparent across simulation & emulation (including Hybrid)

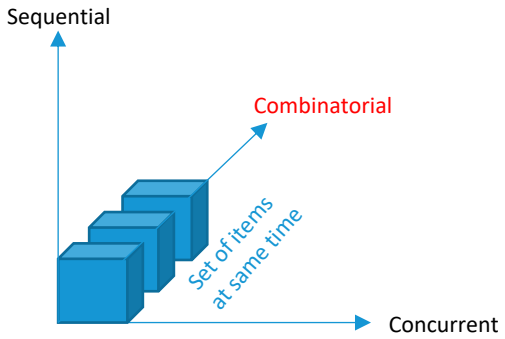


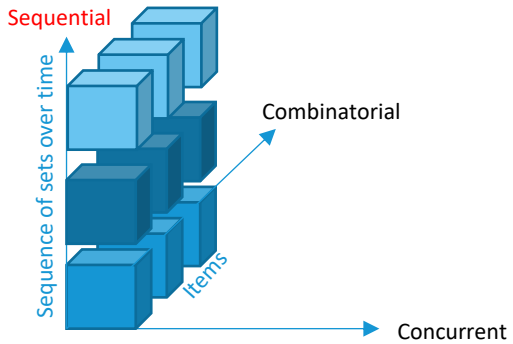


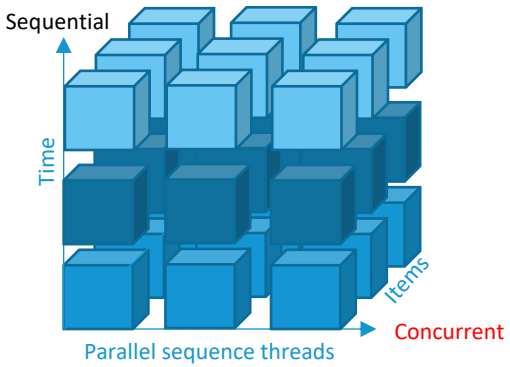
Synthesizing High-level Test Debug Info



Synthesizing 3D Coverage Analysis



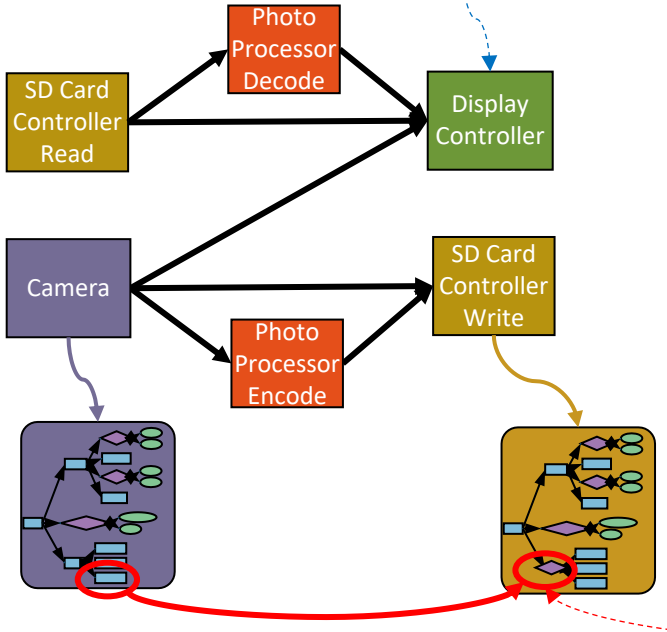


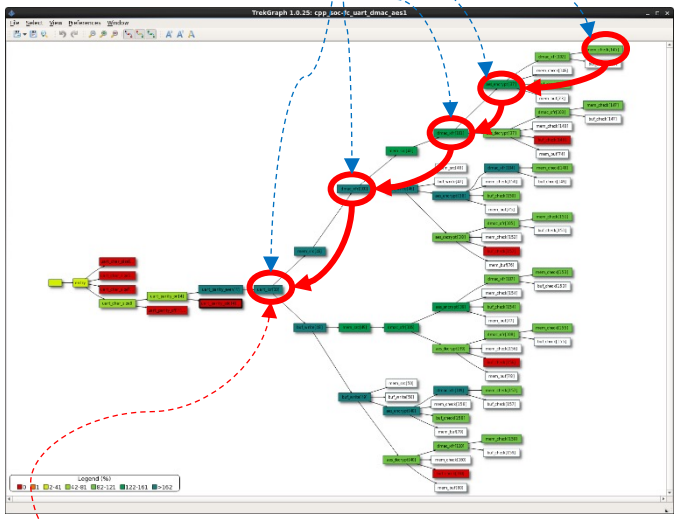


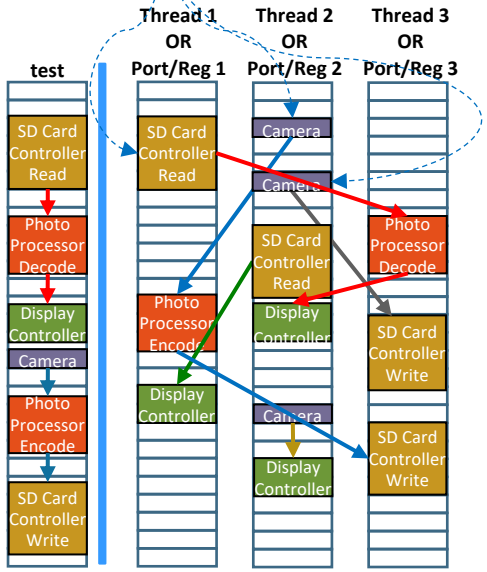
Combinatorial
Function been tested?

Sequential
Sequence of functions been tested?

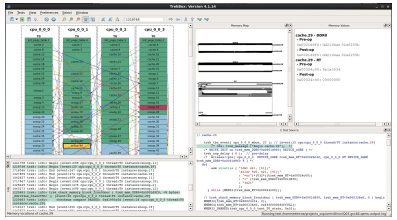
Concurrent
Has this timing combination been tested?







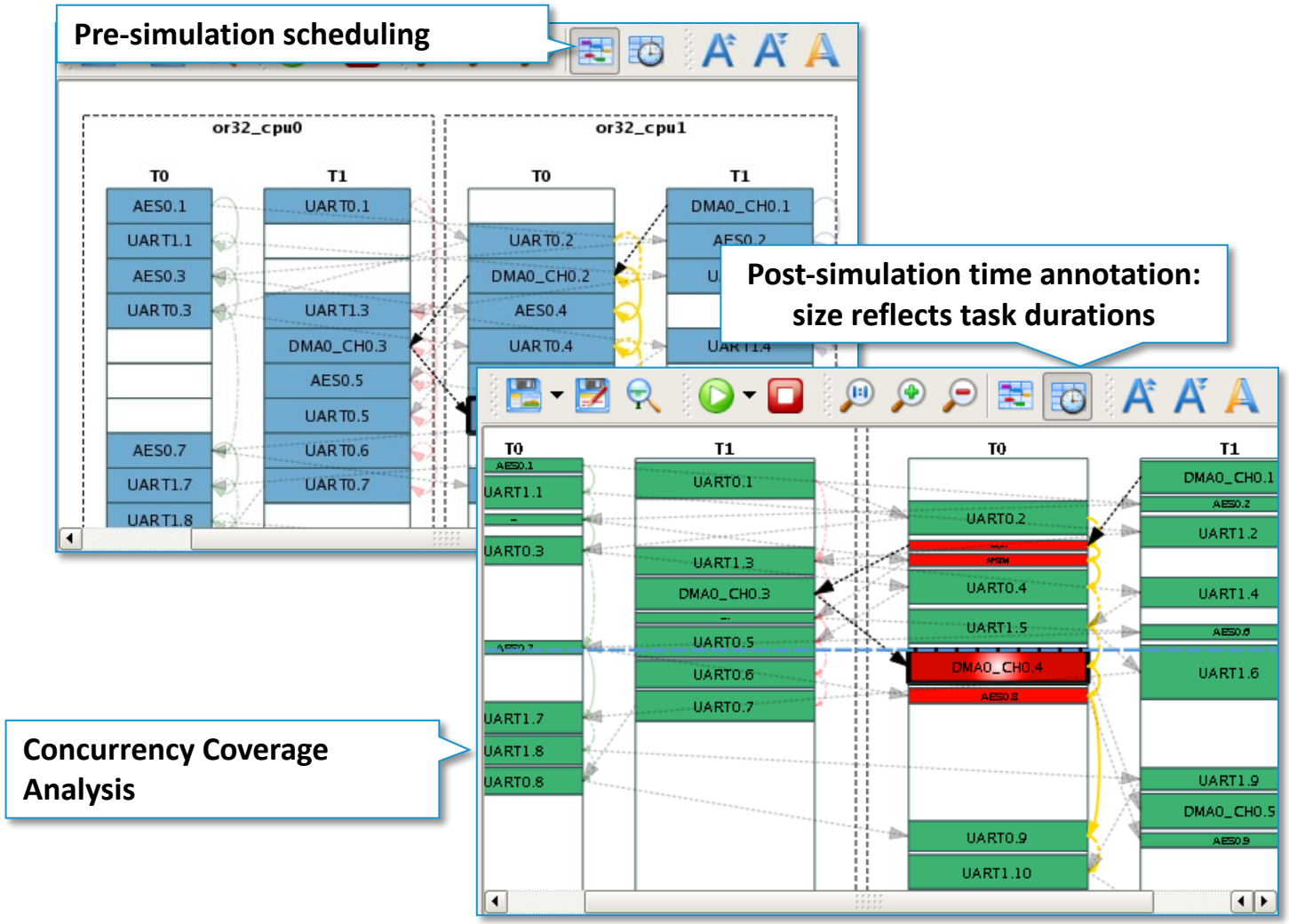
Debug & Profiling
Also needs to be in 3D



Path Constraint/Coverage

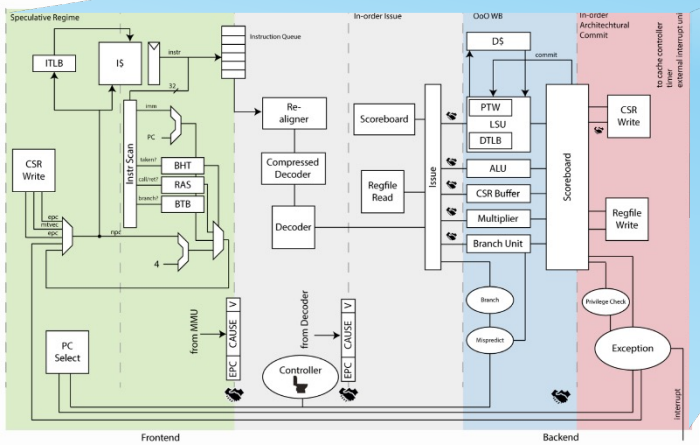
Synthesized Benchmarks & Performance Profiling

- Pre-simulation scheduling updated with post simulation temporal detail
- Test timing combined with scheduling synthesis tests for critical paths and bottlenecks
- Tracks unexpected timing at SoC level otherwise hard to find

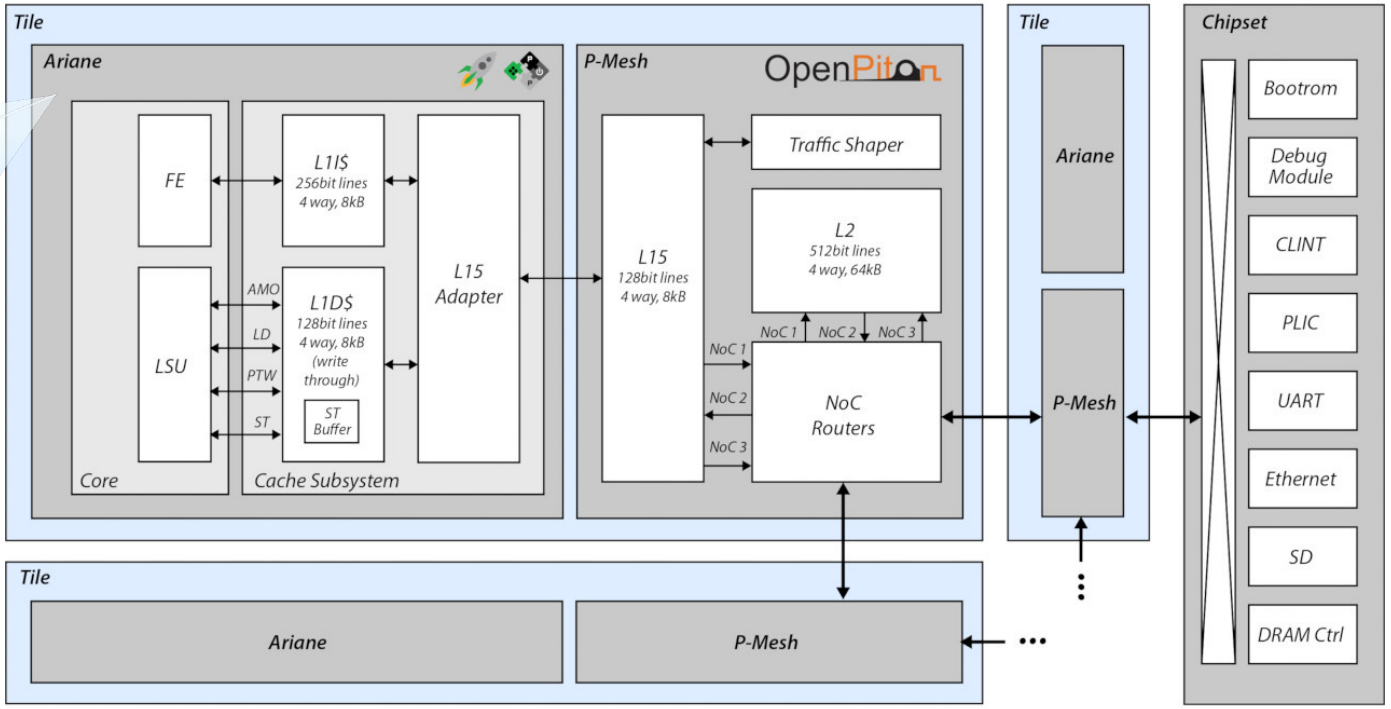


RISC-V Ariane/CVA6 Core & OpenPiton SoC

Ariane/CVA6 Core and OpenPiton SoC



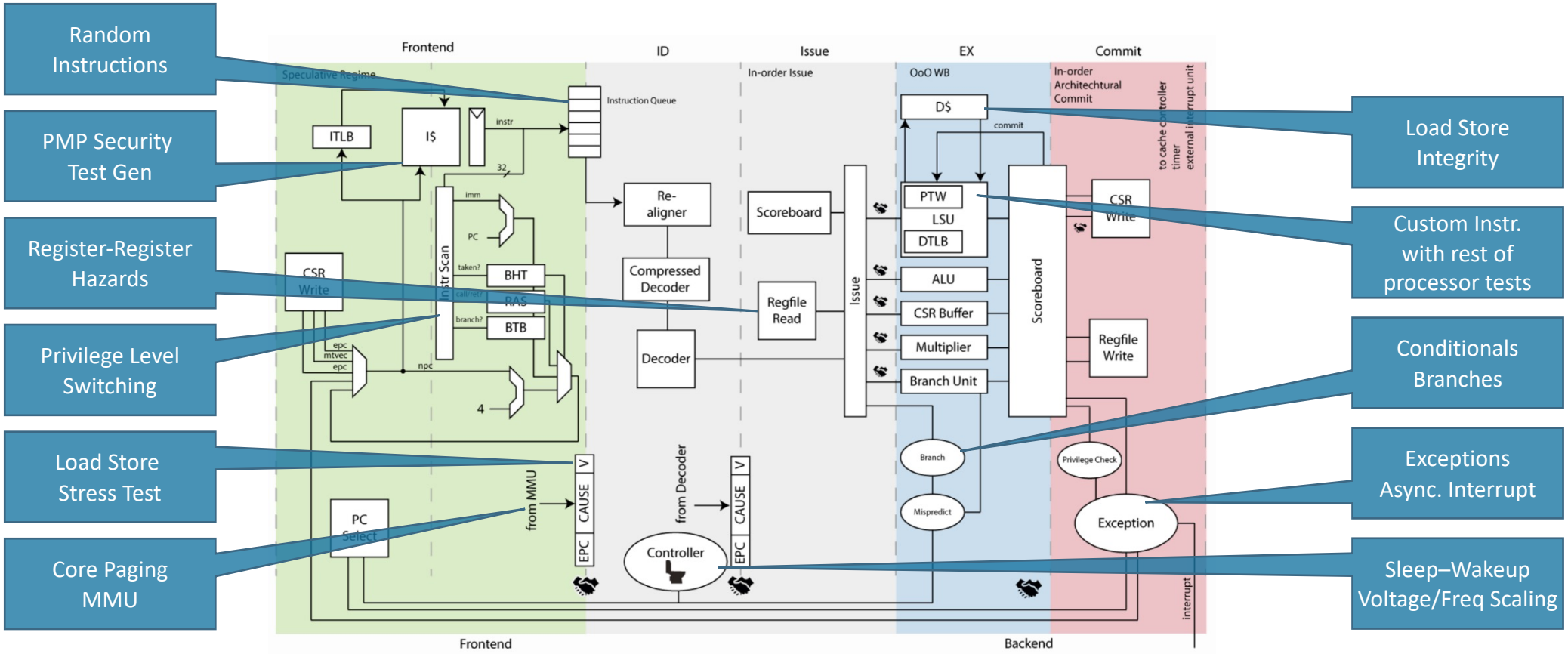
Ariane/CVA6 Core



OpenPiton SoC

RISC-V Core Integrity Test Synthesis

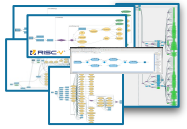
RISC-V Ariane/CVA6 Core Verification Objectives



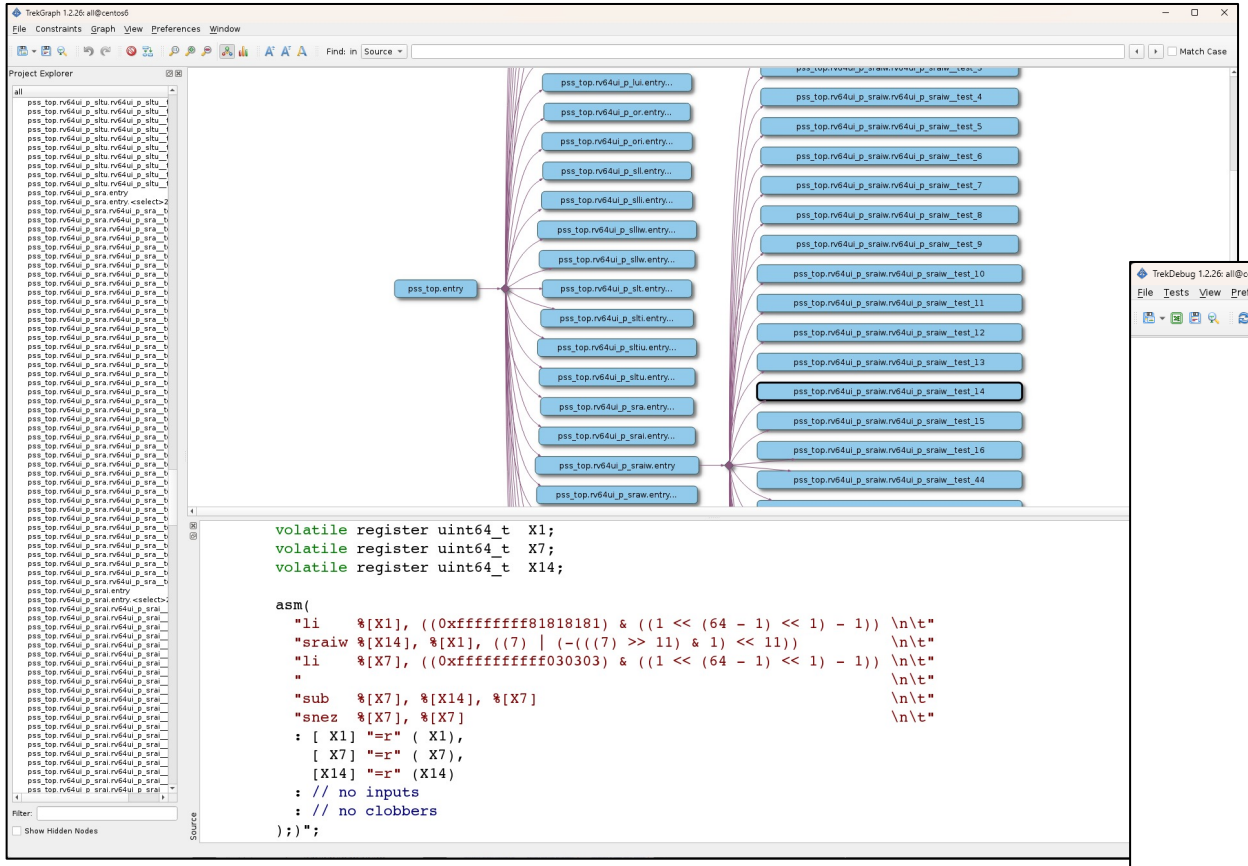
RISC-V Ariane/CVA6 Core “Verification Plan”

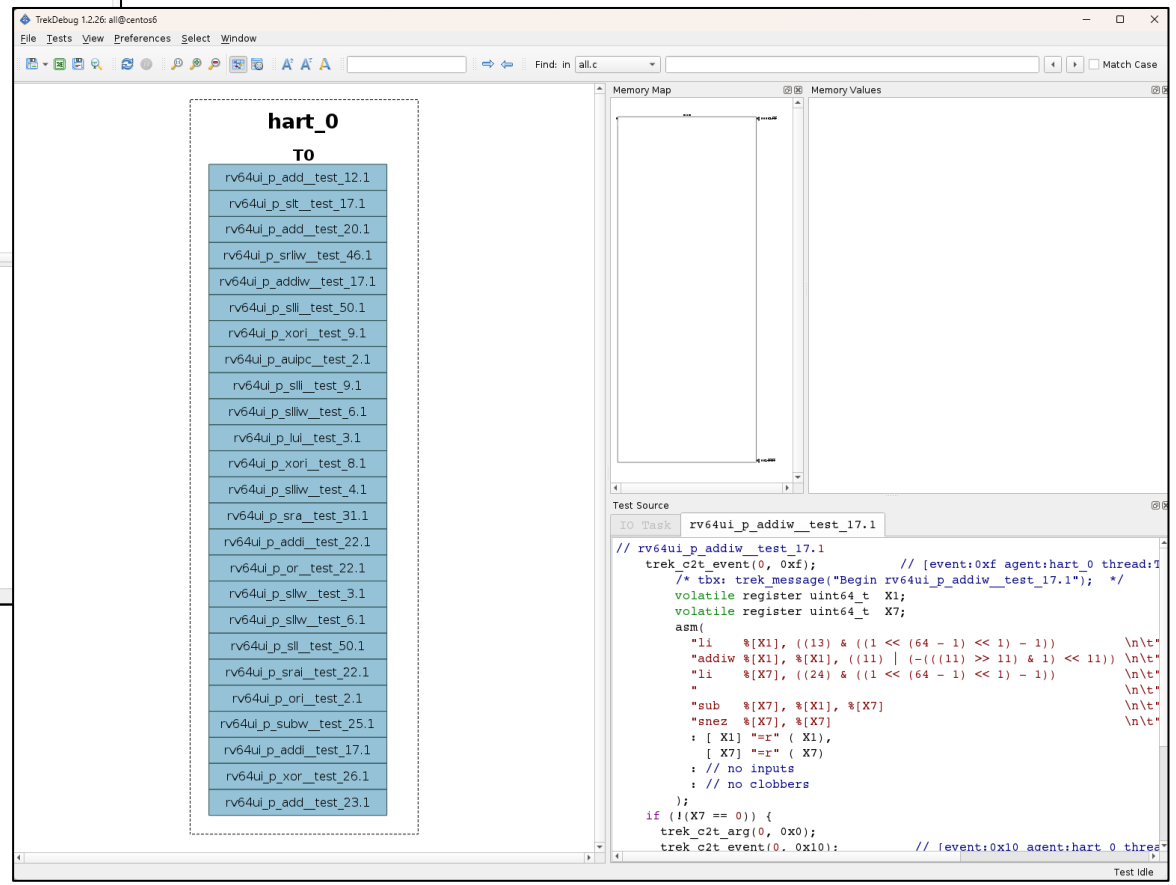
Random Instructions	Do instructions yield correct results
Register/Register Hazards	Pipeline perturbations dues to register conflicts
Load/Store Integrity	Memory conflict patterns
Conditionals and Branches	Pipeline perturbations from synchronous PC change
Exceptions	Jumping to and returning from ISR
Asynchronous Interrupts	Pipeline perturbations from asynchronous PC change
Privilege Level Switching	Context switching
Core Security	Register and Memory protection by privilege level
Core Paging/MMU	Memory virtualization and TLB operation
Sleep/Wakeup	State retention across WFI
Voltage/Freq Scaling	Operation at different clock ratios
Core Coherency	Caches, evictions and snoops

Breker
RISC-V Core-Integrity
SystemVIP



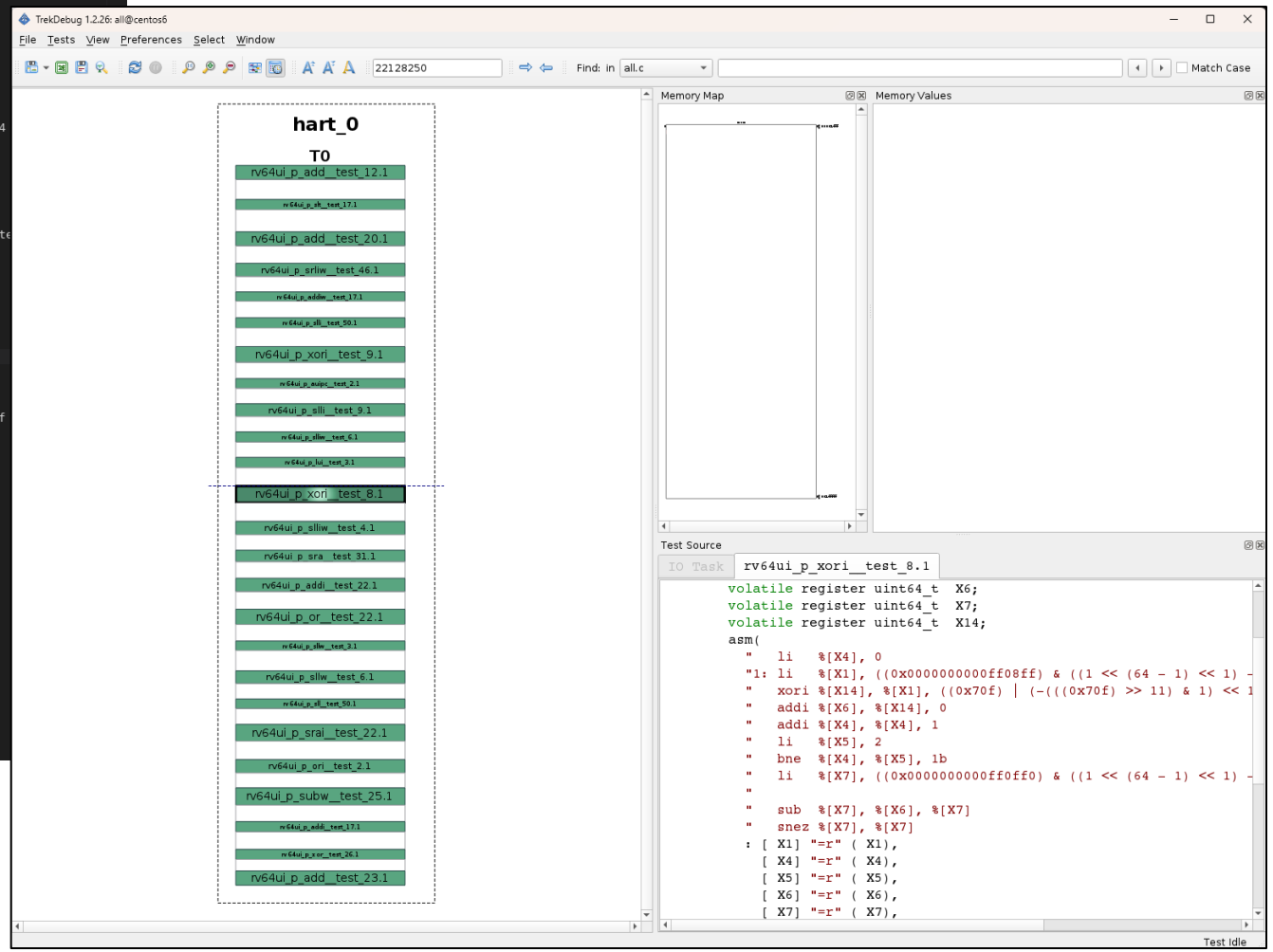
RISC-V Compatibility Tests Model + Synthesized Test





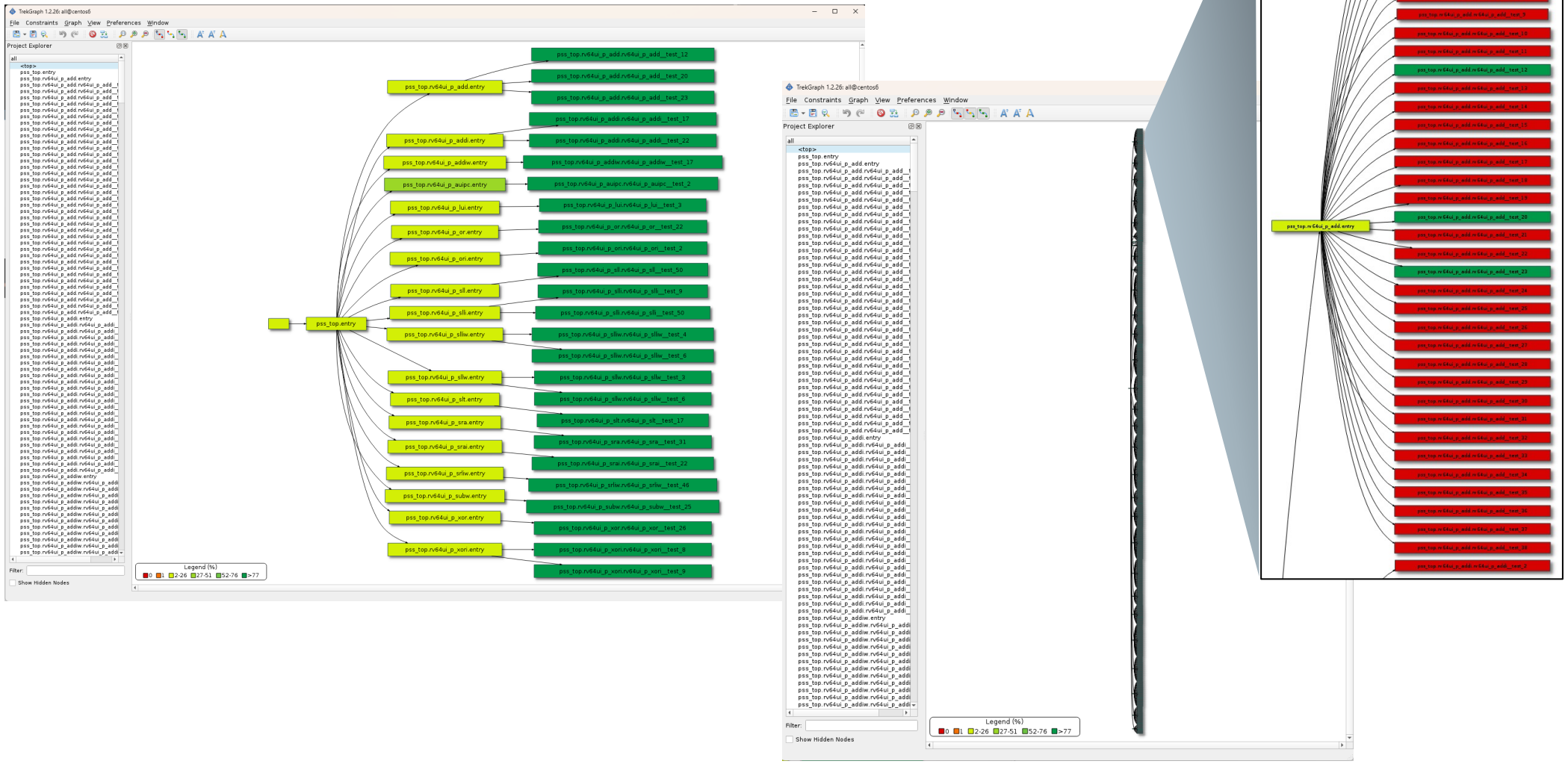
RISC-V Compatibility Tests Run & Timing Back-Annotation

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_args=+TREK_TBX_FILE=all.tbx all.c
sims: ====================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ====================================================
sims: ====================================================
sims:   Simulation Script for OpenSPARC T1
sims:   Copyright (c) 2001-2006 Sun Microsystems, Inc.
sims:   All rights reserved.
sims: ====================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SMP Fri Jan 27 02:56:13 UTC 2023 x86_64
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openpiton/x1y1-all
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verification Systems www.brekersystems.com
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00010001
IOB sending to tile X:  0 Y:  0
   raw tileid 00000000
16607500 TILE0 L1.5 th0: Received PCX PCX_REQTYPE_IFILL   Addr 0xfff1010000, nc 1, size 3, invalall 0, pf
 0, l1way 0
   Data: 0x0000000000000000
   CSM HDID:    0, HD_SIZE:  0, SDID:    0, LSID:  0
   CSM Data: 0x000000000

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```

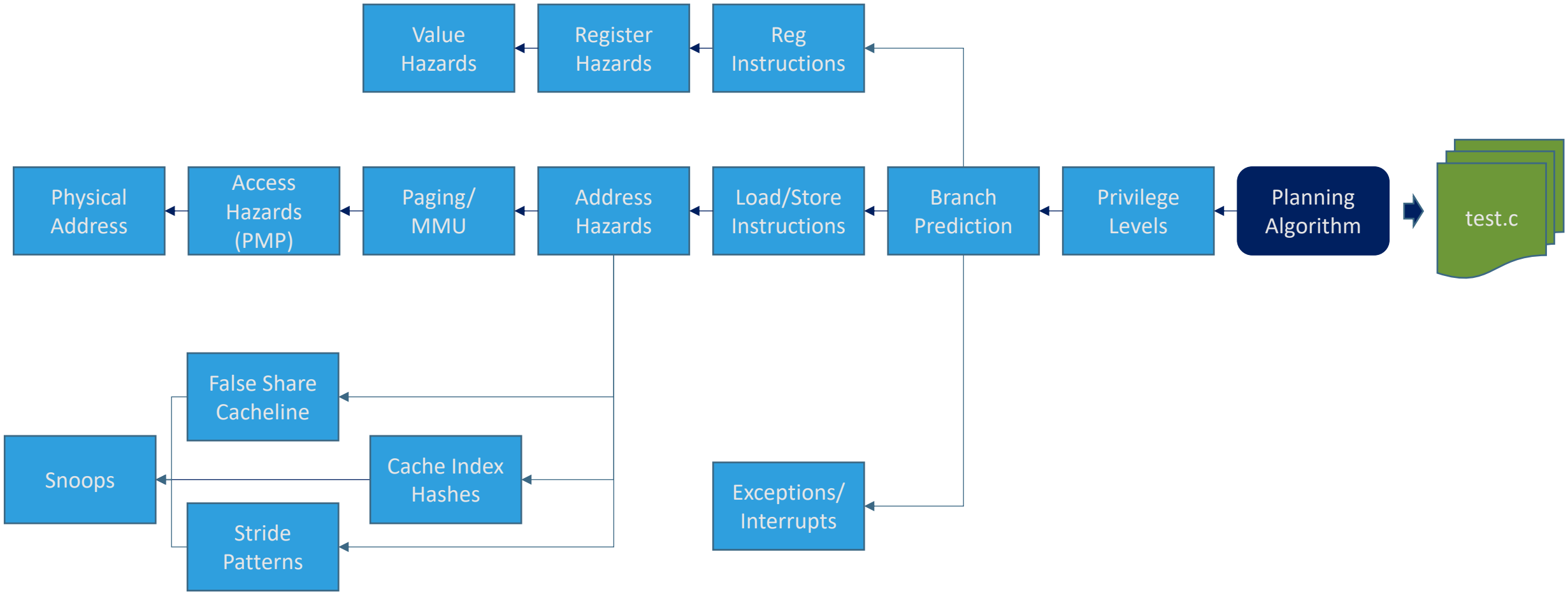


RISC-V Compatibility Tests Path Coverage

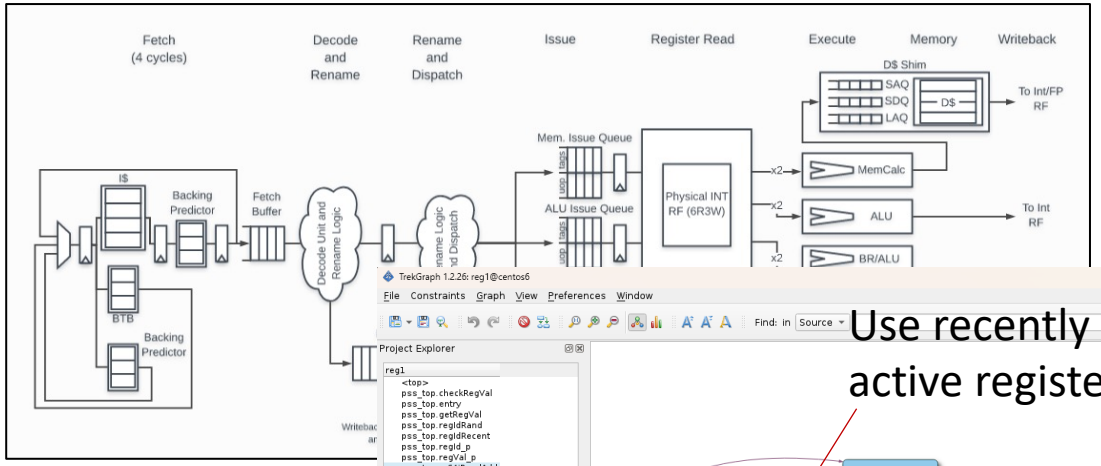
```
trek: info: analyzing coverage...
trek: info: total hits:25 total paths:870 reachable paths:870 satisfied paths:25
```



RISC-V Core Verification Planning Strategies



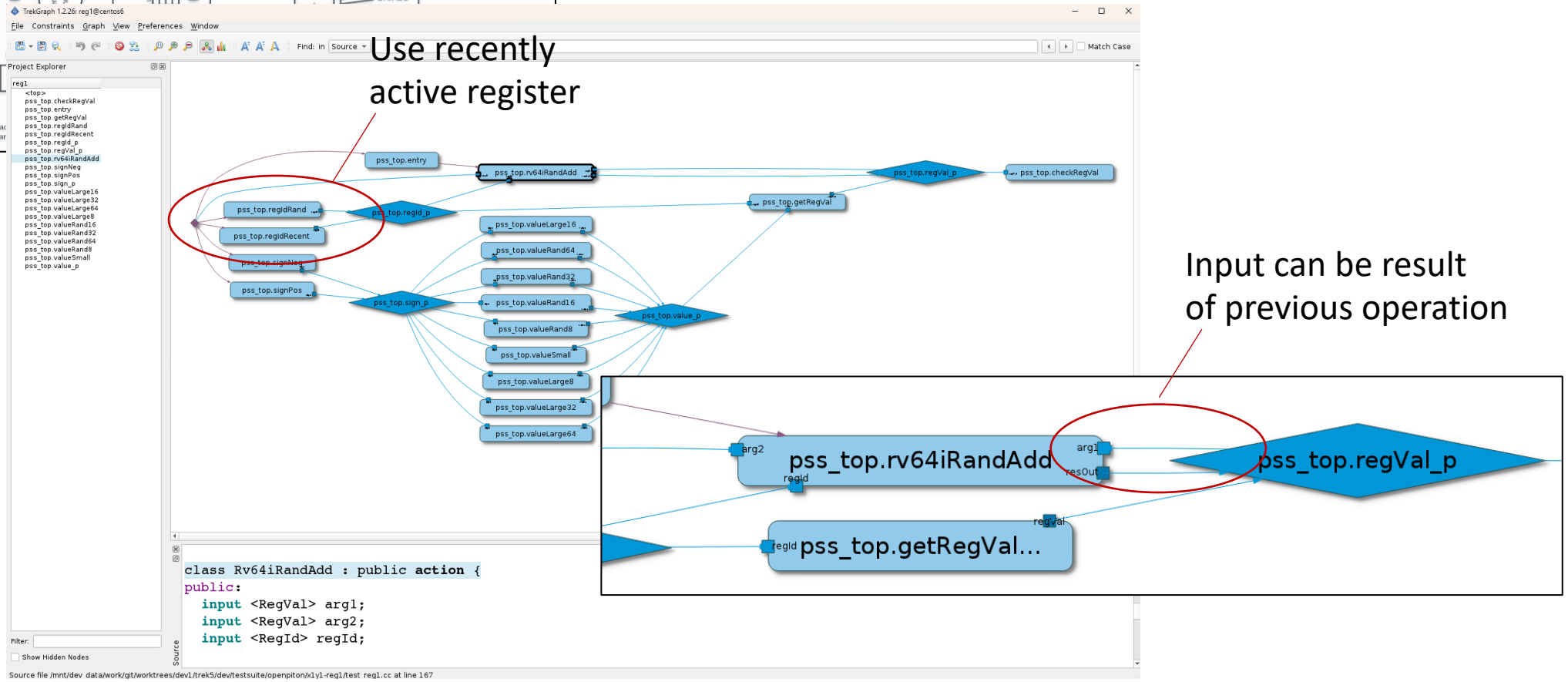
RISC-V Register Hazards Model



Hazard between read from stage N and write from stage N+m

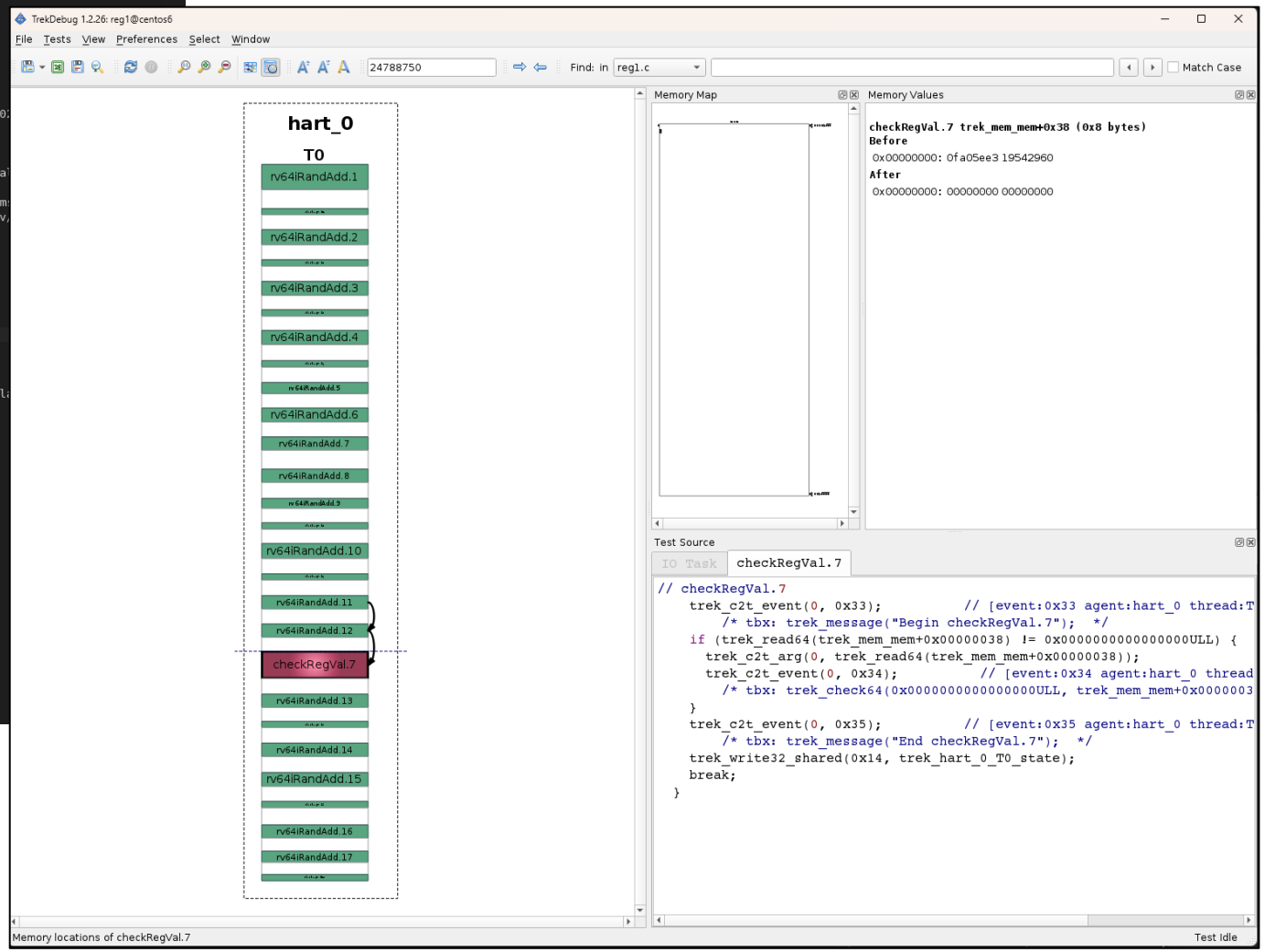
Use recently active register

Input can be result of previous operation



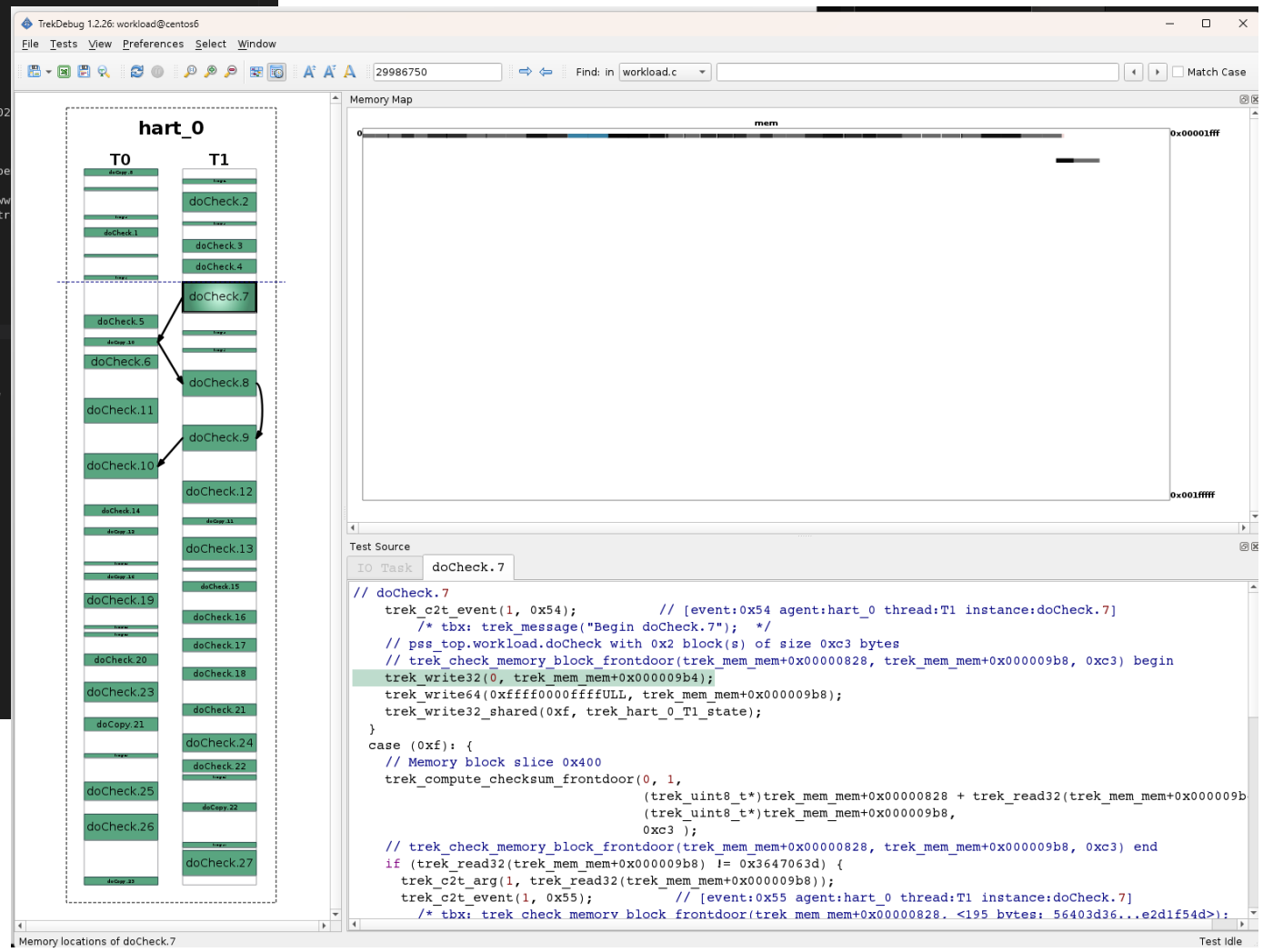
RISC-V Register Hazards Failure Debug

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_args=+TREK_TBX_FILE=all.tbx all.c
sims: ====================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ====================================================
sims: ====================================================
sims:   Simulation Script for OpenSPARC T1
sims:   Copyright (c) 2001-2006 Sun Microsystems, Inc.
sims:   All rights reserved.
sims: ====================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SMP Fri Jan 27 02:56:13 UTC 20
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openpiton/x1y1-a
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verification Systems www.brekersystem
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00010001
IOB sending to tile X:  0 Y:  0
   raw tileid 00000000
16607500 TILE0 L1.5 th0: Received PCX PCX_REQTYPE_IFILL   Addr 0xfff1010000, nc 1, size 3, inval
 0, l1way 0
   Data: 0x0000000000000000
   CSM HDID:    0, HD_SIZE:  0, SDID:    0, LSID:  0
   CSM Data: 0x000000000

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```



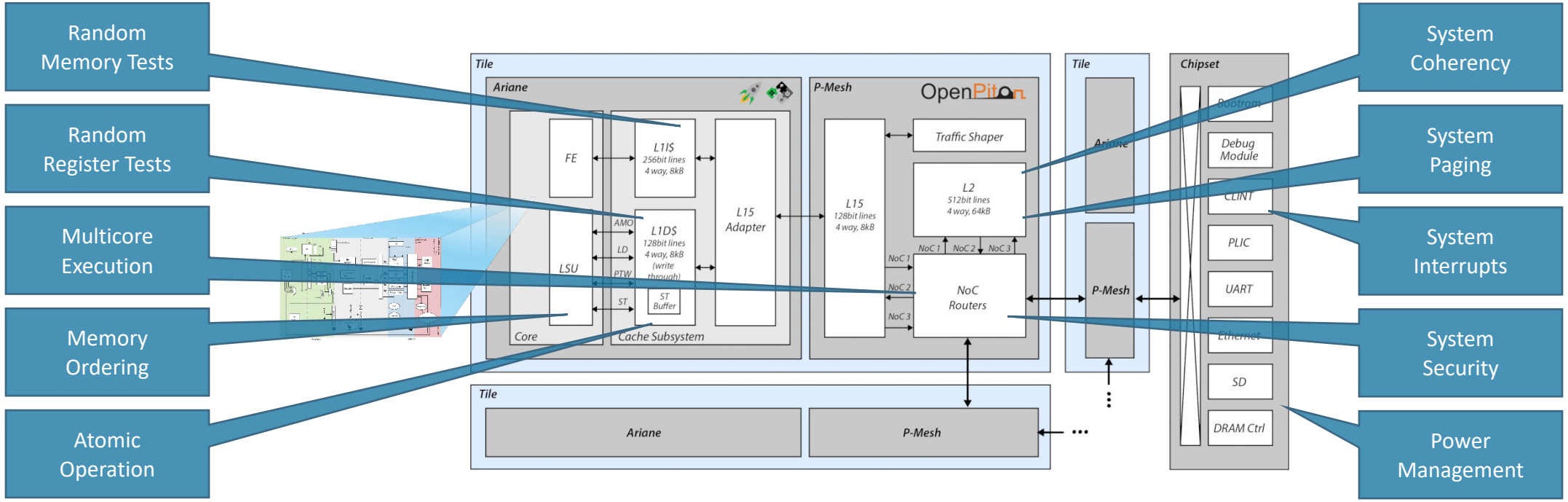
RISCV Memory Hazards: Timing Back-Annotation

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_args=+TREK_TBX_FILE=all.tbx all.c
sims: ==================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ==================================================
sims: ==================================================
sims:   Simulation Script for OpenSPARC T1
sims:   Copyright (c) 2001-2006 Sun Microsystems, Inc.
sims:   All rights reserved.
sims: ==================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SMP Fri Jan 27 02
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/ope
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verification Systems www
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/worktrees/dev1/tr
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00010001
IOB sending to tile X:  0 Y:  0
   raw tileid 00000000
16607500 TILE0 L1.5 th0: Received PCX PCX_REQTYPE_IFILL   Addr 0xfff1010000, nc 1,
 0, l1way 0
   Data: 0x0000000000000000
   CSM HDID:    0, HD_SIZE:  0, SDID:    0, LSID:  0
   CSM Data: 0x000000000

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```



RISC-V SoC Integrity Test Synthesis

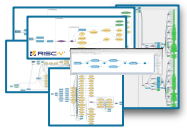
RISC-V OpenPiton SoC Verification Objectives



RISC-V OpenPiton SoC "Verification Plan"

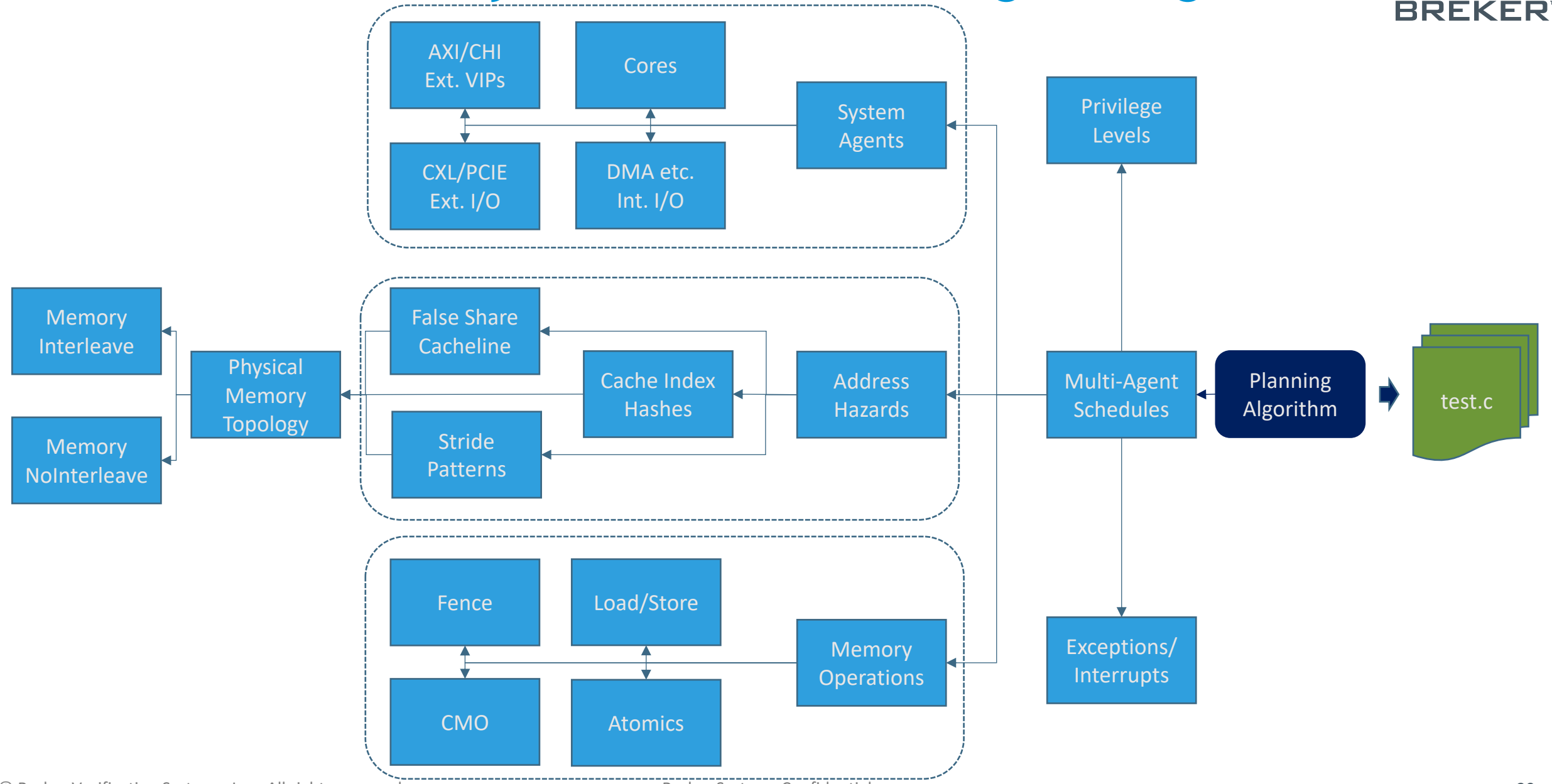
Random Memory Tests	Test Cores/Fabrics/Memory controllers across DDR, OCRAM, FLASH etc
Random Register Tests	Read/write test to all uncore registers
System Interrupts	Randomized interrupts through CLINT
Multi-core execution	Concurrent operations on fabric and memory
Memory ordering	For weakly order memory protocols
Atomic operation	Across all memory types
System Coherency	Cover all cache transitions, evictions, snoops
System Paging/IOMMU	System memory virtualization
System Security	Register and Memory protection across system
Power Management	System wide sleep/wakeup and voltage/freq scaling

Breker
RISC-V SoC-Integrity
SystemVIP

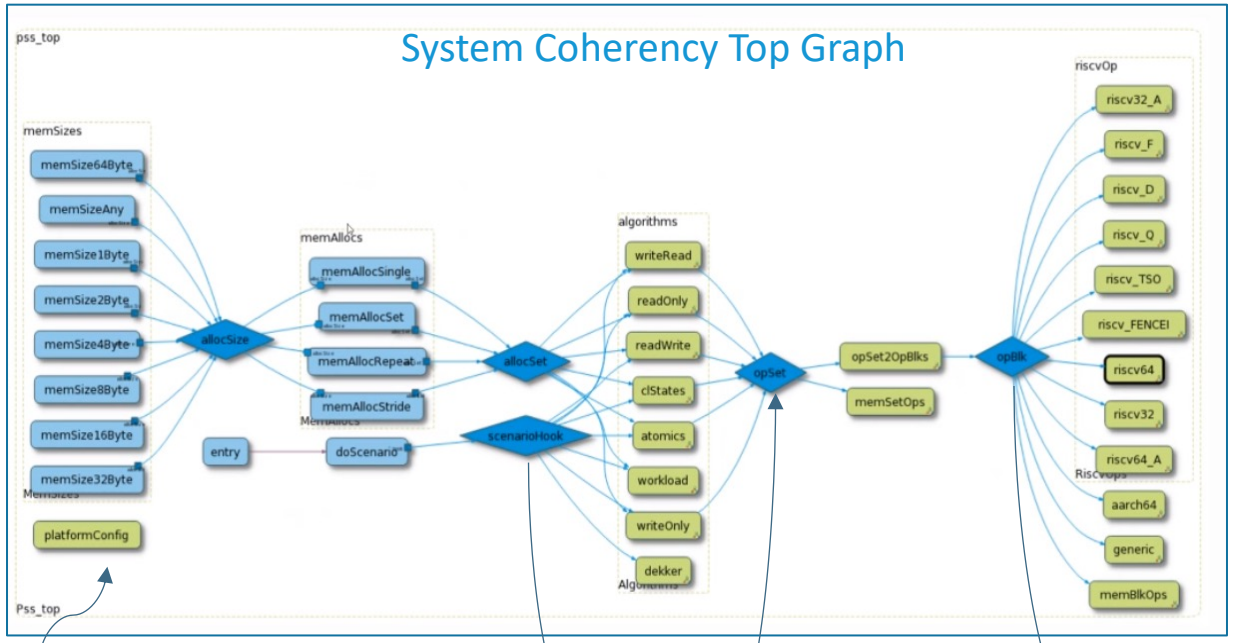


- **End-to-End use cases**
- **Early Firmware Testing**
- **Performance-Power Profiling**

RISC-V SoC Coherency Verification Planning Strategies



Modular, Configurable and Extendable Building Blocks



Max Memsize

Specialized Algorithm

Addl Instructions

Example Customizations

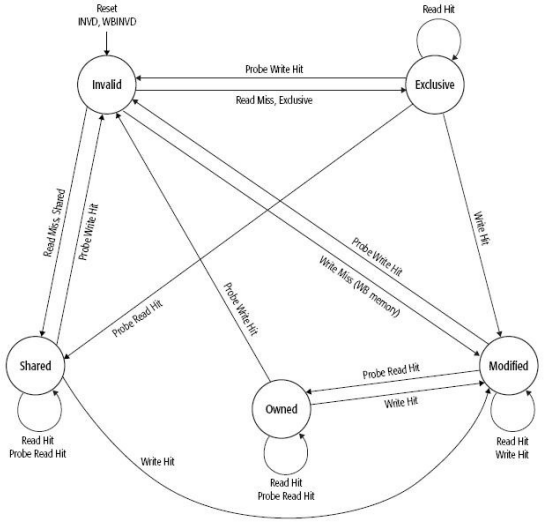
Specific Component Characteristic

Special Coherency Test Algorithm

Extra Processor Instruction

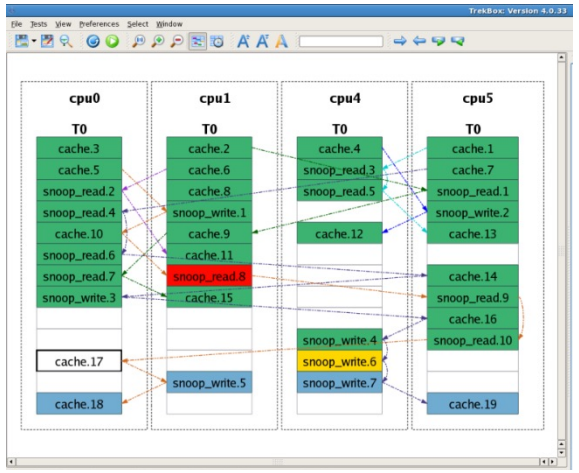
Coherency Oriented Test Generation

- "One Address, Many Data"
- Start with end state, work backwards to find transition scenario

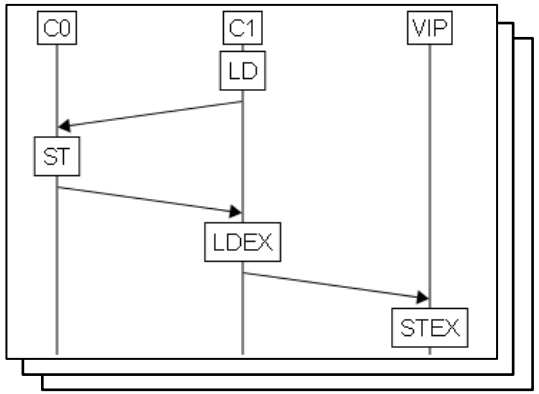


N Transition Sequences

Concurrent Scenario Test Case

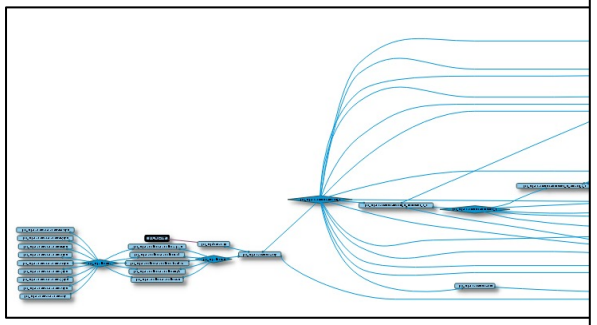


N Transition Scenarios



Schedule Memory
Interleave & Pack
Resolve Dependencies

RISC-V SoC Coherency Test Synthesis



TrekDebug 1.2.26: moesiStates@centos6

File Tests View Preferences Select Window

Find: in moesiStates.c Match Case

hart_0 T0	hart_1 T0
checkBlk.1	multiOp.1
checkBlk.7	flushBlk.1
writeBlk.1	writeBlk.7
flushBlk.6	flushBlk.2
checkBlk.8	writeBlk.2
flushBlk.3	flushBlk.7
checkBlk.9	writeBlk.3
checkBlk.2	flushBlk.8
writeBlk.10	flushBlk.4
checkBlk.3	checkBlk.10
writeBlk.4	multiOp.2
writeBlk.8	checkBlk.4
writeBlk.5	checkBlk.11
writeBlk.9	checkBlk.5
writeBlk.6	flushBlk.9
writeBlk.11	checkBlk.6
multiOp.3	flushBlk.5
multiOp.5	checkBlk.12
multiOp.6	flushBlk.10
writeBlk.12	multiOp.4
checkBlk.16	writeBlk.13
writeBlk.14	multiOp.7

Memory Map

Memory Values

```
writeBlk.9 trek_mem_mem+0x50 (0x8 bytes)
0x00000000:        5deb7686        0e5bce5f
writeBlk.9 trek_mem_mem+0x1a3ba8 (0x8 bytes)
Before
0x00000000:        10c4ca46        97876321
After
0x00000000:        5deb7686        0e5bce5f
```

Test Source

IO Task | writeBlk.9

```
// writeBlk.9
    trek_write32_shared(0x1e, trek_hart_0_T0_state);
  }
  case (0x1e): {    // wait for checkBlk.11
    if (trek_read32_shared(trek_hart_1_T0_state) < 0x1a) break;
    trek_c2t_event(0, 0x23);          // [event:0x23 agent:hart_0 thread:T0 instance:writeBlk.9]
        /* tbx: trek_message("Begin writeBlk.9");  */
    // memAllocHash index: 0x8ee size: 0x8 bytes alignment:8 @trek_mem_mem+0x001a3ba8
    // pss_top.moesiStates.EXCLUSIVE_to_MODIFIED_8_i / pss_top.opSet2OpBlks.singleOp / pss_top.memBlk
    // trek_copy_memory_block(trek_mem_mem+0x00000050, trek_mem_mem+0x001a3ba8, 0x8)
    trek_write64(trek_read64(trek_mem_mem+0x00000050), trek_mem_mem+0x001a3ba8);
    trek_c2t_event(0, 0x24);          // [event:0x24 agent:hart_0 thread:T0 instance:writeBlk.9]
        /* tbx: trek_message("End writeBlk.9");  */
    trek_write32_shared(0x1f, trek_hart_0_T0_state);
    break;
  }
```

Memory locations of writeBlk.9

Test Idle

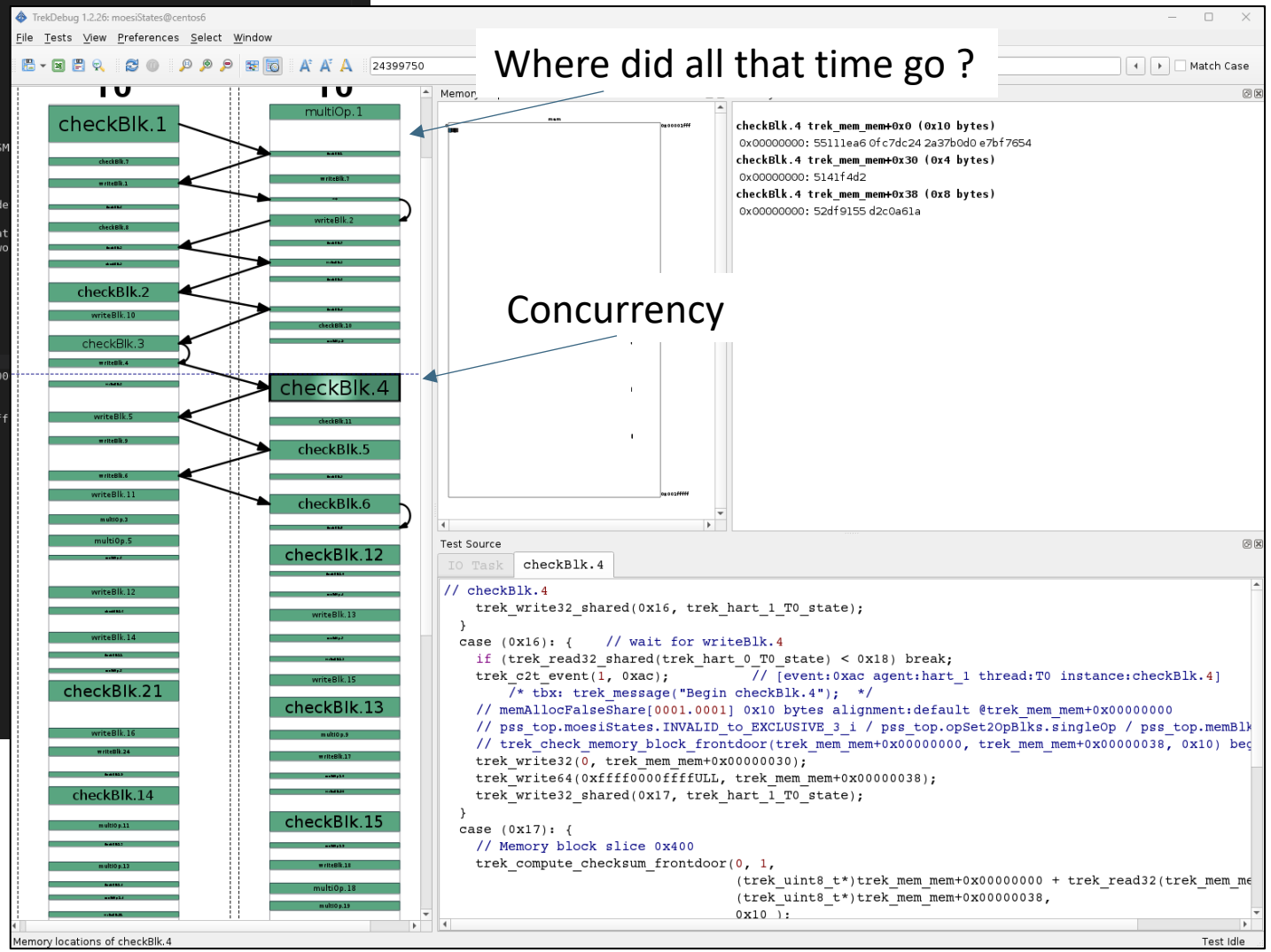
Memory Scoreboard

Address targets capacity eviction

Transition State

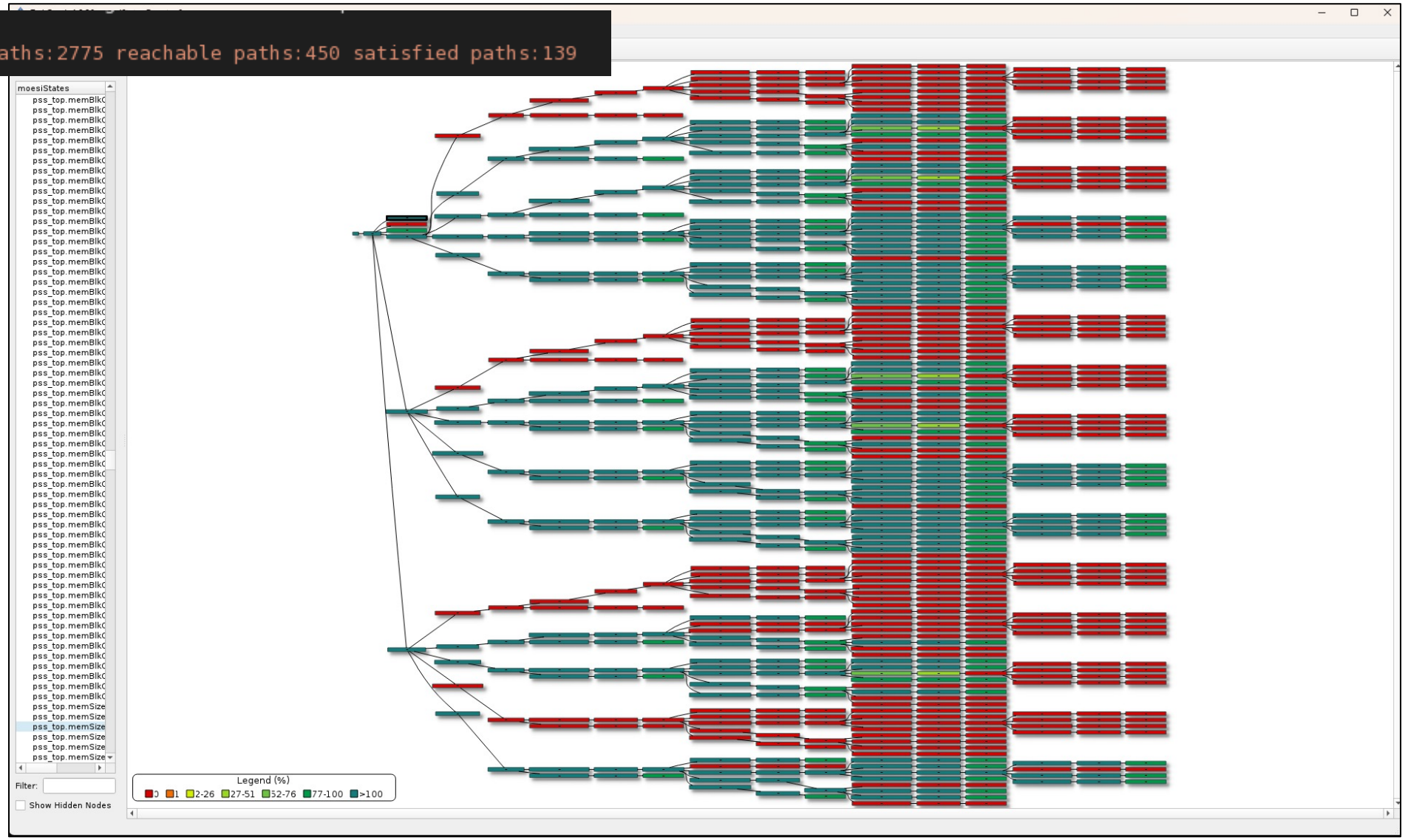
RISC-V SoC Coherency Timing Back-Annotation

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_args=+TREK_TBX_FILE=all.tbx all.c
sims: ==================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ==================================================
sims: ==================================================
sims:   Simulation Script for OpenSPARC T1
sims:   Copyright (c) 2001-2006 Sun Microsystems, Inc.
sims:   All rights reserved.
sims: ==================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SM
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/de
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verificat
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/wo
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00
IOB sending to tile X:  0 Y:  0
   raw tileid 00000000
16607500 TILE0 L1.5 th0: Received PCX PCX_REQTYPE_IFILL   Addr 0xfff
 0, l1way 0
   Data: 0x0000000000000000
   CSM HDID:    0, HD_SIZE:  0, SDID:    0, LSID:  0
   CSM Data: 0x000000000

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```

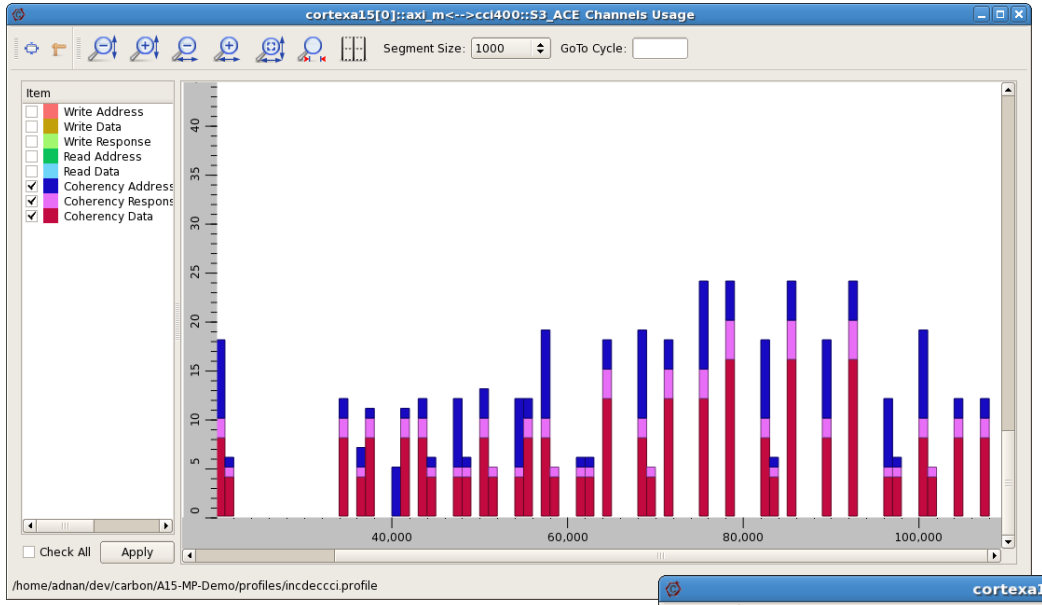


RISC-V SoC Coherency Scenario Coverage

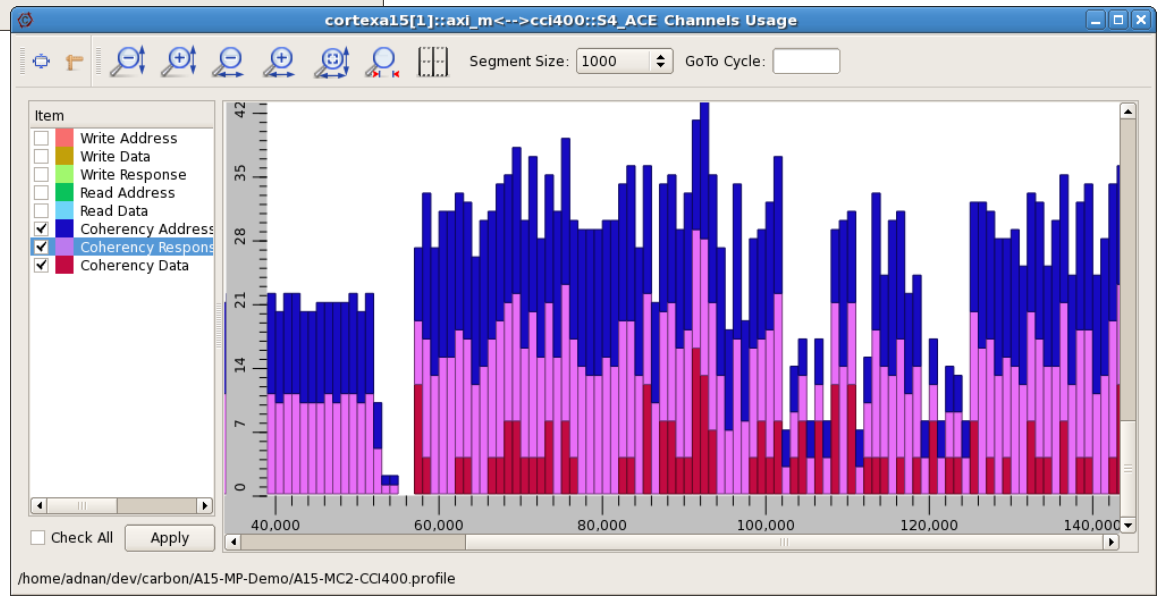
```
trek: info: analyzing coverage...
trek: info: total hits:722 total paths:2775 reachable paths:450 satisfied paths:139
```



Efficacy of System-Integrity Testing using the RISC-V TrekApp



Typical directed coherency test …

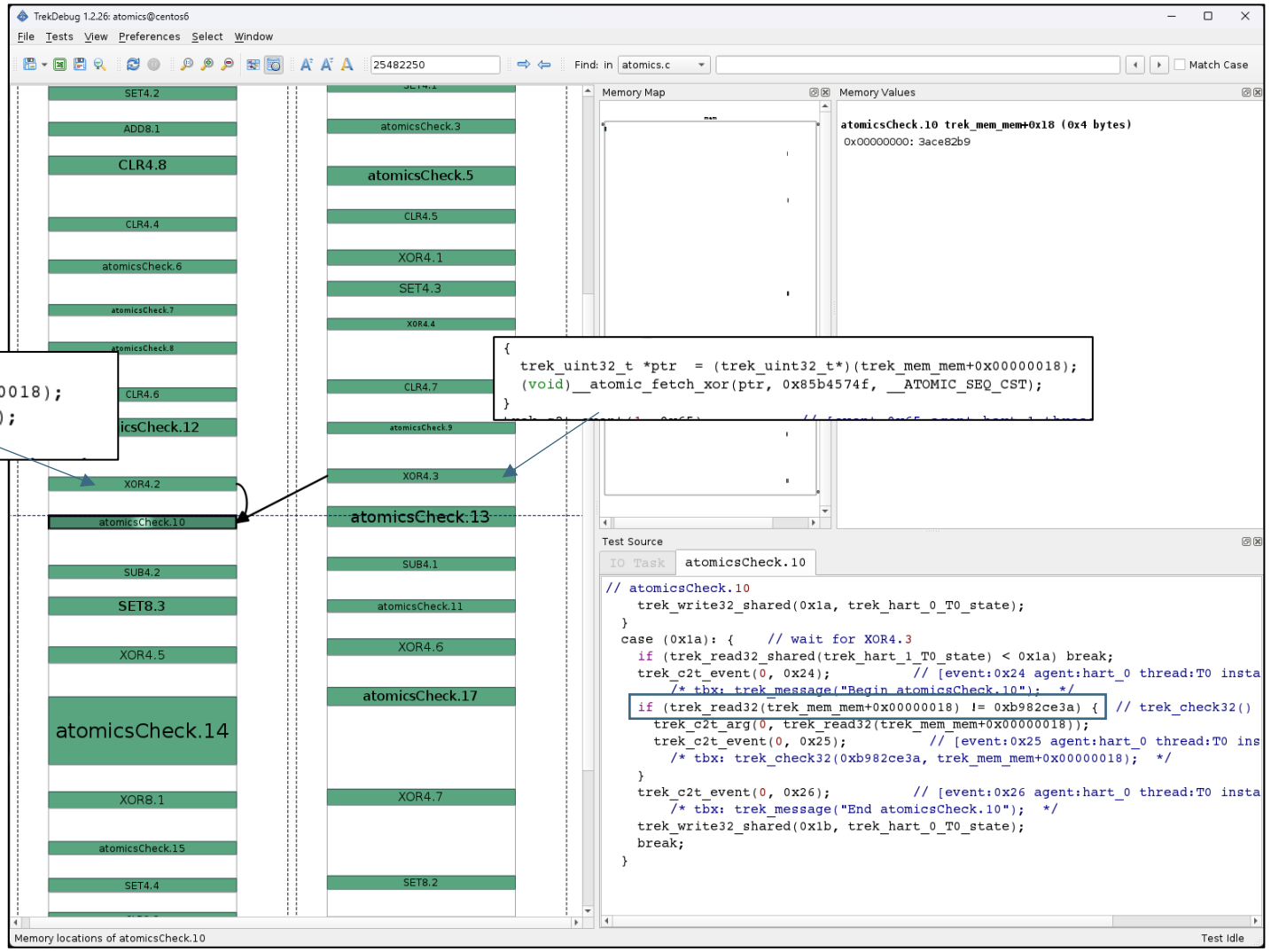


… vs. RISC-V TrekApp automated Sys-Integrity tests

RISC-V SoC Atomics : Timing Back Annotation

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_args=+TREK_TBX_FILE=all.tbx all.c
sims: ==================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ==================================================
sims: ==================================================
sims:   Simulation Script for OpenSPARC T1
sims:   Copyright (c) 2001-2006 Sun Microsystems, Inc.
sims:   All rights reserved.
sims: ==================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SMP Fri Jan 27 02:56:13 UTC 2023 x86_64 x86_64 x86_6
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openpiton/x1y1-all
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verification Systems www.brekersystems.com
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openpiton/x
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00010001
IOB sending to ti
   raw tileid 000
16607500 TILE0 L1
 0, l1way 0
   Data: 0x000000
   CSM HDID:    0
   CSM Data: 0x00

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```

```
{
  trek_uint32_t *ptr  = (trek_uint32_t*)(trek_mem_mem+0x00000018);
  (void)__atomic_fetch_xor(ptr, 0x1d1b128d, __ATOMIC_SEQ_CST);
}
```




```
{
  trek_uint32_t *ptr  = (trek_uint32_t*)(trek_mem_mem+0x00000018);
  (void)__atomic_fetch_xor(ptr, 0x85b4574f, __ATOMIC_SEQ_CST);
}
```

RISC-V SoC Memory Ordering: Dekker Algorithm

- Assume initial state A=0 , B=0

- The Dekker Algorithm States

```
core 0: ST A, 1; MEM_BARRIER; LD B
core 1: ST B, 1; MEM_BARRIER; LD A
error iff ( A == 0 && B == 0 )
```

- This is a test for a weakly ordered memory system
  - Such a system must preserve the property that a LD may not reorder ahead of a previous ST from the same agent

Dekker Scaled to Multiple Processors

Core 0	Core 1	Core 2	Core 3
ST A	ST B	ST C	ST D
LD B	LD C	LD D	LD A

- Error if all loads see initial value
- Dekker randomized for all memories, operation sizes, load/store sources

RISC-V SoC Memory Ordering: Timing Back-Annotation

```
sims -sys=manycore -ariane -vlt_run -x_tiles=1 -y_tiles=1 -asm_diag_root=/mnt/dev_data/work/git/worktrees/dev1/trek5/b
uild/dev/testsuite/openpiton/x1y1-all -model_dir=/mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuite/openp
iton/x1y1-all -rtl_timeout=10000000 -sim_run_args=+max_cycle=1500000 -sim_run_
sims: ==================================================
sims:   Simulation Script for OpenPiton
sims:   Modified by Princeton University on June 9th, 2015
sims: ==================================================
sims: ==================================================
sims:   Simulation Script for OpenSPARC T1
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sims:   All rights reserved.
sims: ==================================================
sims: start_time Thu Mar  2 11:59:35 PST 2023
sims: running on centos6
sims: uname is Linux centos6 5.15.90.1-microsoft-standard-WSL2 #1 SMP Fri Jan 
4 GNU/Linux
sims: version 2.0
sims: dv_root /tools/vendors/RISCV/openpiton/piton
sims: model_dir /mnt/dev_data/work/git/worktrees/dev1/trek5/build/dev/testsuit
INFO(155750): trek: Starting with +TREK_TBX_FILE=all.tbx
INFO(155750): trek: info: Breker TrekBox-1.2.26 (c) Breker Verification System
INFO(155750): trek: info: Generating file: /mnt/dev_data/work/git/worktrees/de
1y1-all/all.tdb
INFO(155750): trek: info: random seed: 0x7438c1bb
INFO(155750): trek: info: ****  Start of Test ****
Reset complete
Info: Qsel value(0)
Info: cpx request 1
Info: cpx packet from iob ->170000000000000000000000000000010001
Info: cpx request 0
Doing IOB stuff - got values: 00017000 00000000 00000000 00000000 00010001
IOB sending to tile X:  0 Y:  0
   raw tileid 00000000
16607500 TILE0 L1.5 th0: Received PCX PCX_REQTYPE_IFILL   Addr 0xfff1010000, n
 0, l1way 0
   Data: 0x0000000000000000
   CSM HDID:    0, HD_SIZE:  0, SDID:    0, LSID:  0
   CSM Data: 0x000000000

0000000000fd690c L15 TILE0:
NoC1 credit:  8
NoC1 reserved credit:  0
TILE0 Pipeline: *  X  X
Stage 1 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S1 Address: 0xfff1010000
L15_MON_END


0000000000fd6b00 L15 TILE0:
NoC1 credit:  7
NoC1 reserved credit:  0
TILE0 Pipeline: X  *  X
Stage 2 status:    Operation: L15_REQTYPE_IFILL
   TILE0 S2 Address: 0xfff1010000
   TILE0 S2 Cache index:   0
```
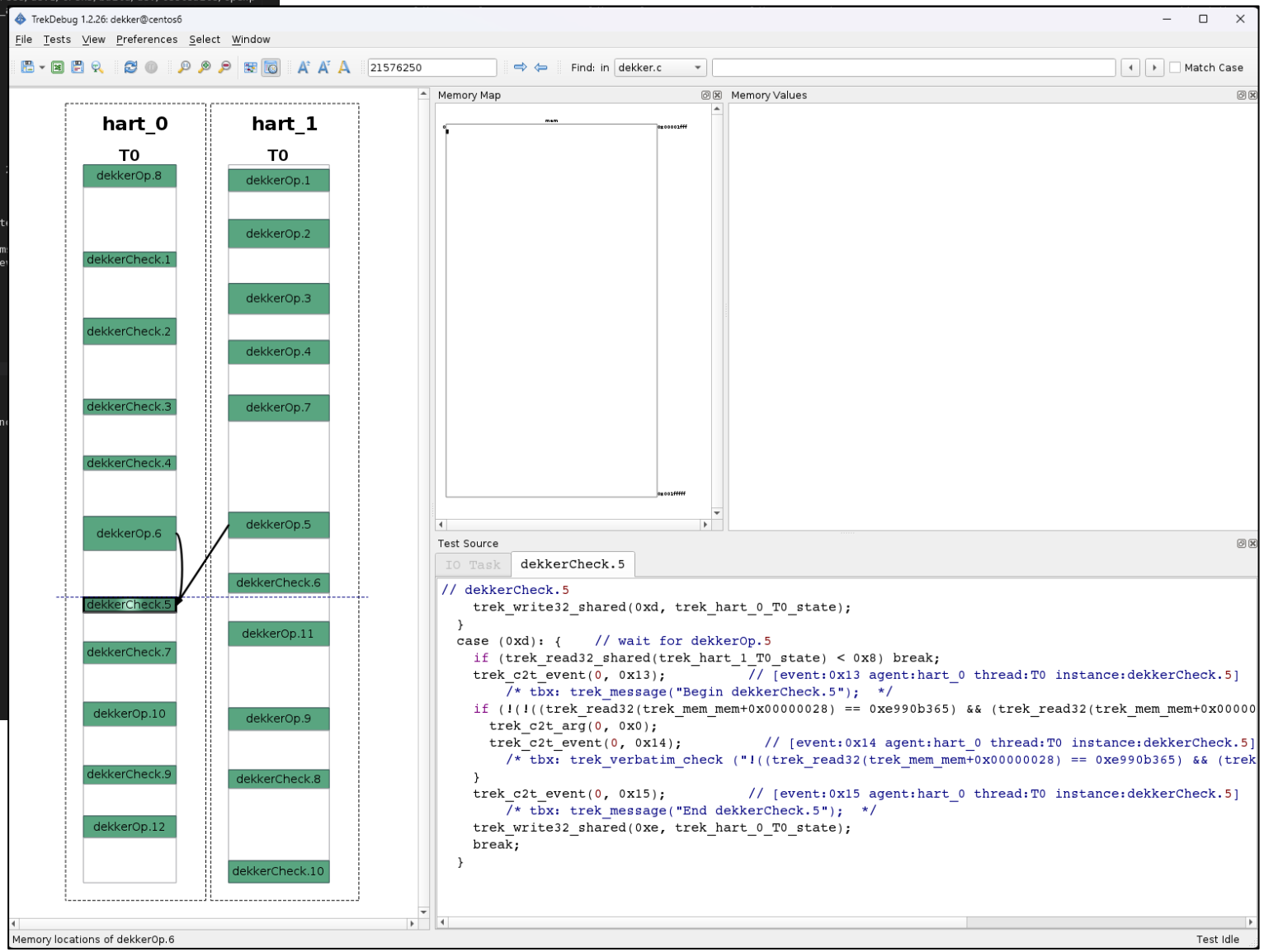
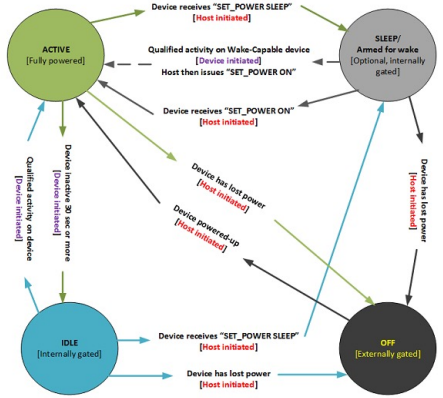



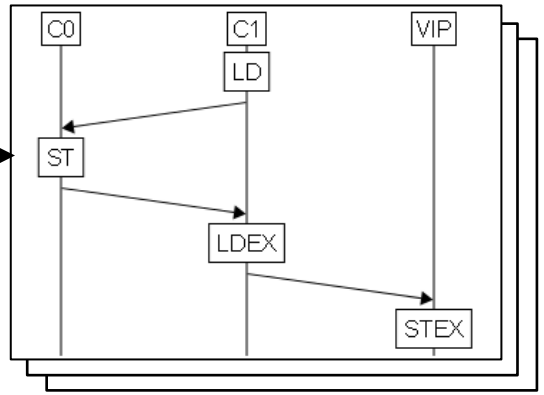
Conclusion

Power Management TrekApp

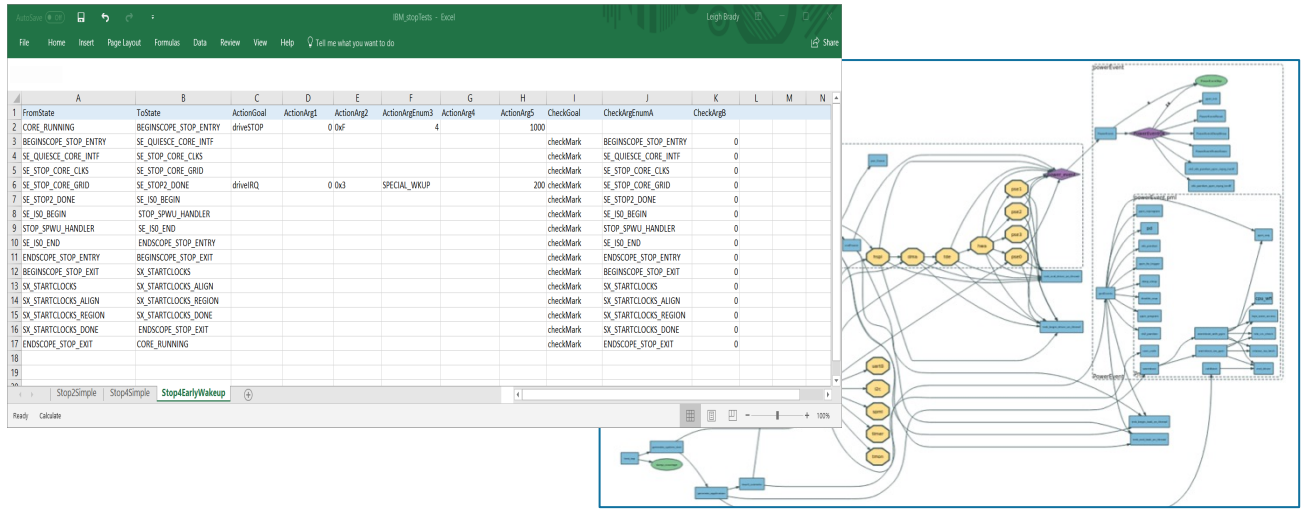


N Transition Sequences

N Transition Scenarios

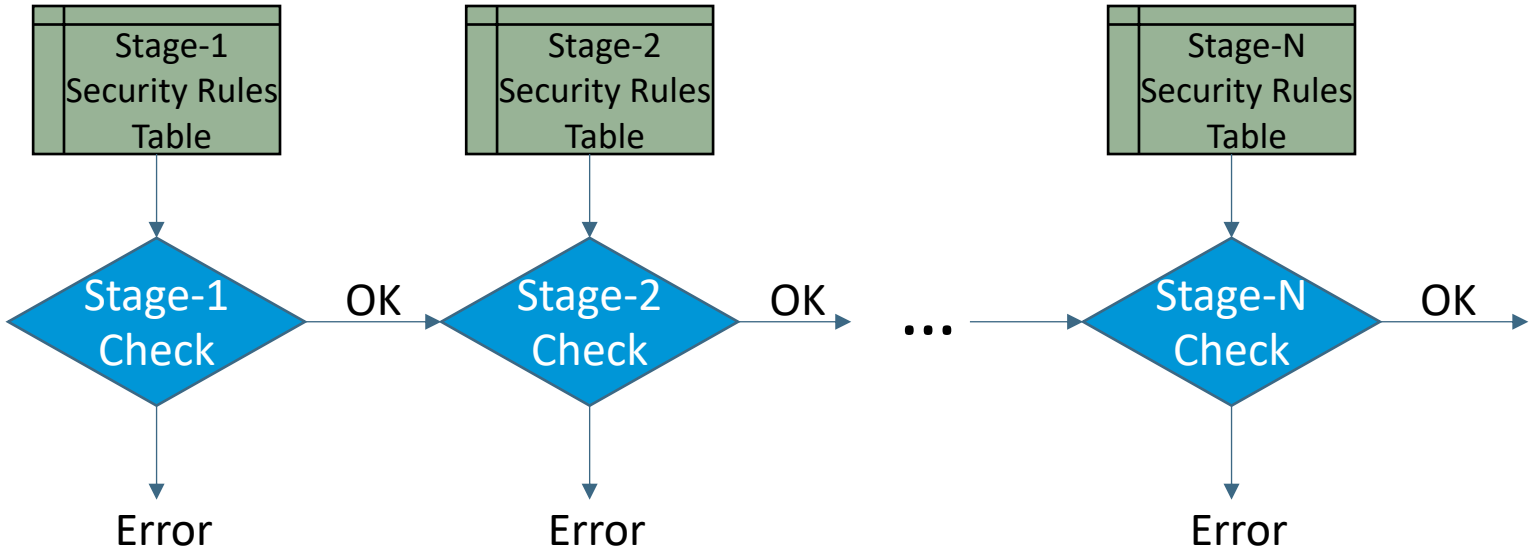


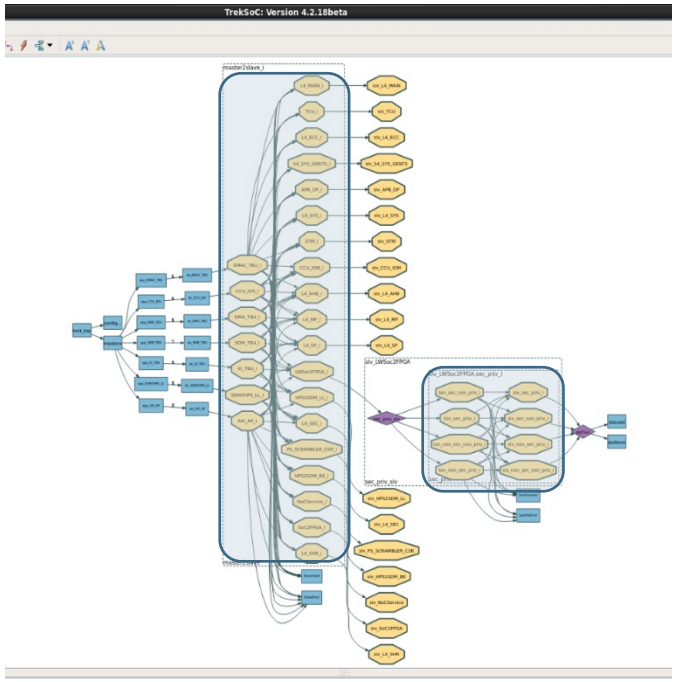
- TrekApp uses state table to turn SM into multi-transition graph
- Overlay power domain reset tests onto functional tests
- Works with other SM scenarios, e.g. Boot Rom verification



	A	B	C	D	E	F	G	H	I	J	K
1	FromState	ToState	ActionGoal	ActionArg1	ActionArg2	ActionArgEnum3	ActionArg4	ActionArg5	CheckGoal	CheckArgEnumA	CheckArgB
2	CORE_RUNNING	BEGINSCOPE_STOP_ENTRY	driveSTOP	0	0xF	4		1000			
3	BEGINSCOPE_STOP_ENTRY	SE_QUIESCE_CORE_INTF							checkMark	BEGINSCOPE_STOP_ENTRY	0
4	SE_QUIESCE_CORE_INTF	SE_STOP_CORE_CLKS							checkMark	SE_QUIESCE_CORE_INTF	0
5	SE_STOP_CORE_CLKS	SE_STOP_CORE_GRID							checkMark	SE_STOP_CORE_CLKS	0
6	SE_STOP_CORE_GRID	SE_STOP2_DONE	driveIRQ	0	0x3	SPECIAL_WKUP		200	checkMark	SE_STOP_CORE_GRID	0
7	SE_STOP2_DONE	SE_IS0_BEGIN							checkMark	SE_STOP2_DONE	0
8	SE_IS0_BEGIN	STOP_SPWU_HANDLER							checkMark	SE_IS0_BEGIN	0
9	STOP_SPWU_HANDLER	SE_IS0_END							checkMark	STOP_SPWU_HANDLER	0
10	SE_IS0_END	ENDSCOPE_STOP_ENTRY							checkMark	SE_IS0_END	0
11	ENDSCOPE_STOP_ENTRY	BEGINSCOPE_STOP_EXIT							checkMark	ENDSCOPE_STOP_ENTRY	0
12	BEGINSCOPE_STOP_EXIT	SX_STARTCLOCKS							checkMark	BEGINSCOPE_STOP_EXIT	0
13	SX_STARTCLOCKS	SX_STARTCLOCKS_ALIGN							checkMark	SX_STARTCLOCKS	0
14	SX_STARTCLOCKS_ALIGN	SX_STARTCLOCKS_REGION							checkMark	SX_STARTCLOCKS_ALIGN	0
15	SX_STARTCLOCKS_REGION	SX_STARTCLOCKS_DONE							checkMark	SX_STARTCLOCKS_REGION	0
16	SX_STARTCLOCKS_DONE	ENDSCOPE_STOP_EXIT							checkMark	SX_STARTCLOCKS_DONE	0
17	ENDSCOPE_STOP_EXIT	CORE_RUNNING							checkMark	ENDSCOPE_STOP_EXIT	0

Security TrekApp

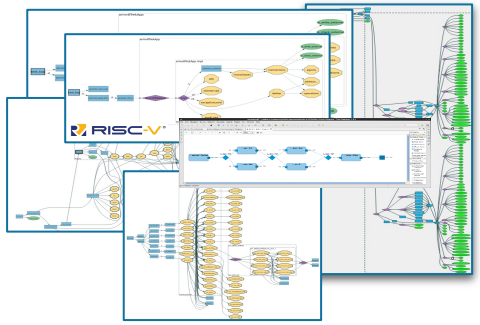


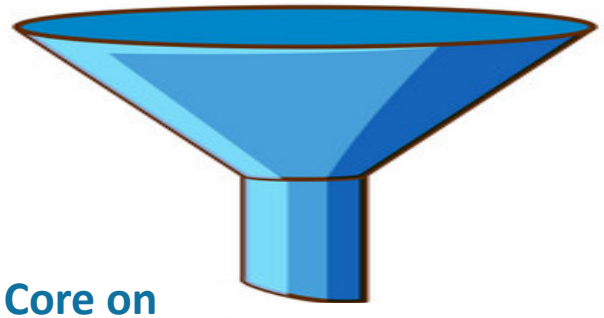


- Security TrekApp in limited production with key customer cooperation
- Allows vulnerabilities to be derived from correct operation graph
- Works with multi-stage pipeline SoC, also could operate on protected key/register scenario and SoC protected regions

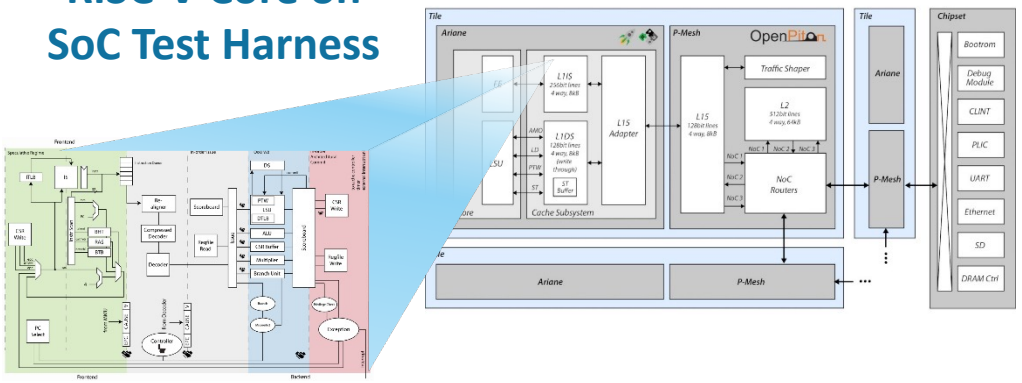
Push-Button Breker SystemVIP Library

A Comprehensive, Automated Health Check for SoCs





RISC-V Core on SoC Test Harness



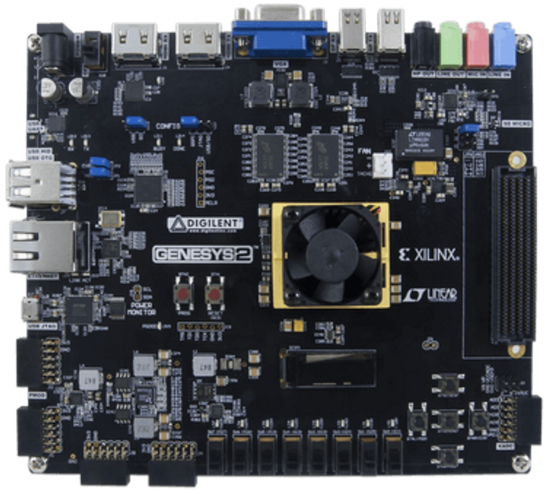
SoC Integrity TrekApp Library

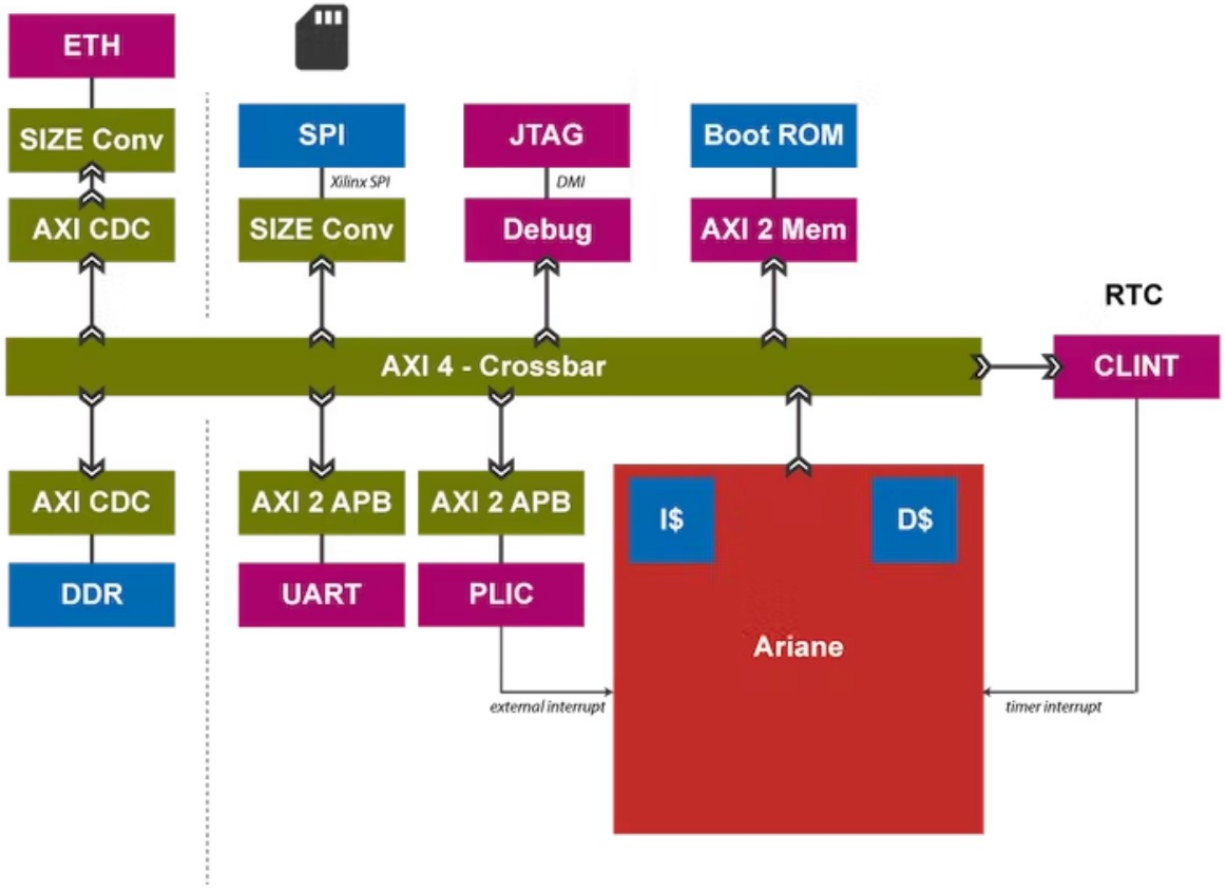
- The ***Coherency TrekApp*** verifies cache and system-level coherency in a multiprocessor SoC
- The ***Power Management TrekApp*** automates power domain switching verification
- The ***Security TrekApp*** automates testing of hardware access rules for HRoT fabrics
- The ***Networking & Interface TrekApp*** automates packet generation, CXL, UCIe interface tests
- The ***SoC Toolkit TrekApp*** series of tests for typical sources of bugs across Arm and RISC-V SoCs

Other TrekApps

- The ***RISC-V Core TrekApp*** provides fast, pre-packaged tests for RISC-V Core and SoC integrity issues
- The ***Firmware TrekApp*** early testing of firmware without a processor model
- The ***End-to-end IP TrekApp*** IP test sets ported from UVM to SoC

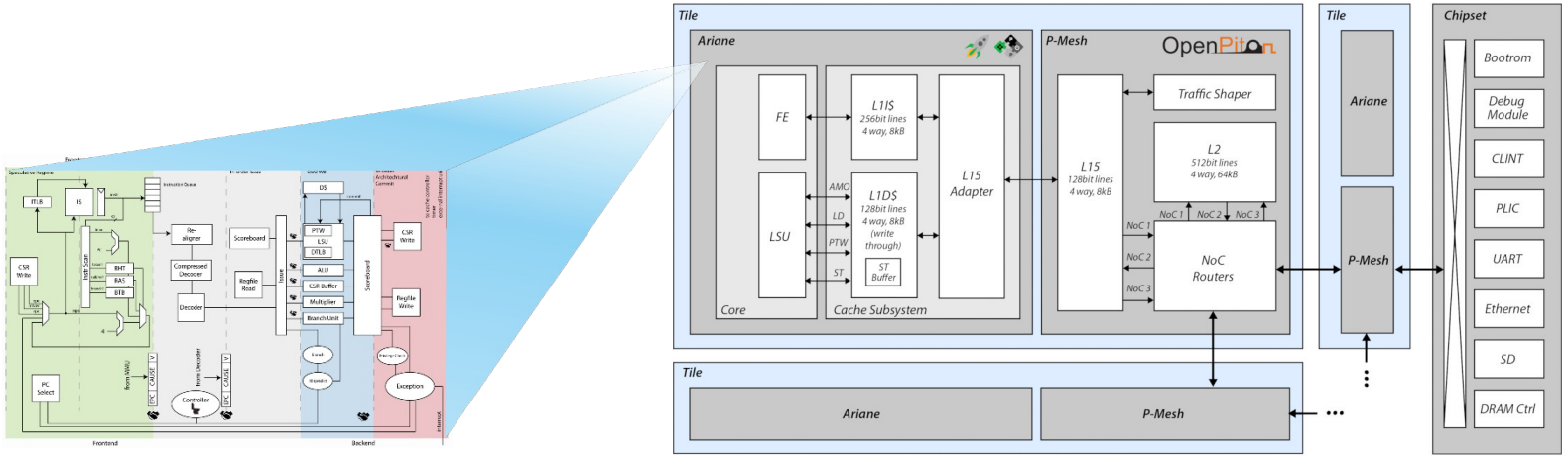
CVA6 Hardware Test:
Next phase test hardware with same content





FPGA block diagram implementing the Ariane CPU.

RISC-V System Integrity



"Working with Breker to develop the RISC-V TrekApp over the past year has been very rewarding. As RISC-V adoption continues to grow, support from design tool providers like Breker is key to accelerating time to market and assuring SoC quality."

Mohit Gupta, vice president and general manager of the SiFive IP business unit.

"After an extensive evaluation, we choose Breker's System Coherency TrekApp to help to ensure our design's coherency. The TrekApp offers ease to use and extremely fast setup and covers broad aspect of verification from simple workload to complex scenarios that includes Dekker and Atomics tests. Its flexible scaling will scale with us as we go from verifying the coherency of a few CPUs to hundreds of CPUs, matching our needs now and for our future RISC-V solution offerings."

JianYing Peng, CEO of Nuclei System Technology.

Thank You For Listening

For more information:

Go to **BrekerSystems.com**

Email: **info@BrekerSystems.com**