DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

Architecture to Analytics A2A

DVCON 2024

September 18-19, 2024 | Radisson Blu, Marathahalli, Bengaluru

AI For Verification

Today's Reality vs. Tomorrow's Promise

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cadence®

Agenda

- Opportunity for AI in Verification
- AI Optimization vs. Generative AI
- Reality – Optimization
- Promise – Generation
- What's Next?

Productivity Challenge in IC Design

Complexity Is Increasing

100X

Over the Next Decade

Source: Cadence analysis

More Annual Design Starts

4X

Over the Next Decade

(<=10nm)

Source: IBS Global Semiconductor Industry Service Report: Design Activities and Strategic Implications, July 2022
Source: Cadence analysis

Not Enough Engineers

Source: https://semiengineering.com/engineering-talent-shortage-now-top-risk-factor/

AI-Driven Opportunity

EDA 40-year History

Improving Productivity Through Design Abstraction

Manual Layout → Automated Transistor-Level Layout → Automated Cell-Based Place and Route → RTL Synthesis → High-Level Synthesis

A new generation of task abstraction tools

LLM-Based AI

Excellence in Simulation and Optimization

NUMERICAL SOLVERS	SMT SOLVERS	GRAPH THEORY AND TOPOLOGY
BINARY DECISION DIAGRAMS	BOUNDED MODEL CHECKER	DISTRIBUTED PROCESSING
SAT SOLVERS	ADAPTIVE MESHING	NON-LINEAR SOLVERS
SYMBOLIC MODEL CHECKERS	MATRIX SOLVERS	COMPUTATIONAL GEOMETRY

A new leap forwards in QOR and performance

Optimization AI

A Layered Approach to AI

cādence.ai

Chips-to-systems Intelligent Design Acceleration

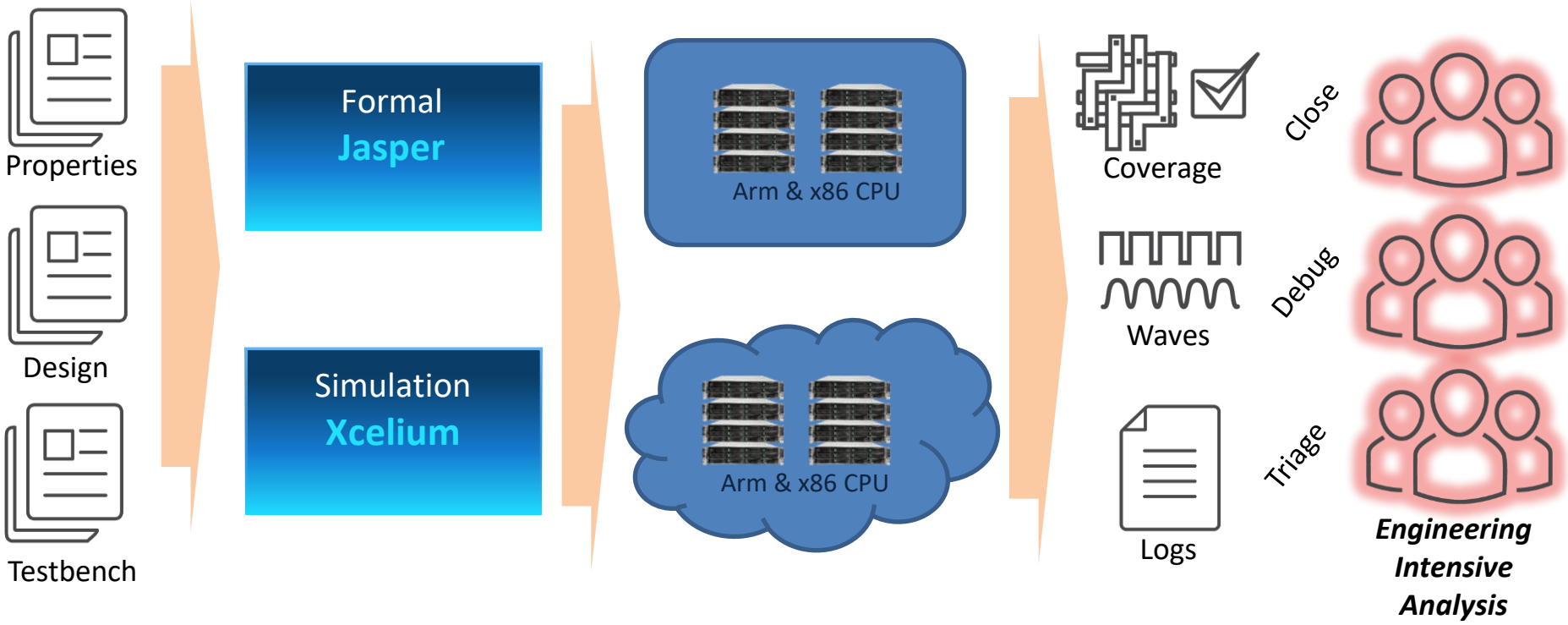
Cadence Co-Pilot (LLM-Based AI)

AI OPTIMIZATION SOLUTIONS

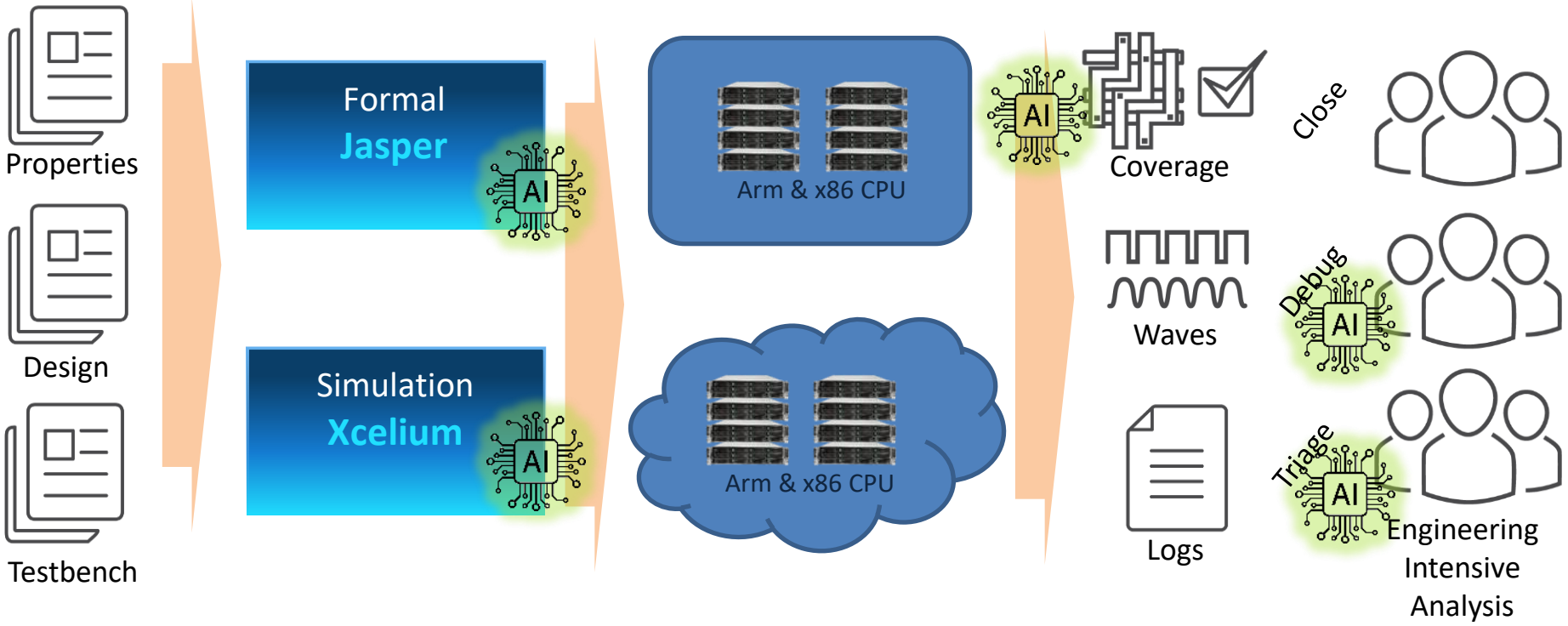
Cadence JedAI Data & AI Platform

AI Optimization

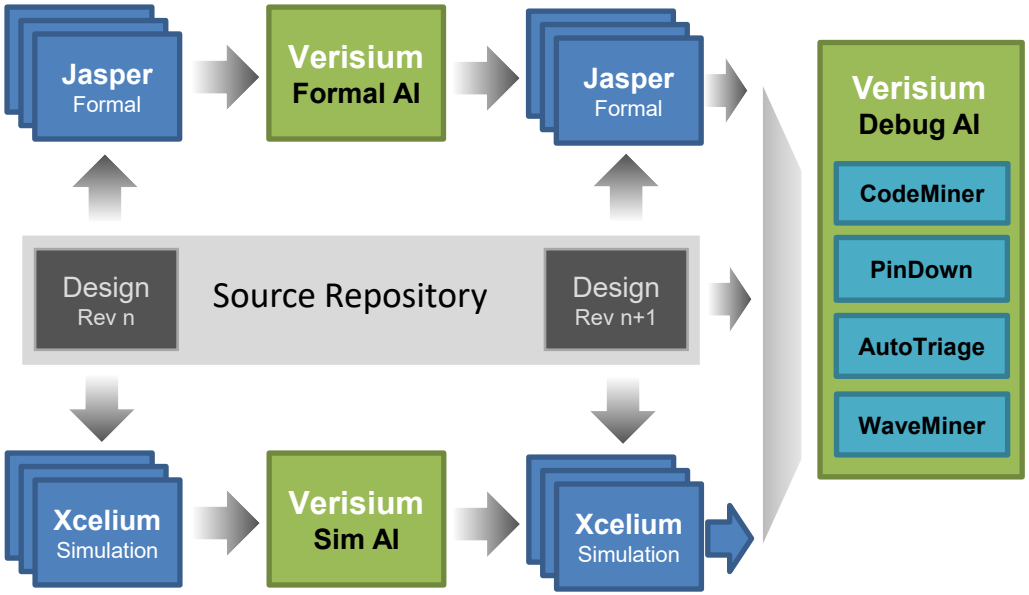
Verification Workflow



AI Optimization Potential



AI Optimization Reality



Technology

- ML Regression Speedup
  - Resource and engine prediction
  - Random variable outcome prediction
- ML Bug Hunting
  - Bug scenario prediction
- ML Coverage Maximization
  - Coverage hole correlation
- ML Bug Prediction
  - Source repository behavior modelling
- AI Source Analysis
  - Semantic impact analysis
- AI Waveform Analysis
  - Behavioral property analysis

AI Optimization Results

6x UVM Regression Speedup

- SimAI
  ML random variable outcome prediction

2x More Formal Proofs

- FormalAI SmartProof
  ML engine prediction

16x Faster Waveform Debug

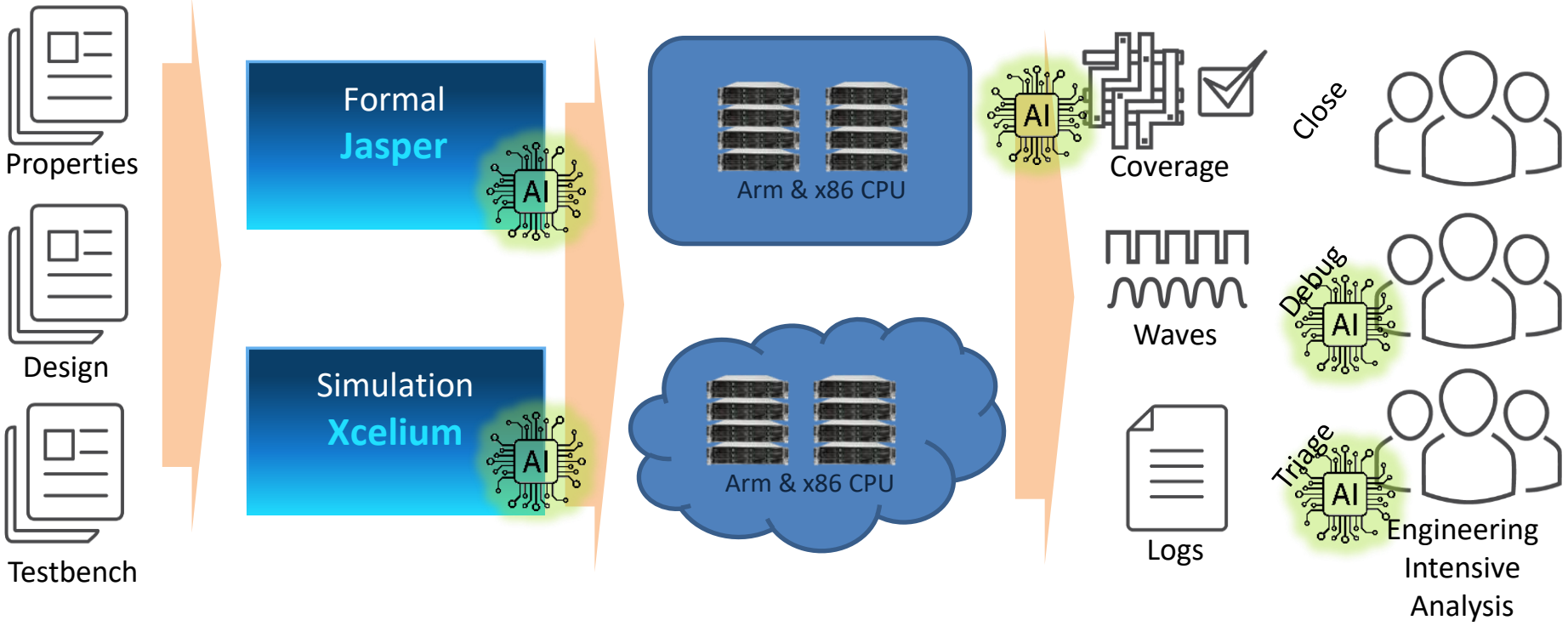
- WaveMiner
  Behavioral property analysis
- CodeMiner
  AI semantic impact analysis

7x Regression Debug Speedup

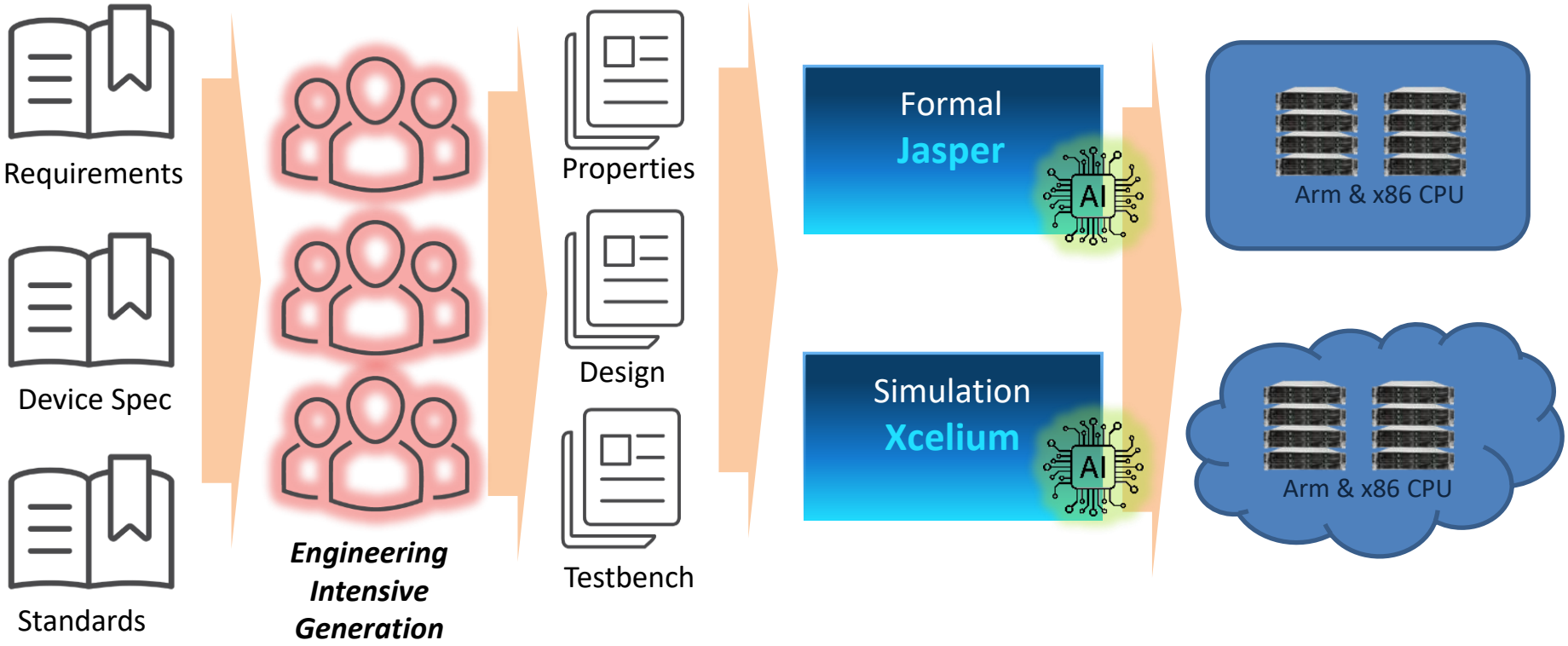
- PinDown
  ML bug prediction

AI Generation

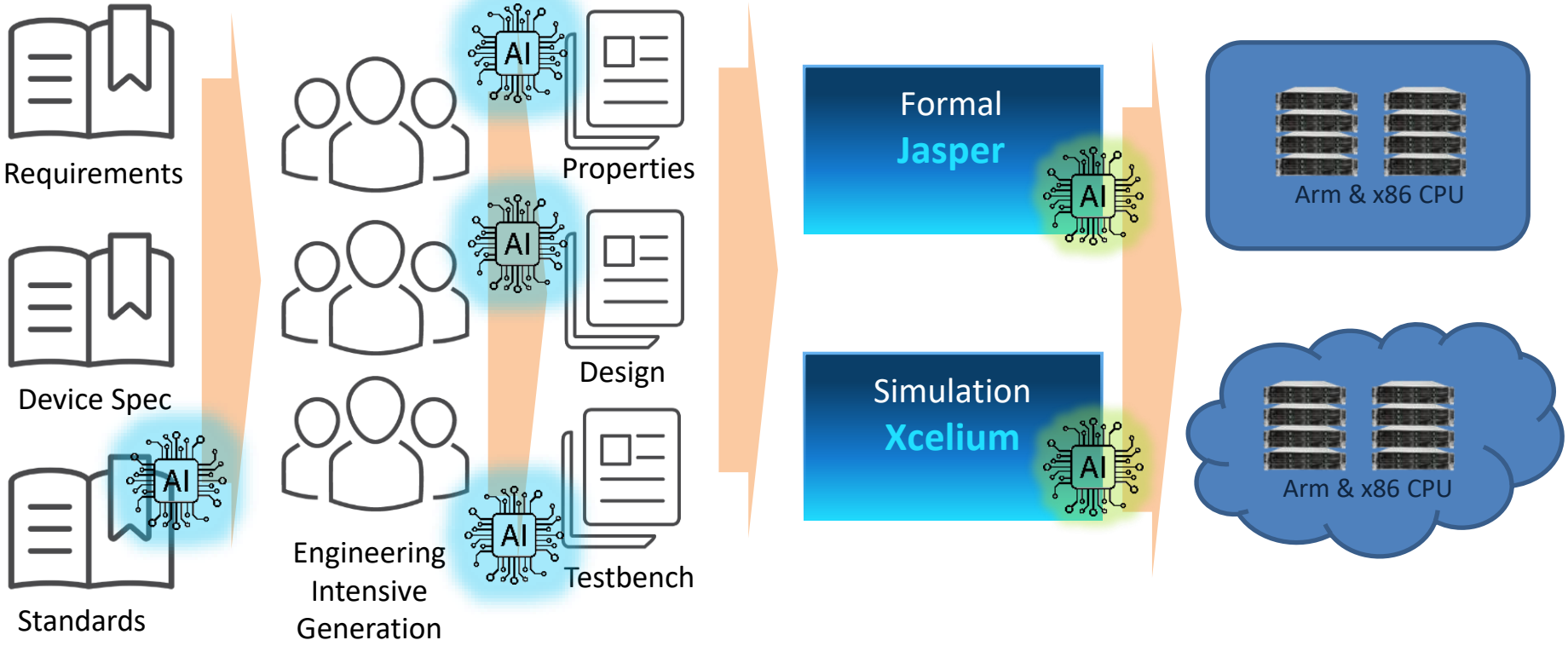
AI Optimization



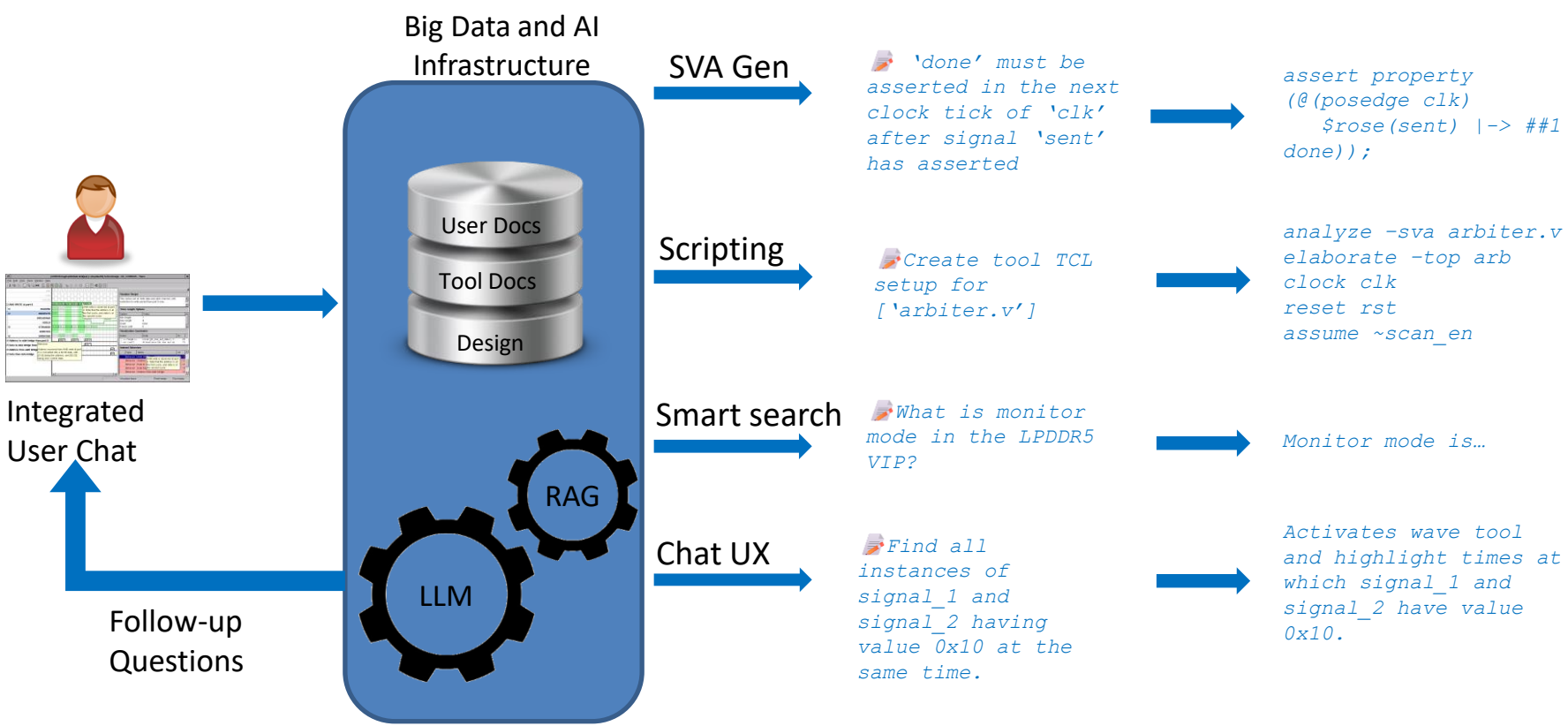
Spec to Code Workflow



AI Generation Potential



Verification Copilot



Generative AI Deployment

Verification Copilot

Llama Index | Nemo | Tuned RAG | User Rag — RAG Ecosystem

GPT | Llama | Tuned LLM | User LLM — LLM Ecosystem

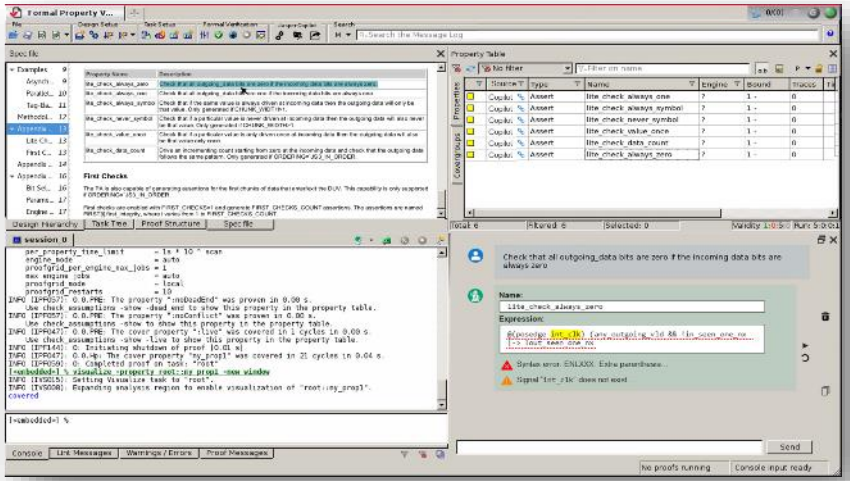
Docs | Standards | Private Data — Training Data

Commercial Cloud | Compute Farm — Compute

On Prem user tuned Copilot

GenAI EDA Value Add

Generate SVA for: 'done' must be asserted in the next clock tick of 'clk' after signal 'sent' was asserted



Jasper Agent

- ✓ SVA Linter
- ✓ Syntax issues
- ✓ Equivalence
- ✓ Intersection
- ✓ Implication
- ✓ Conflicts
- ✓ Ranking
- ✓ Clustering

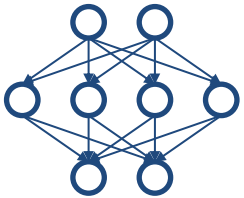
```
assert property (@(posedge clk)
        $rose(sent) |-> ##1 done));
```

Beyond LLM

CNN

2012 (AlexNet)

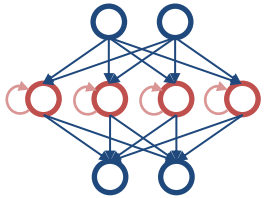
Good for images
Not good for text

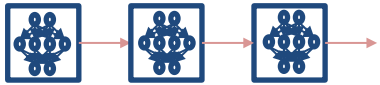


RNN

2014 (seq2seq)

Good for short text
Expensive to train





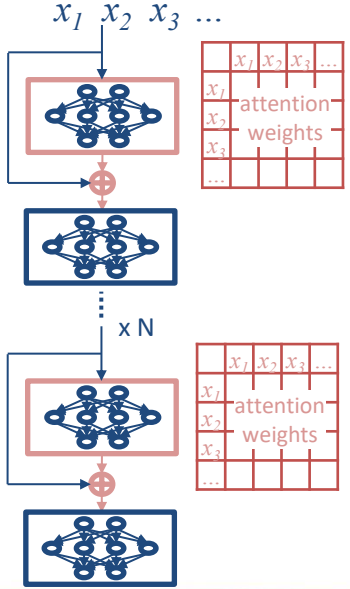
Remember previous words

LLM

2022 (ChatGPT)

Fast to train (no recurrence)
Support 10k+ word prompts
Inference expensive (n^2 prompt length)

Sequence of words

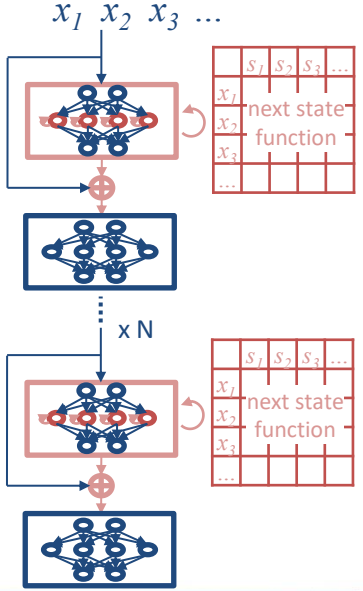


SSM

2024 (Mamba)

Fast to train
Fast inference
Support 1M+ word prompts

Sequence of words



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Thank-you

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