2022
DESIGN AND VERIFICATION™
DVCON
CONFERENCE AND EXHIBITION
EUROPE

MUNICH, GERMANY
DECEMBER 6 - 7, 2022

An end-to-end approach to Design and Verify BMS: from Requirements to Virtual Field Testing

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Speedgoat

SYSTEMS INITIATIVE

Agenda

- System-level Modeling and Verification
- From Model to Embedded Hardware: SiL and PiL Verification
- Real-time verification with HiL Testing

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System-level Modeling and Verification

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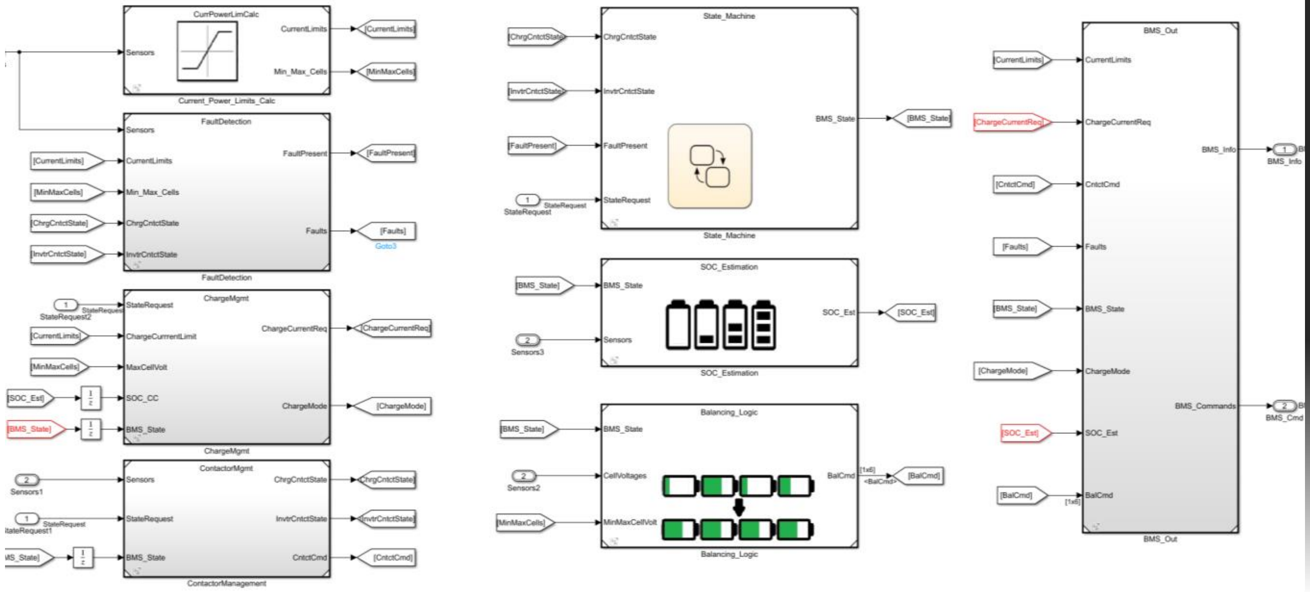
SYSTEMS INITIATIVE

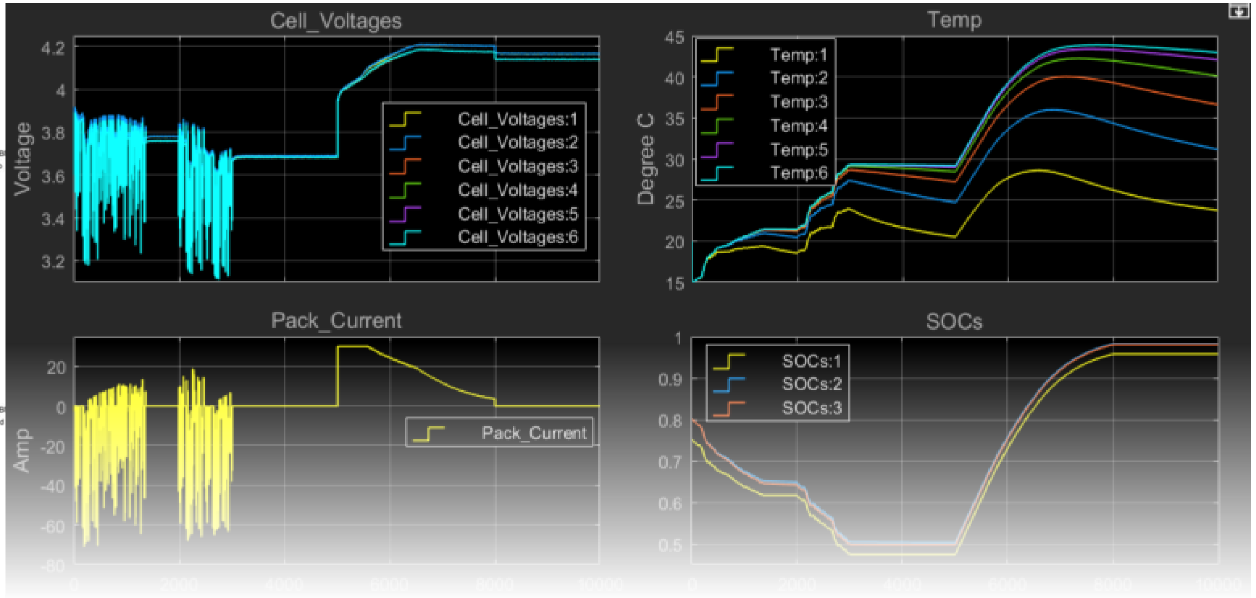
Motivation

Collaboration Gap

Long Iteration Cycles

Safety Critical System





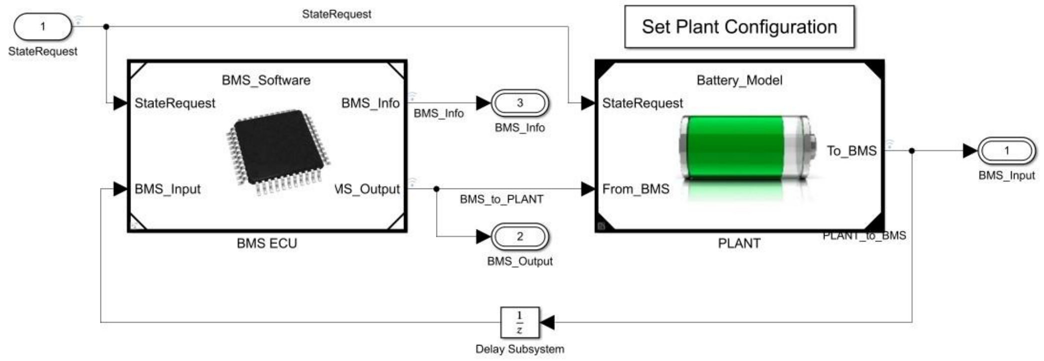
Multi-Domain System Modeling

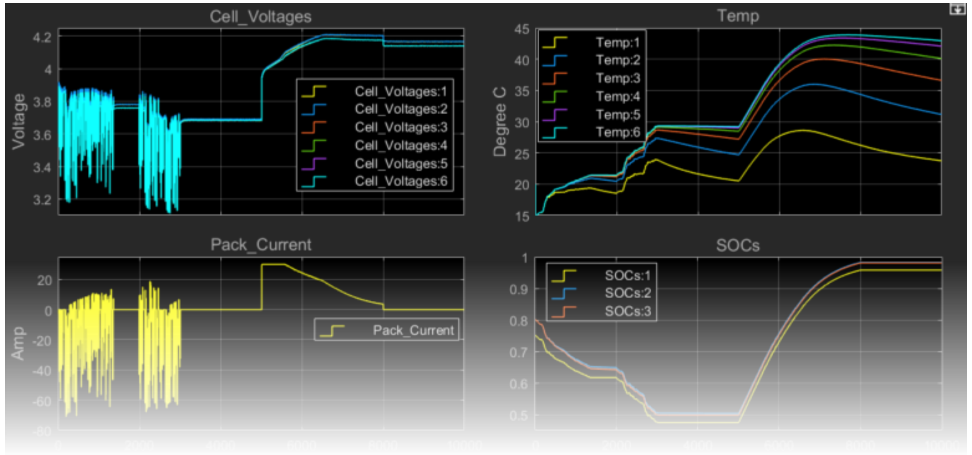
Simulations & Code Generation

Model V&V and HIL Testing

Evaluate Battery Management System Behavior

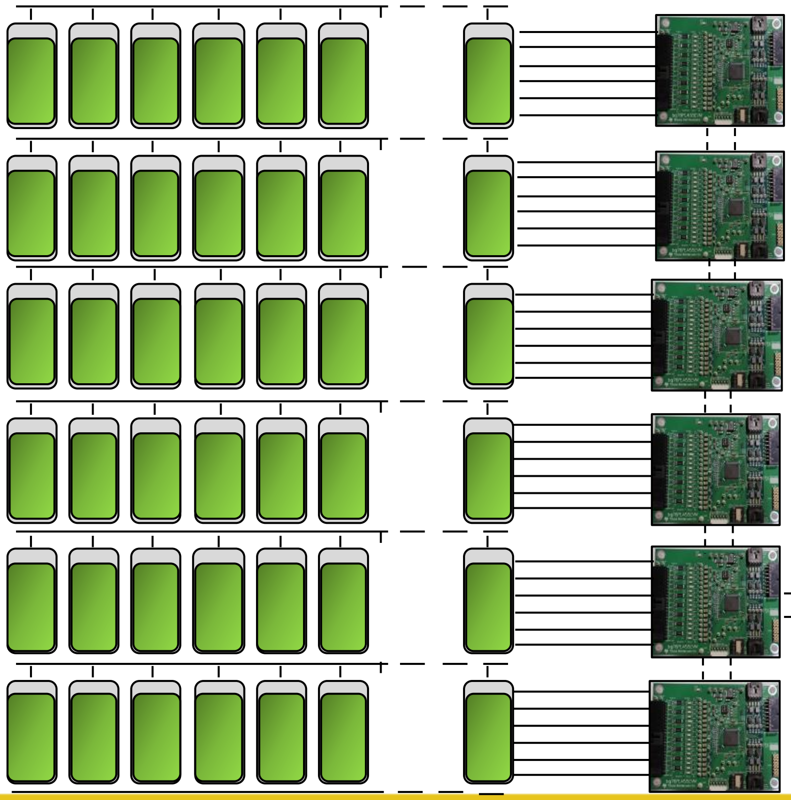
- Simulate interaction between software modules
- Design & test algorithms for different operating conditions
- Calibrate software before putting into battery pack or vehicle





Battery Management System Architecture

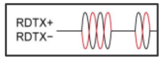
Battery Pack | Cell Monitoring | Software



```
if (((uint32_T)State_Machine_DW.temporalCounter_i3) < 15U) {
  State_Machine_DW.temporalCounter_i3 = (uint8_T)((int32_T)(((ir
    State_Machine_DW.temporalCounter_i3) + 1));
}

if (((uint32_T)State_Machine_DW.is_active_c2_State_Machine) == (
  State_Machine_DW.is_active_c2_State_Machine = 1U;
  State_Machine_DW.is_MainStateMachine = State_Machine_IN_Standk
  *rty_BMS_State = 0;
  State_Machine_DW.MonitorCurrLimMode = MonitorCurrLimModeType_N
  State_Machine_DW.MonitorCellVoltageMode =
    MonitorCellVoltageModeType_NoCellVoltFault;
  State_Machine_DW.Delta = (real32_T)fabs((real_T)((real32_T)
    ((*rtu_Pack_Voltage) - sum_gyOCKAG3(rtu_Cell_Voltages))));
```

Supervisory tasks
SOC estimation
Contactor management
Isolation monitoring
Fault detection and recovery
Thermal management
Current & power limits



Measurement
Cell Diagnostic,
Cell Balancing

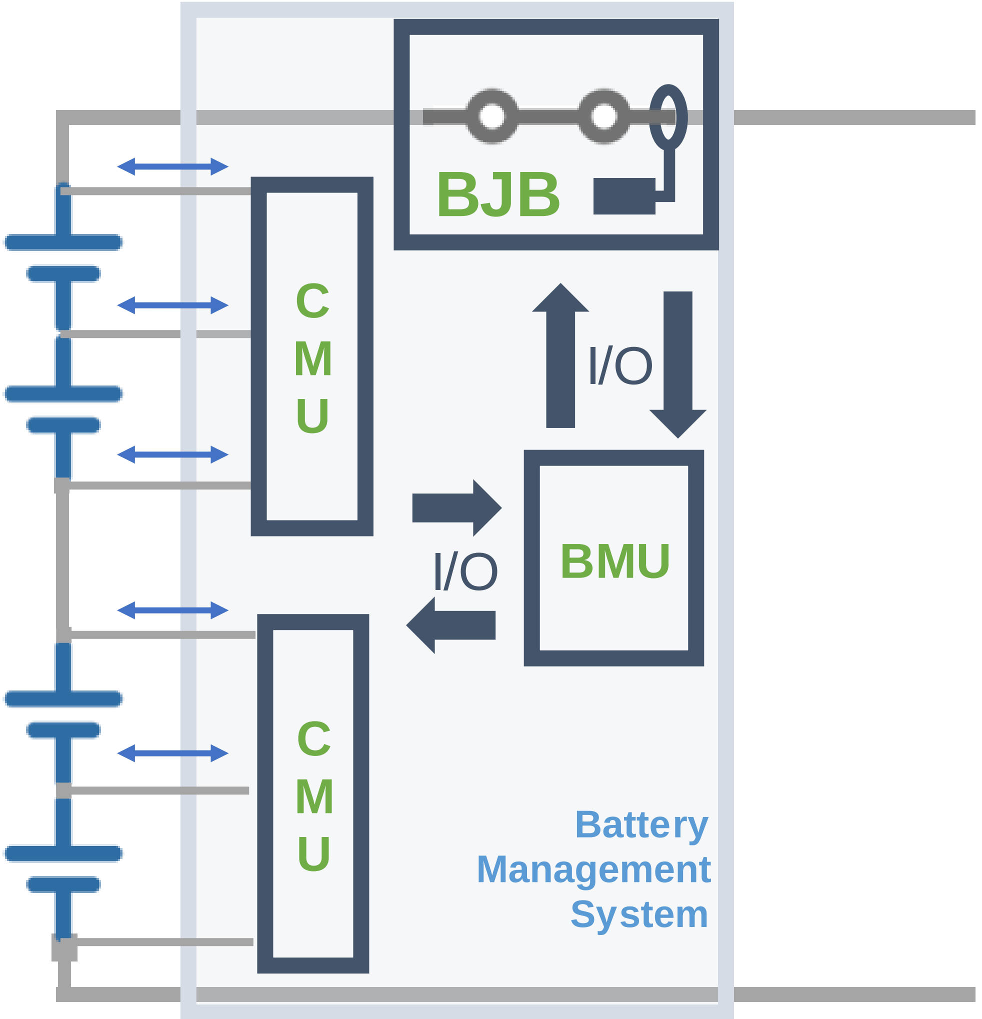
Typical Battery Management System Architecture

A BMS for a battery pack is typically composed of:

1) Battery Management Unit (BMU)
Centralized control of battery pack. Includes state estimation (SoC, SoH, SoX). Typically uses CAN as well as proprietary protocols to interface to CMU

2) Cell Management Units (CMU)
Takes care of cell balancing (active or passive) and measurement of individual cell voltages (1s) and temperatures.
Typically interfaced using proprietary communication protocols.

3) Battery Junction Box (BJB)
Switching unit connecting to the load that typically includes current sensors. May interface via CAN bus.



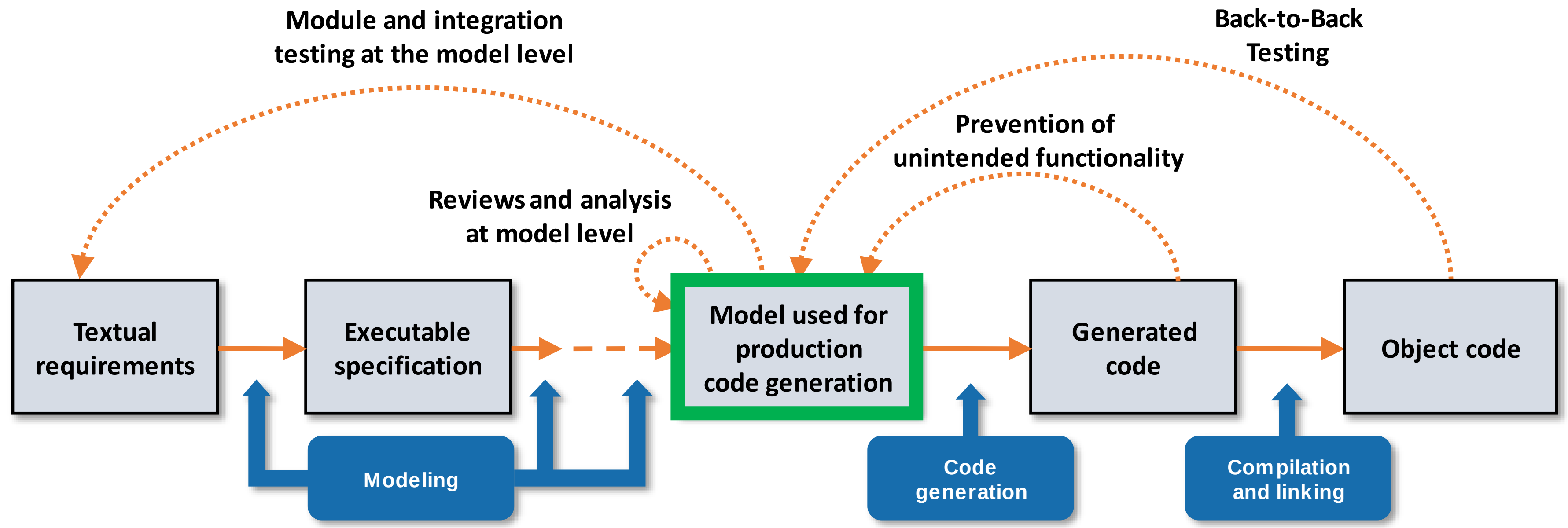
Model-Based Design Verification Workflow

Model Verification

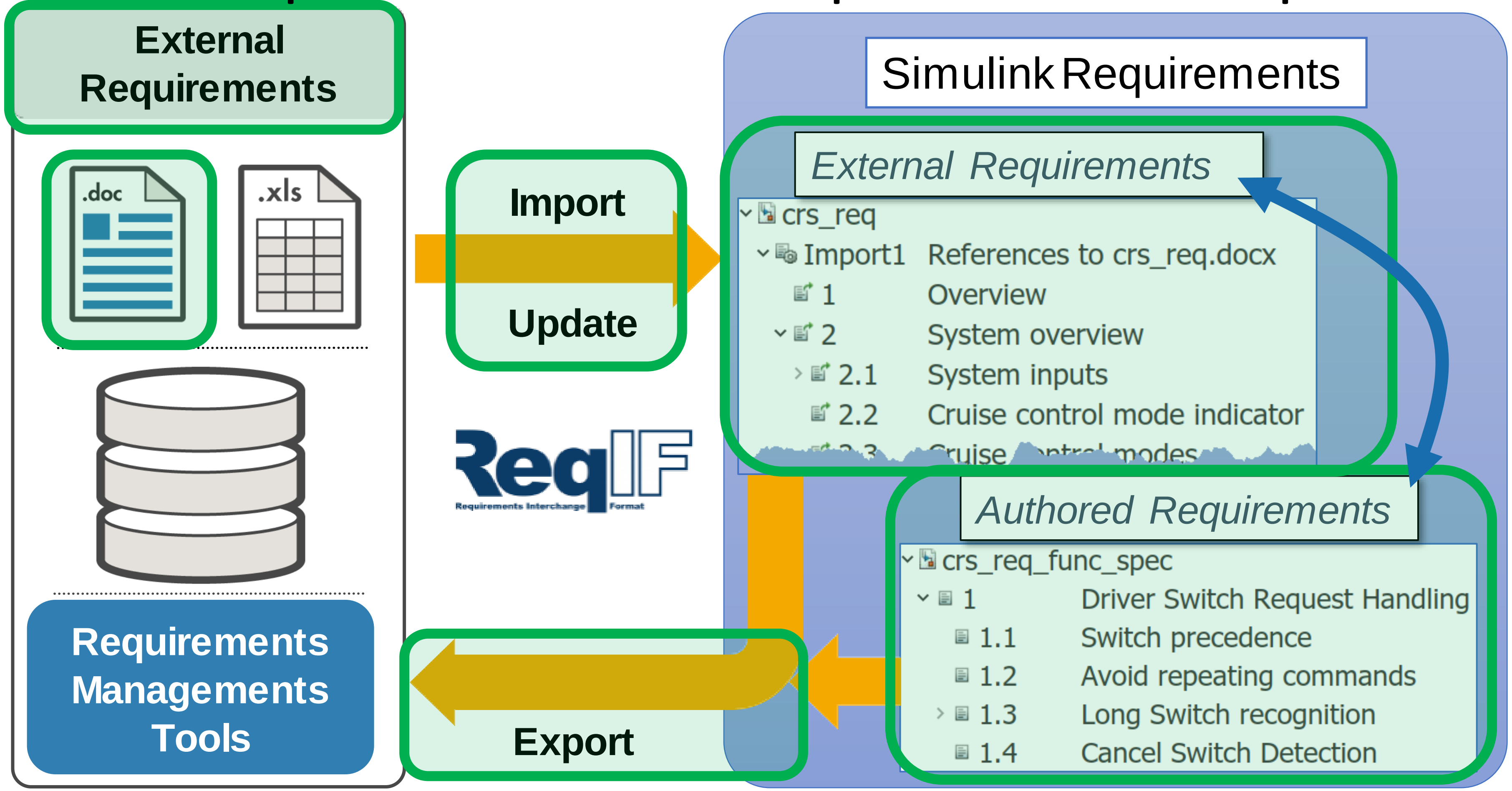
Discover design errors at design time

Code Verification

Gain confidence in the generated code

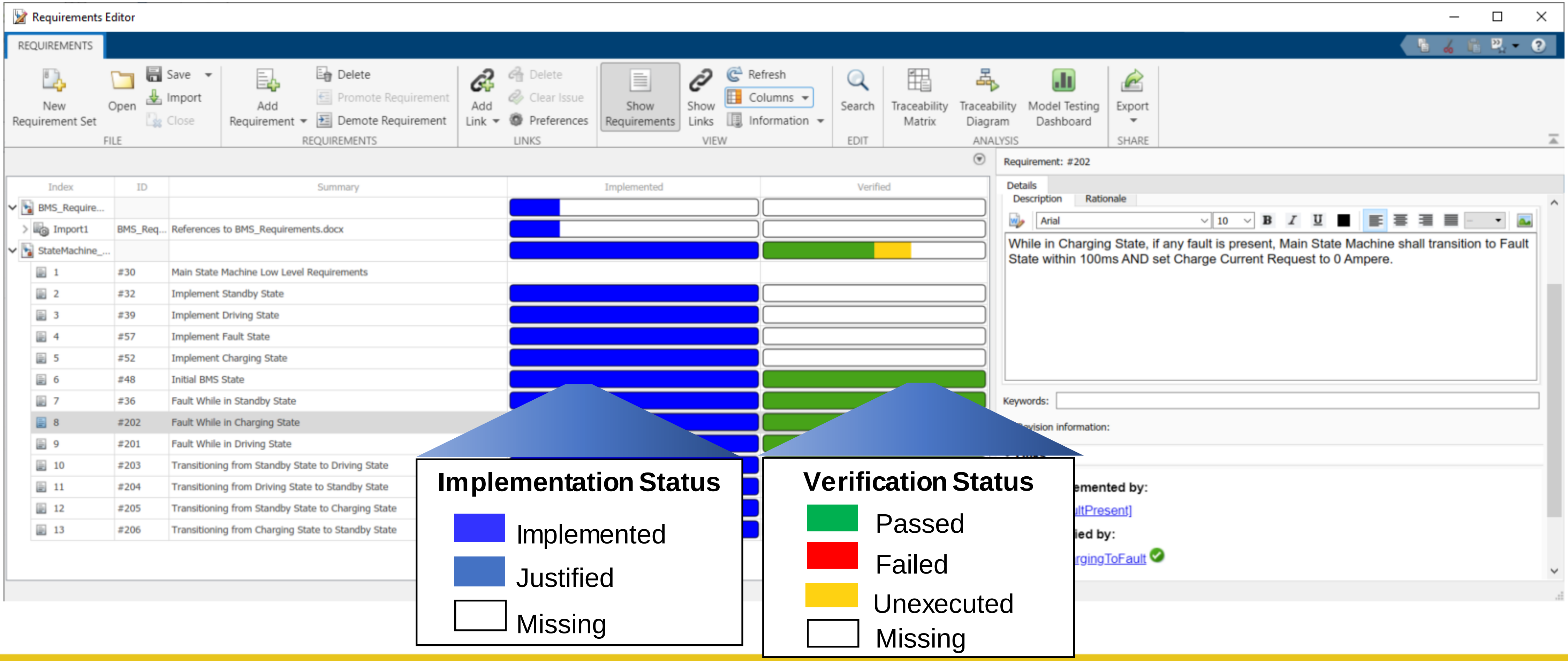


Requirements Import and Export

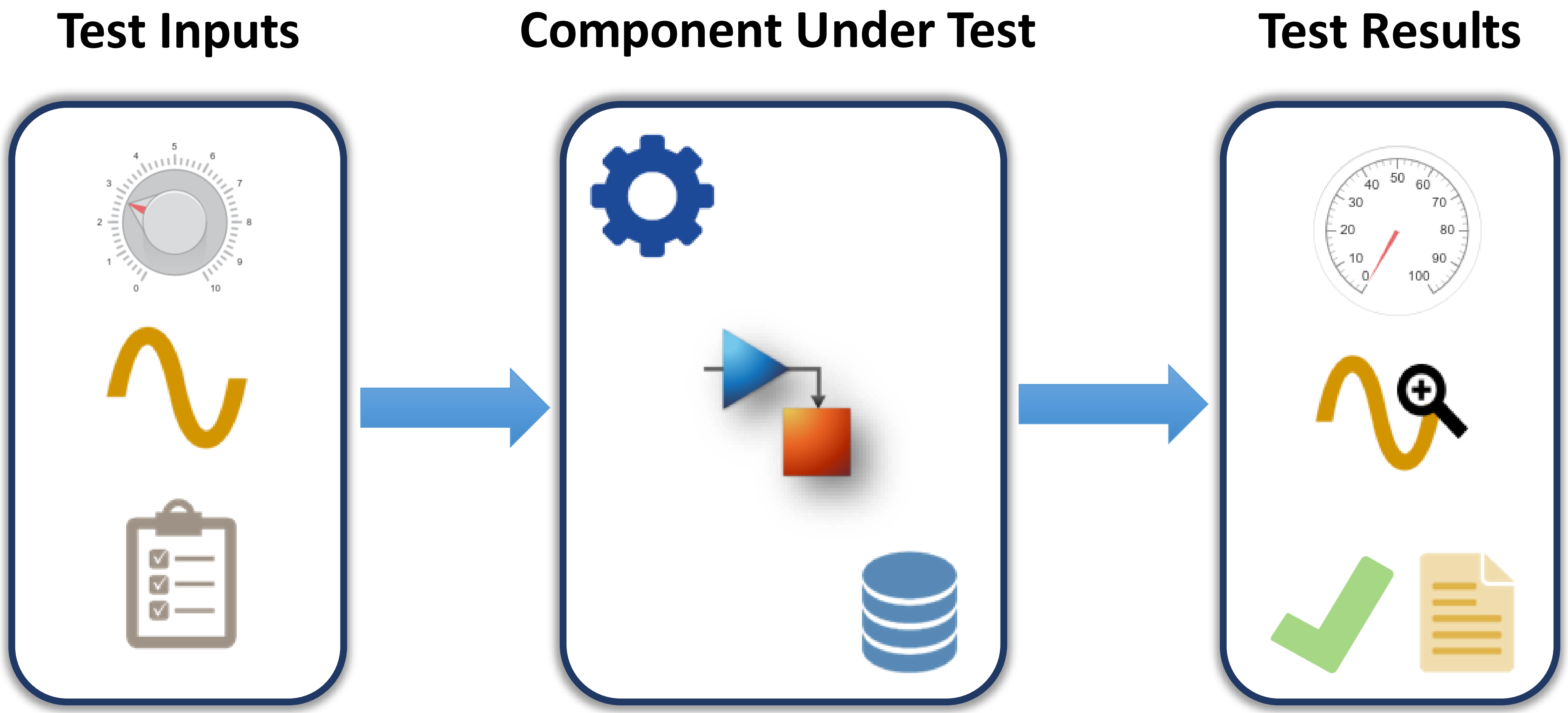


- Import from:
  - Word / Excel
  - IBM® Rational® DOORS®
  - ReqIF™ standard
- Update synchronizes changes from source
- Edit and add further details to import
- Author requirements
- Export ReqIF
  - Enables roundtrip with external tools

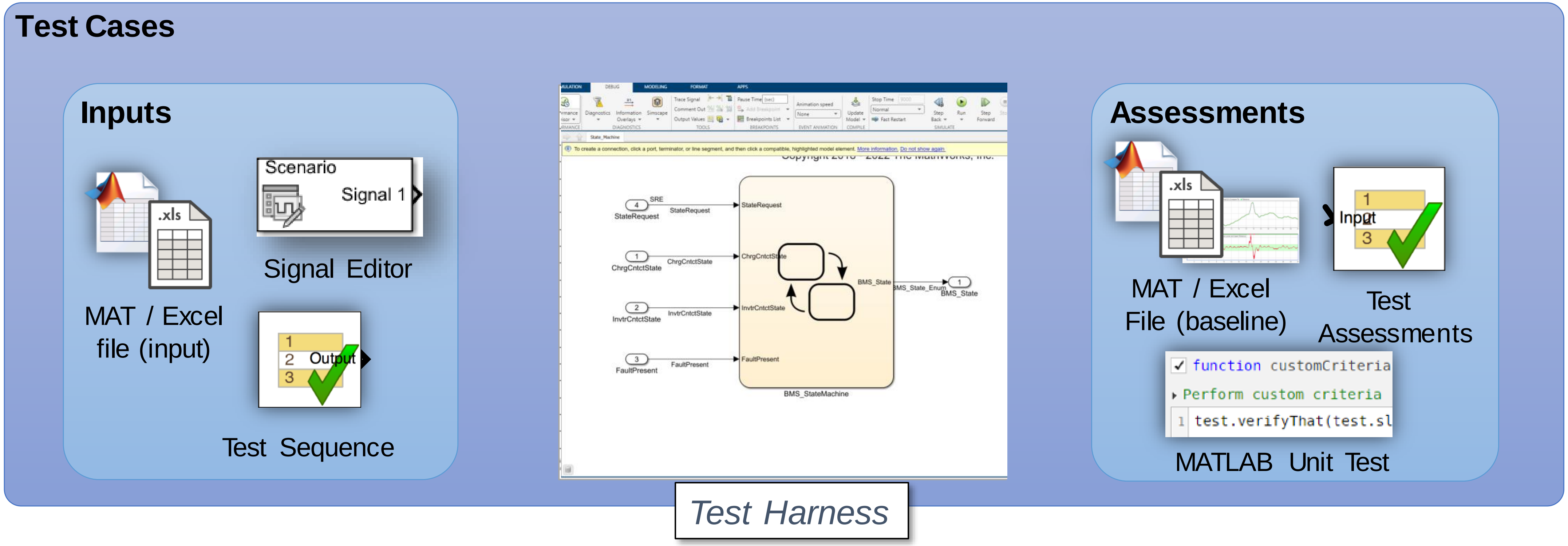
Manage Requirement Traceability



Systematic Functional Testing



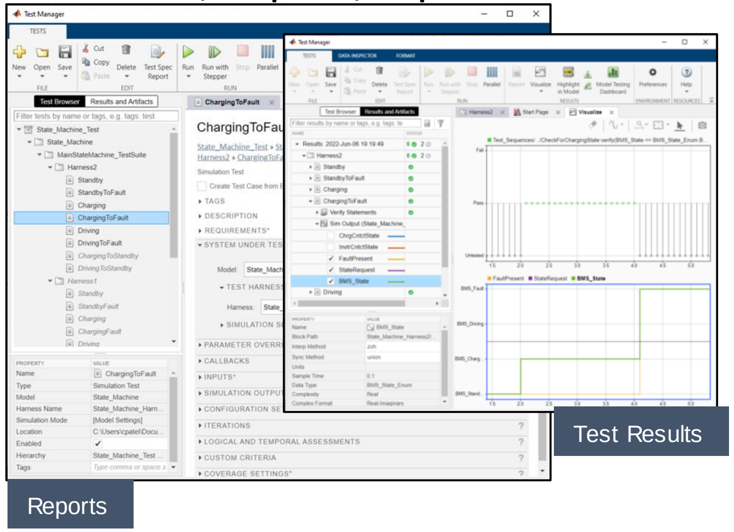
Create Test Harnesses



Test Management

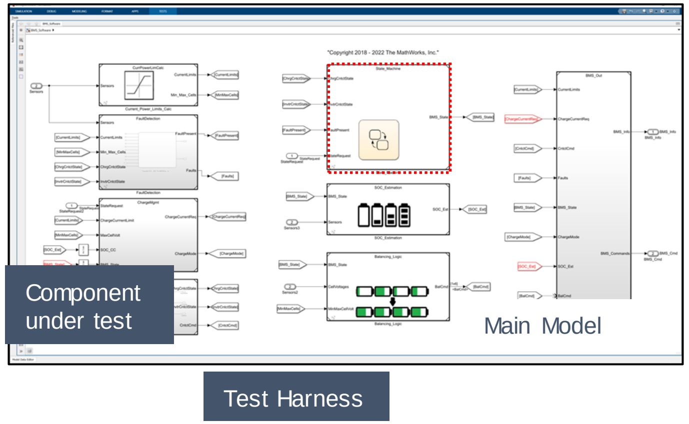
Test Manager

- Author, manage, organize tests
- Execute simulation, equivalence and baseline tests
- Review, export, report



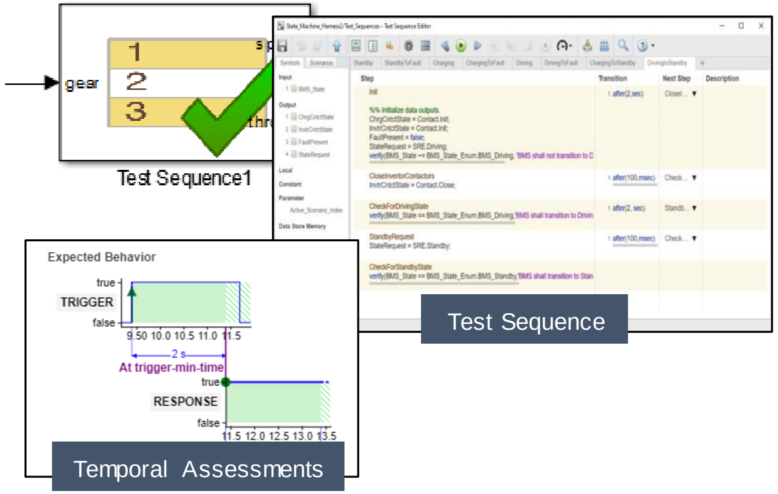
Test Harnesses

- Isolate Component Under Test
- Synchronized, simulation test environment



Test Authoring

- Specify test inputs, expected outputs, and tolerances
- Construct complex test sequences and assessments



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From Model to Embedded Hardware: SiL and PiL Verification

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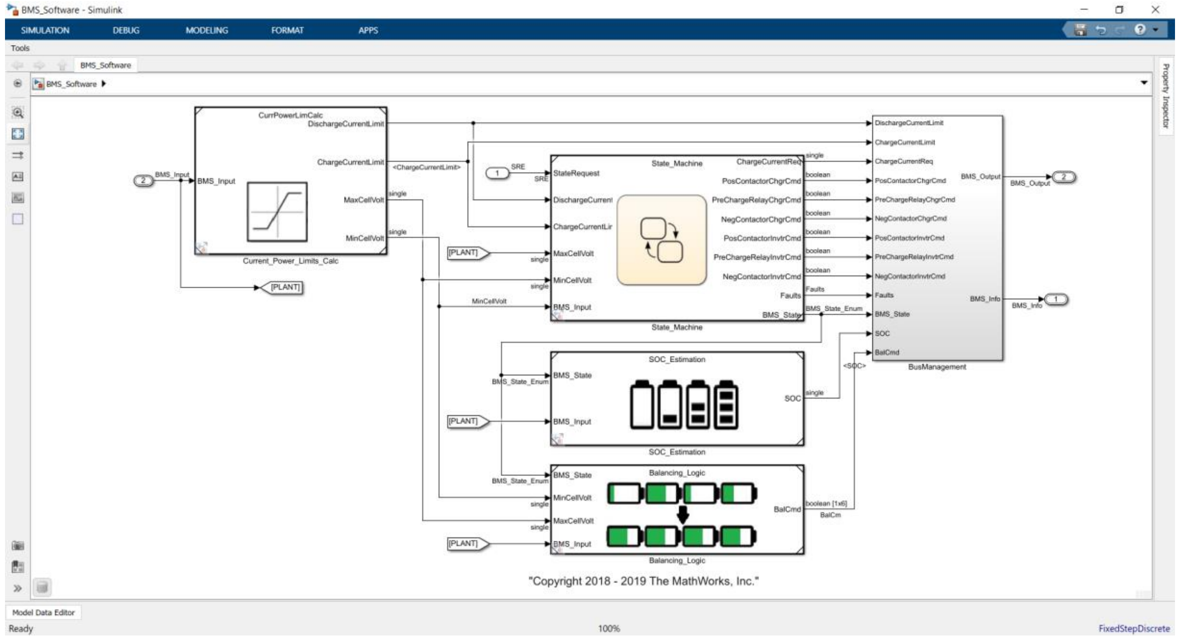
Hardware Aware Models



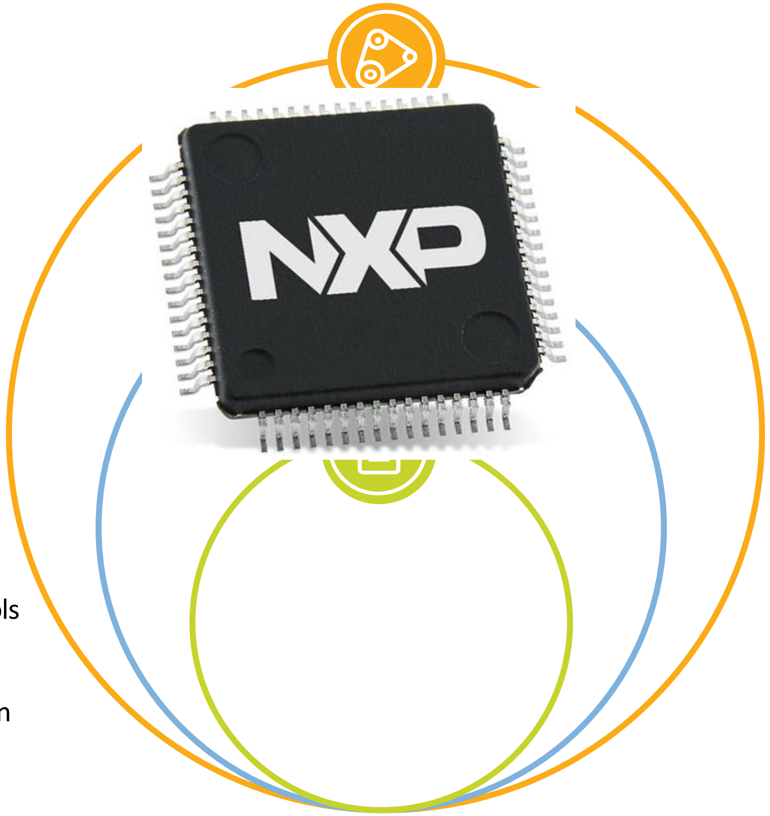
Embedded Applications Development Environment

DRIVERS, MIDDLEWARE, LIBRARIES

- Simplify hardware access by using hardware optimized software

CONFIGURATION, BUILD, DEBUG TOOLS

- Application development inside an IDE
- Build Tools, Debug Tools and Configuration Tools integrated within the IDE
- Drivers, Middleware and Libraries configuration and initialization in a graphical environment



REAL TIME MONITOR, DEMO TOOLS

- Check the status of the running on target application in real time
- Write and read variables, registers, memory locations
- Monitor signals on the embedded target
- Fast demo design

From Model to Embedded Hardware

MBDT

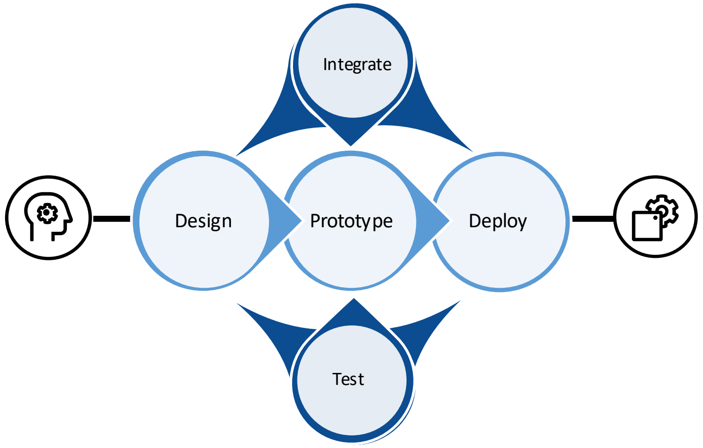
MODEL-BASED
DESIGN TOOLBOX

- Collection of Drivers, Libraries and Tools
- Embedded systems design and deployment on NXP MCUs directly from **Simulink**

MATHWORKS ECOSYSTEM
MATLAB/SIMULINK

- Model-Based Design
- Simulation
- Automatic Code Generation
- Verification and Validation

From Idea to Application



MBDT

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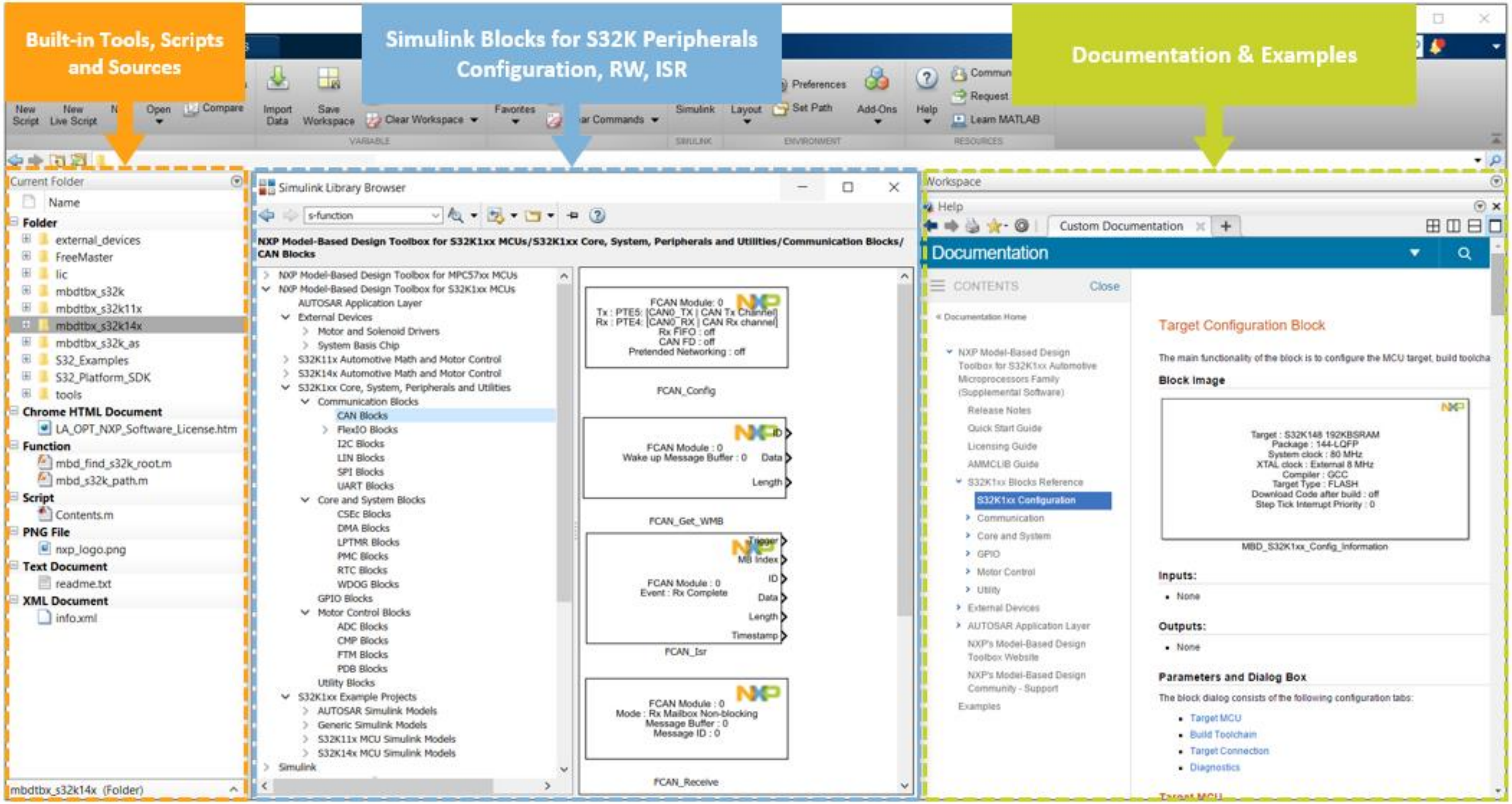
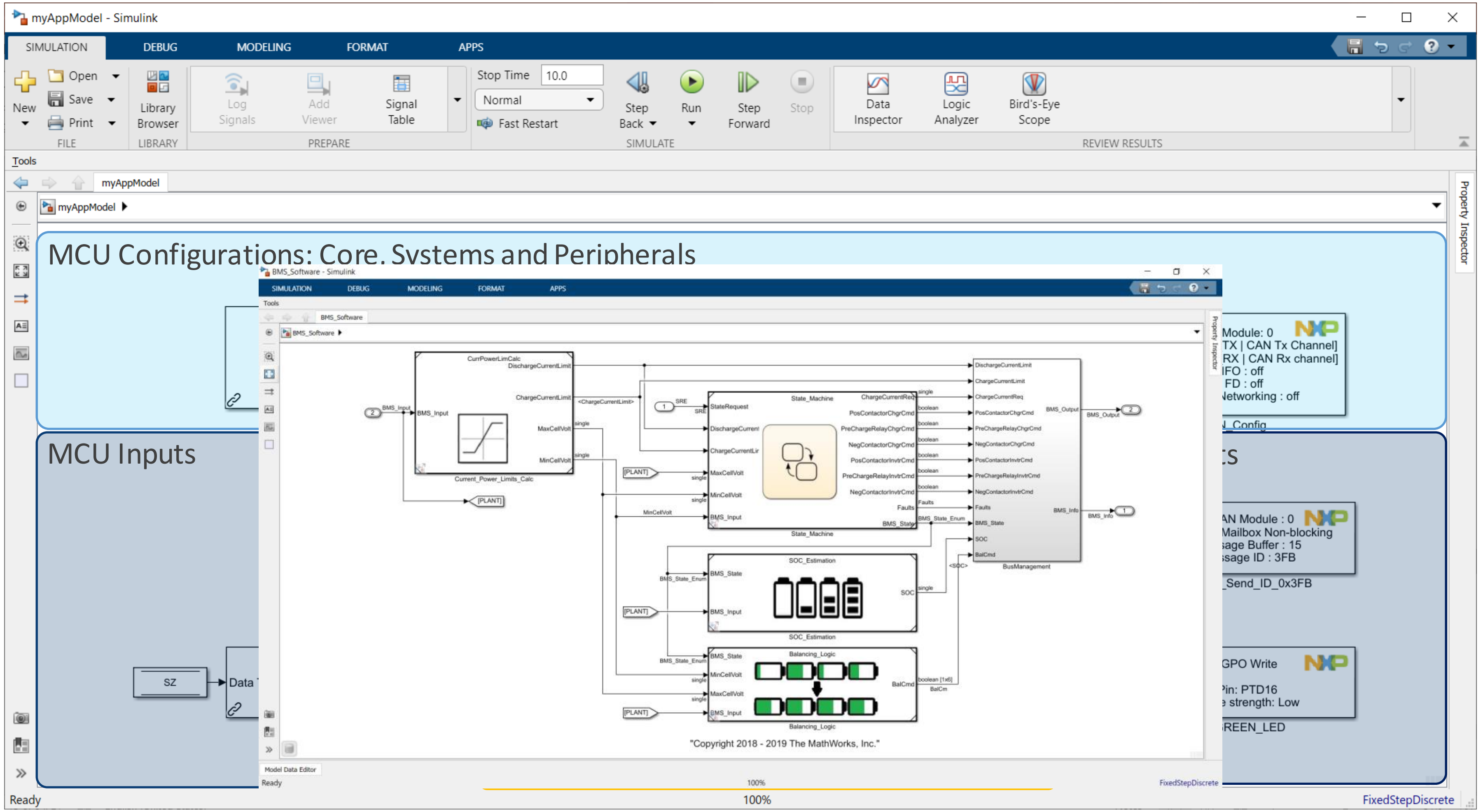
Model-Based Design Toolbox



Embedded Applications Development Flow



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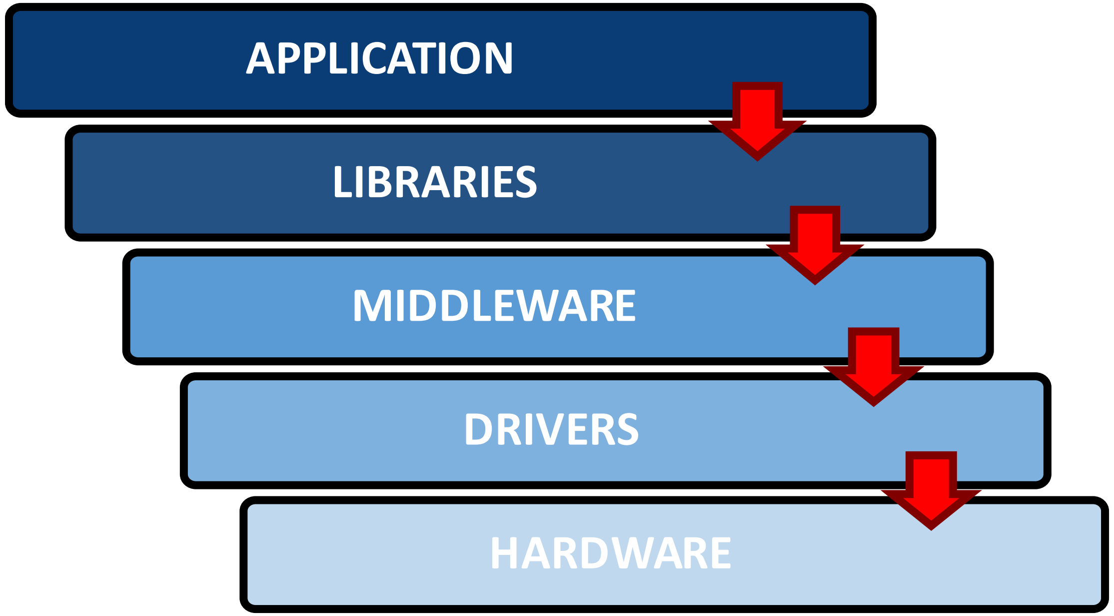
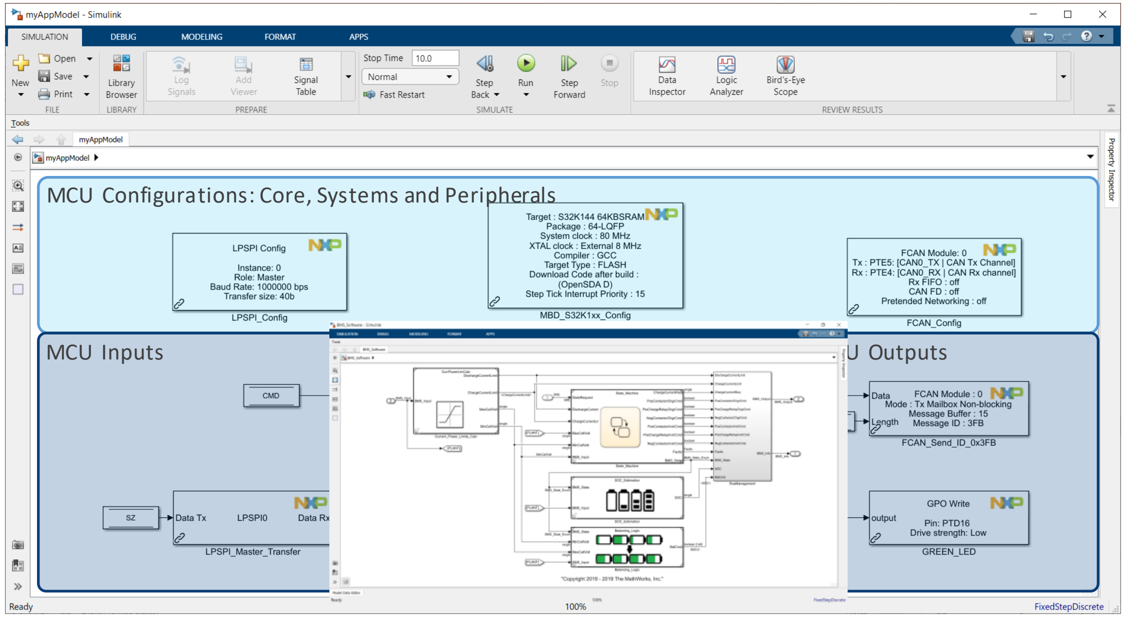
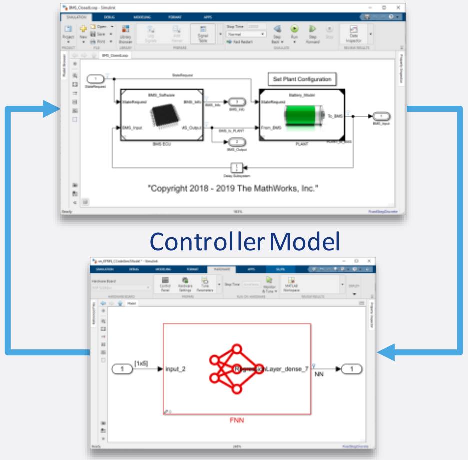




Virtual Field Testing

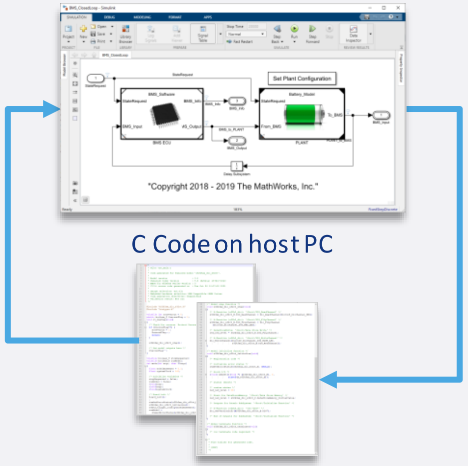
Model-in-the-Loop

Plant model with test signals



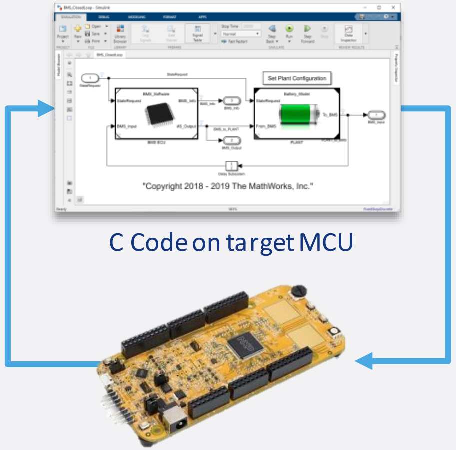
Software-in-the-Loop

C code with test signals



Processor-in-the-Loop

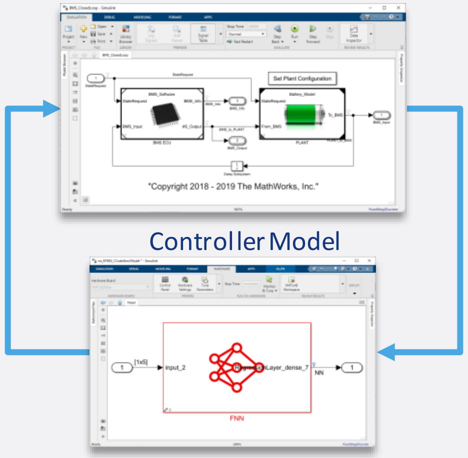
Embedded code with test signals



Virtual Field Testing

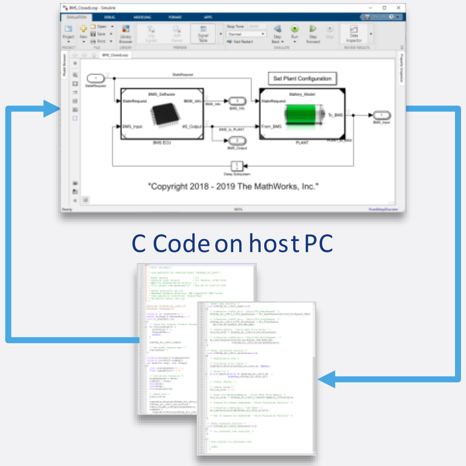
Model-in-the-Loop

Plant model with test signals



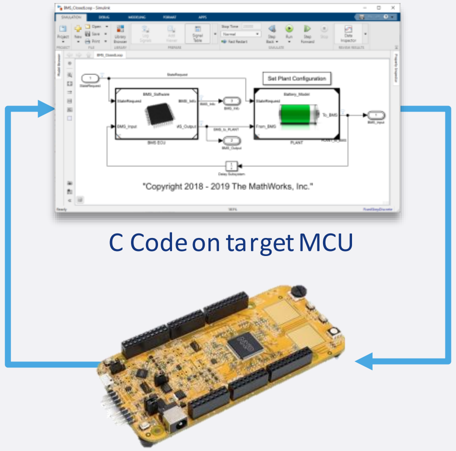
Software-in-the-Loop

C code with test signals



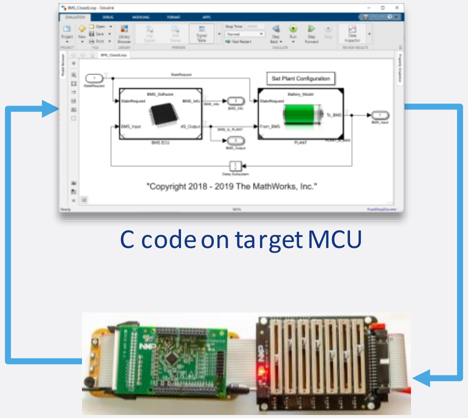
Processor-in-the-Loop

Embedded code with test signals



External Mode

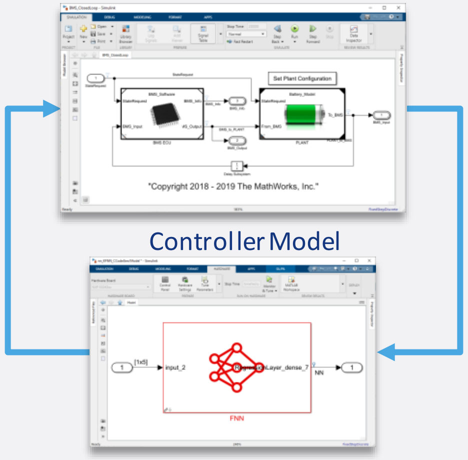
Device monitoring



Virtual Field Testing

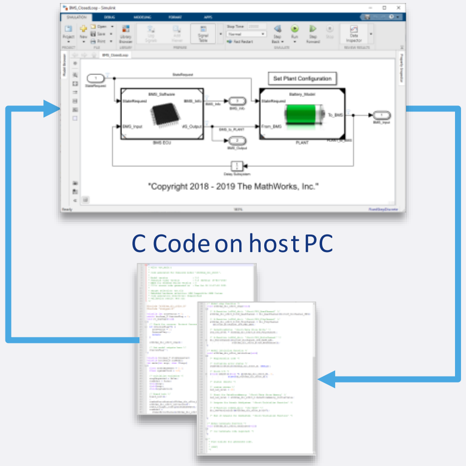
Model-in-the-Loop

Plant model with test signals



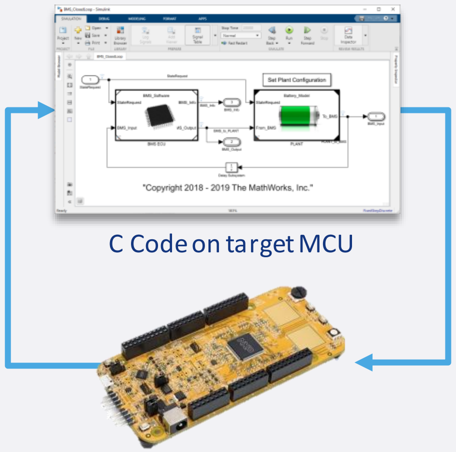
Software-in-the-Loop

C code with test signals



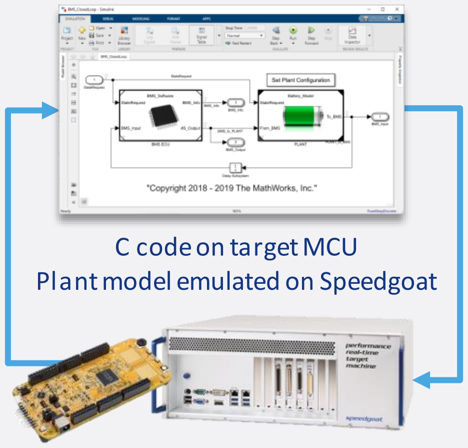
Processor-in-the-Loop

Embedded code with test signals

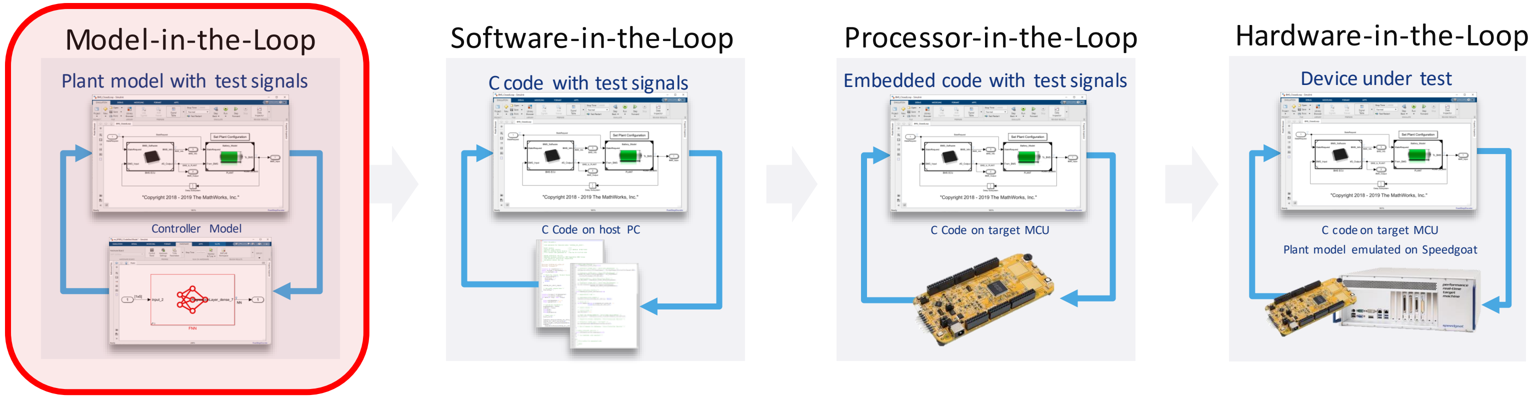


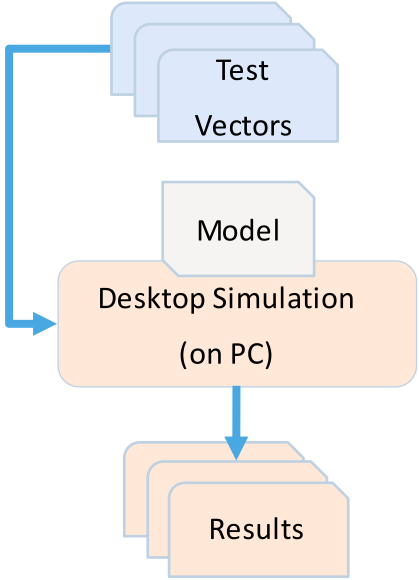
Hardware-in-the-Loop

Device under test

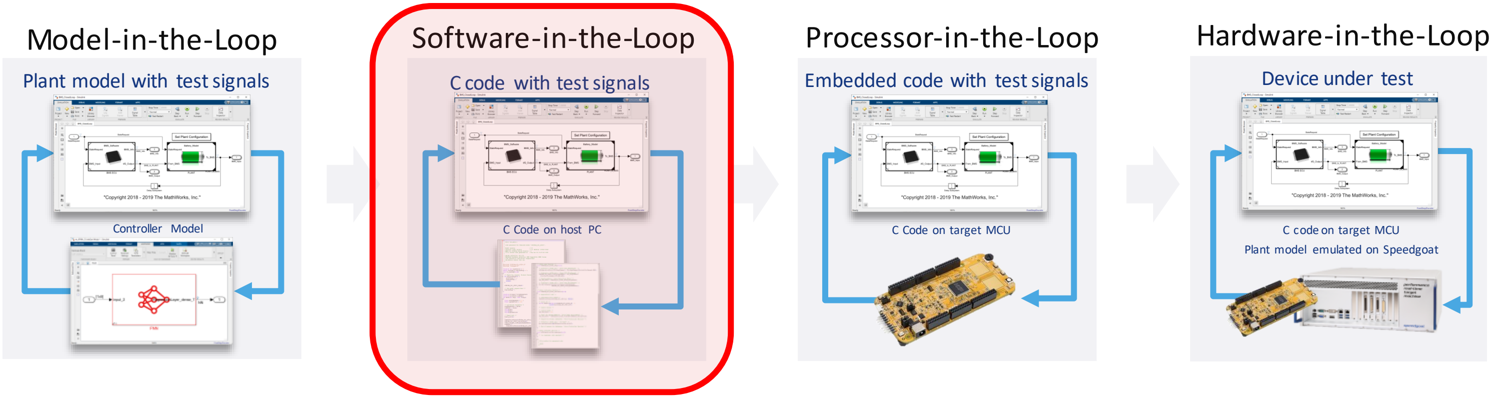


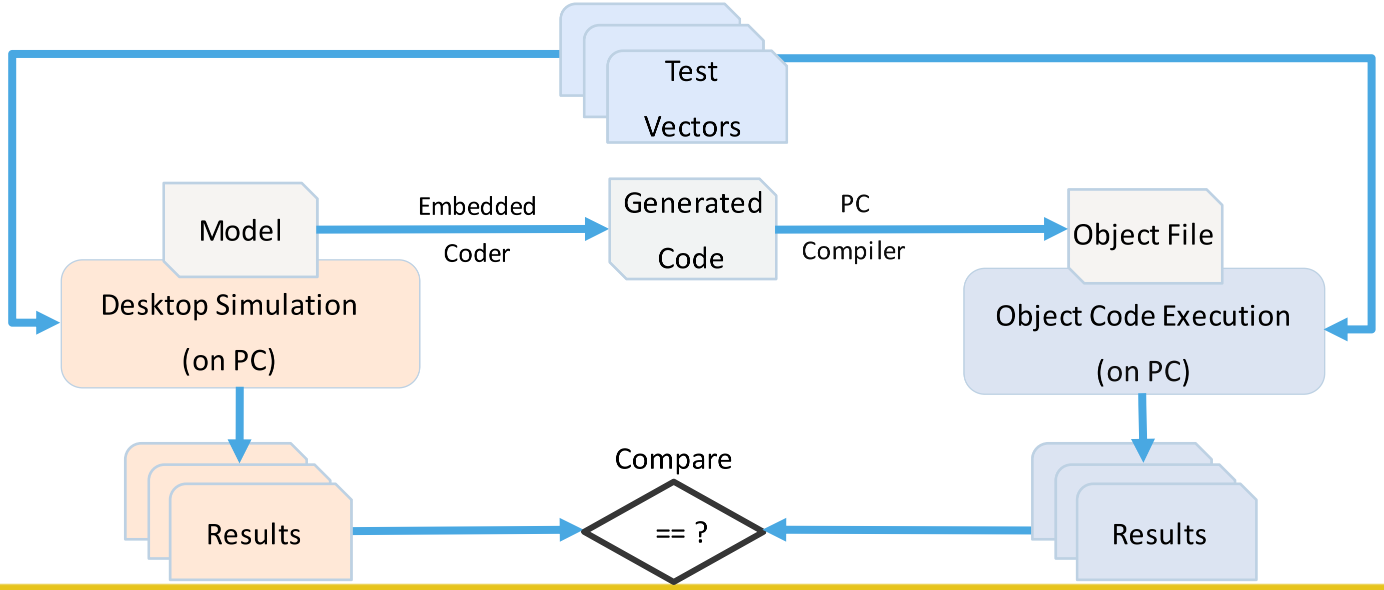
MiL - SiL - PiL - HiL



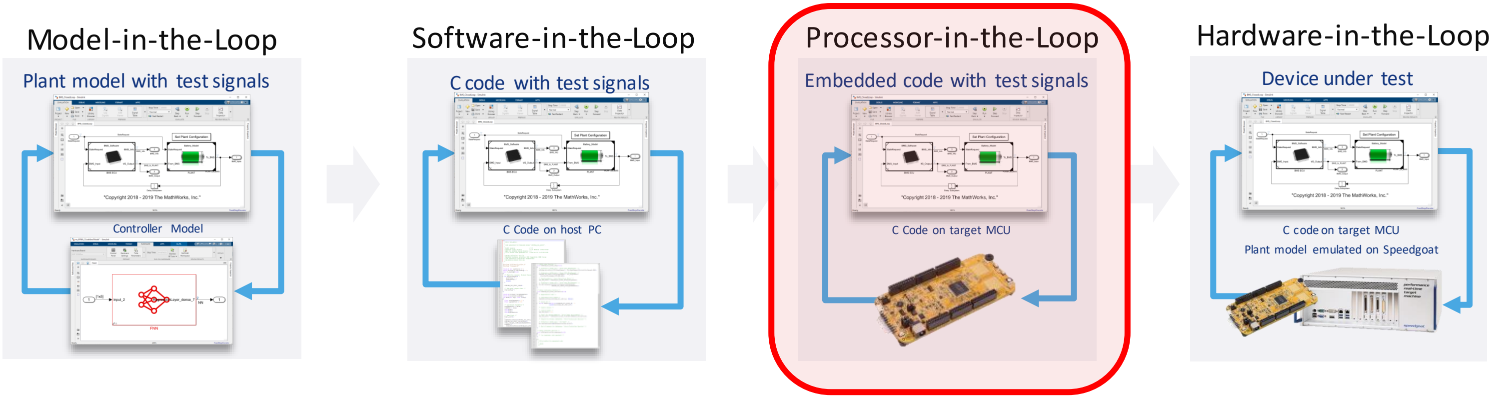


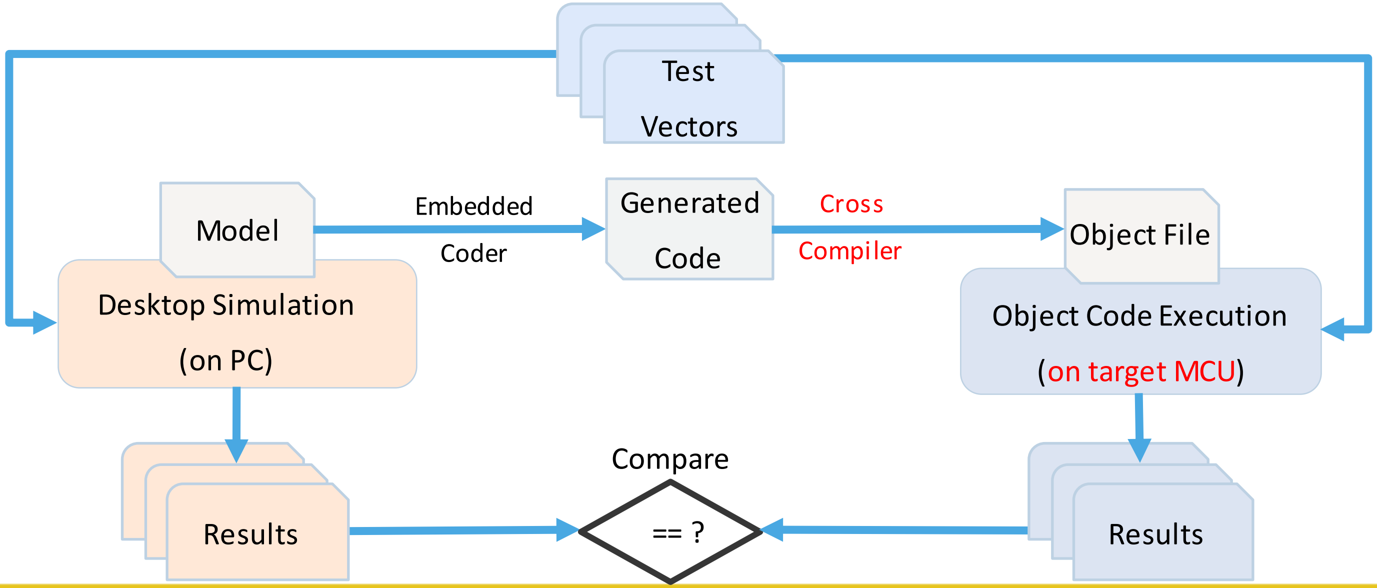
MiL - SiL - PiL - HiL



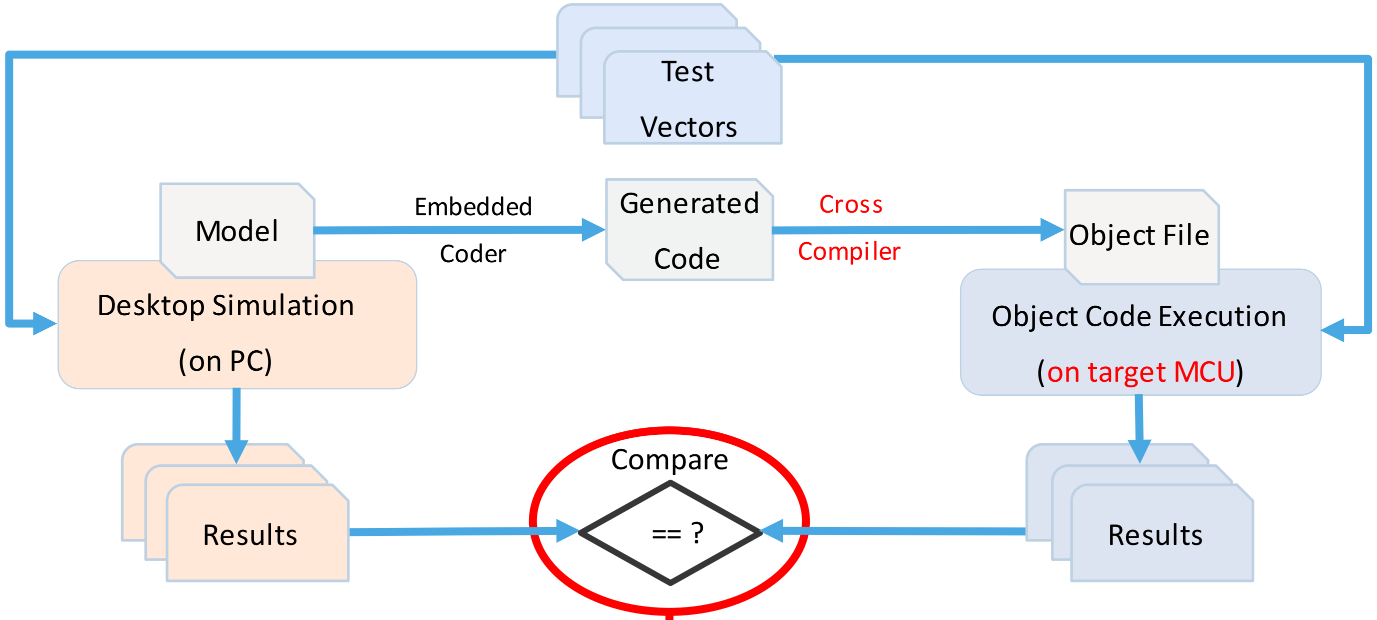


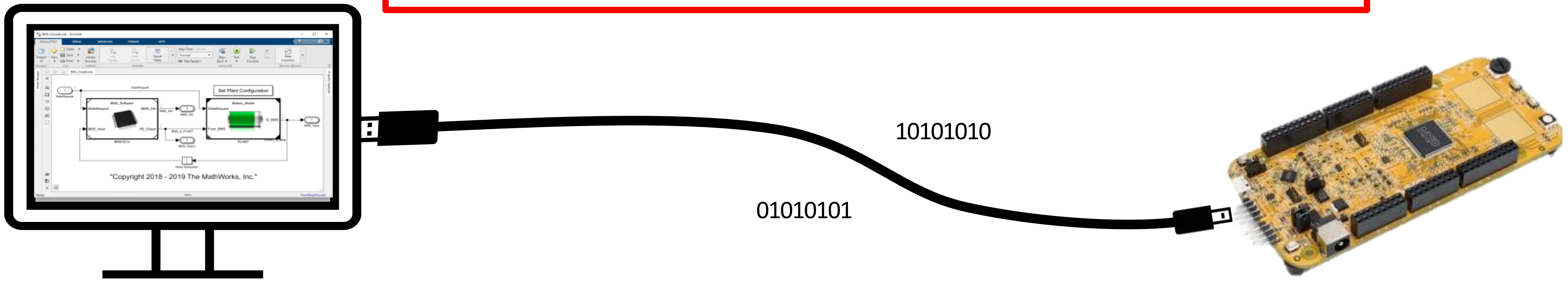
MiL - SiL - PiL - HiL

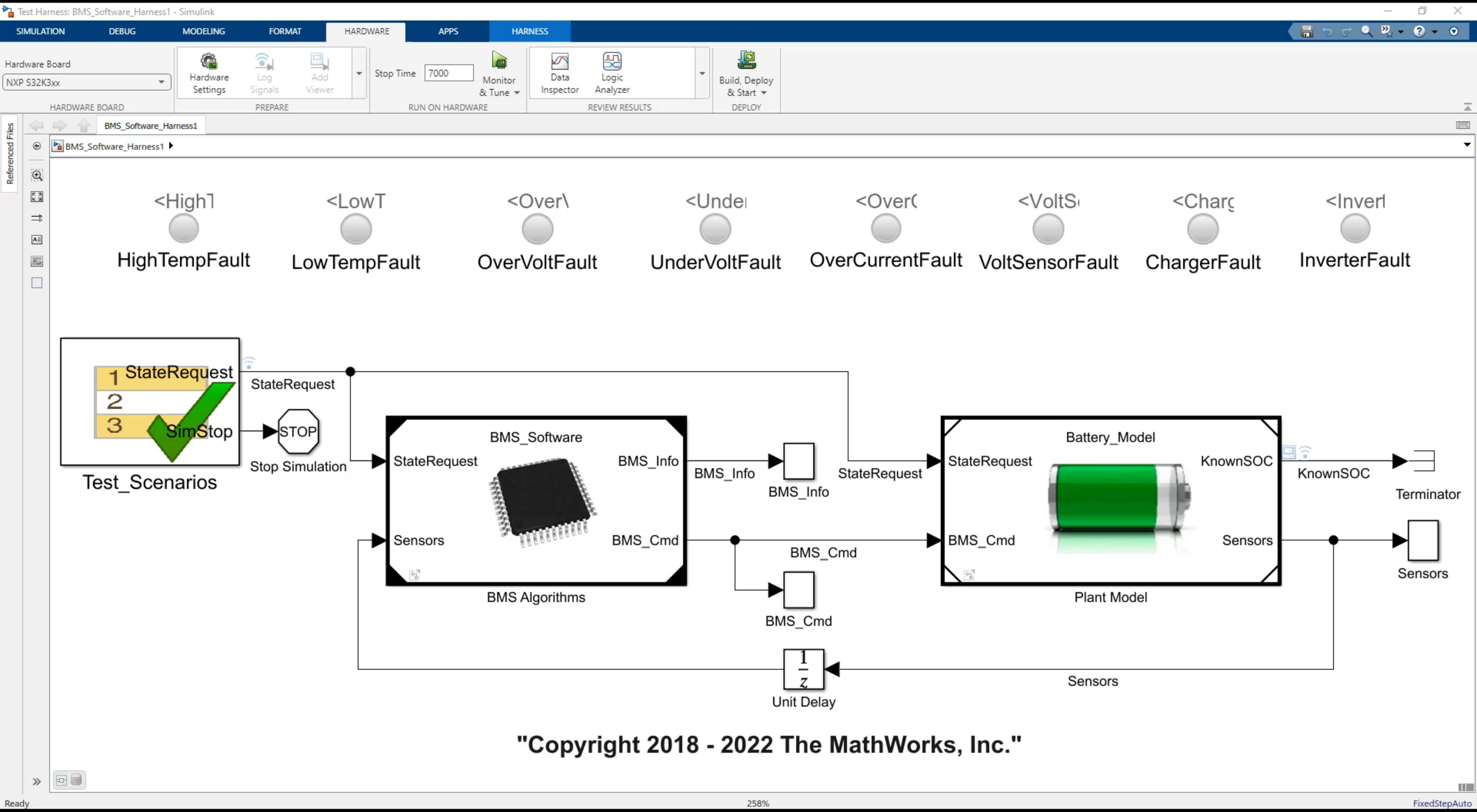




MiL and PiL Equivalence Test






Test Harness: BMS_Software_Harness1 - Simulink
SIMULATION
DEBUG
MODELING
FORMAT
HARDWARE
APPS
HARNESS
Hardware Board
NXP S32K3xx
Hardware Settings
Log Signals
Add Viewer
Stop Time
7000
Monitor & Tune
Data Inspector
Logic Analyzer
Build, Deploy & Start
HARDWARE BOARD
PREPARE
RUN ON HARDWARE
REVIEW RESULTS
DEPLOY
BMS_Software_Harness1
Referenced Files
HighTempFault
LowTempFault
OverVoltFault
UnderVoltFault
OverCurrentFault
VoltSensorFault
ChargerFault
InverterFault
StateRequest
SimStop
Test_Scenarios
STOP
Stop Simulation
BMS_Software
BMS_Info
BMS_Cmd
Sensors
BMS Algorithms
Battery_Model
KnownSOC
Plant Model
Terminator
Unit Delay
"Copyright 2018 - 2022 The MathWorks, Inc."
Ready
258%
FixedStepAuto

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Real-Time Verification with HiL Testing

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SYSTEMS INITIATIVE

Real-Time Systems for BMS Testing

REQUIREMENTS

C or HDL Code generated from plant model

DESKTOP SIMULATION

SYSTEM MODEL

Plant
Batteries, loads, cell balancing electronics, batteries, passive circuit components

Controller
Algorithms for energy and thermal management

REAL-TIME SIMULATION
REAL-TIME DEVELOPMENT PLATFORM

HARDWARE PROTOTYPE
Battery packs, power electronics, electrical loads, fast charging

HARDWARE-IN-THE-LOOP SIMULATION
Behavioural model running on a real-time computer with virtual battery cells and packs

Real-time communication

RAPID CONTROL PROTOTYPING
ol algorithms running on a real-time computer, microcontroller, or Simulink-programmable FPGA

C or HDL Code generated from controller model

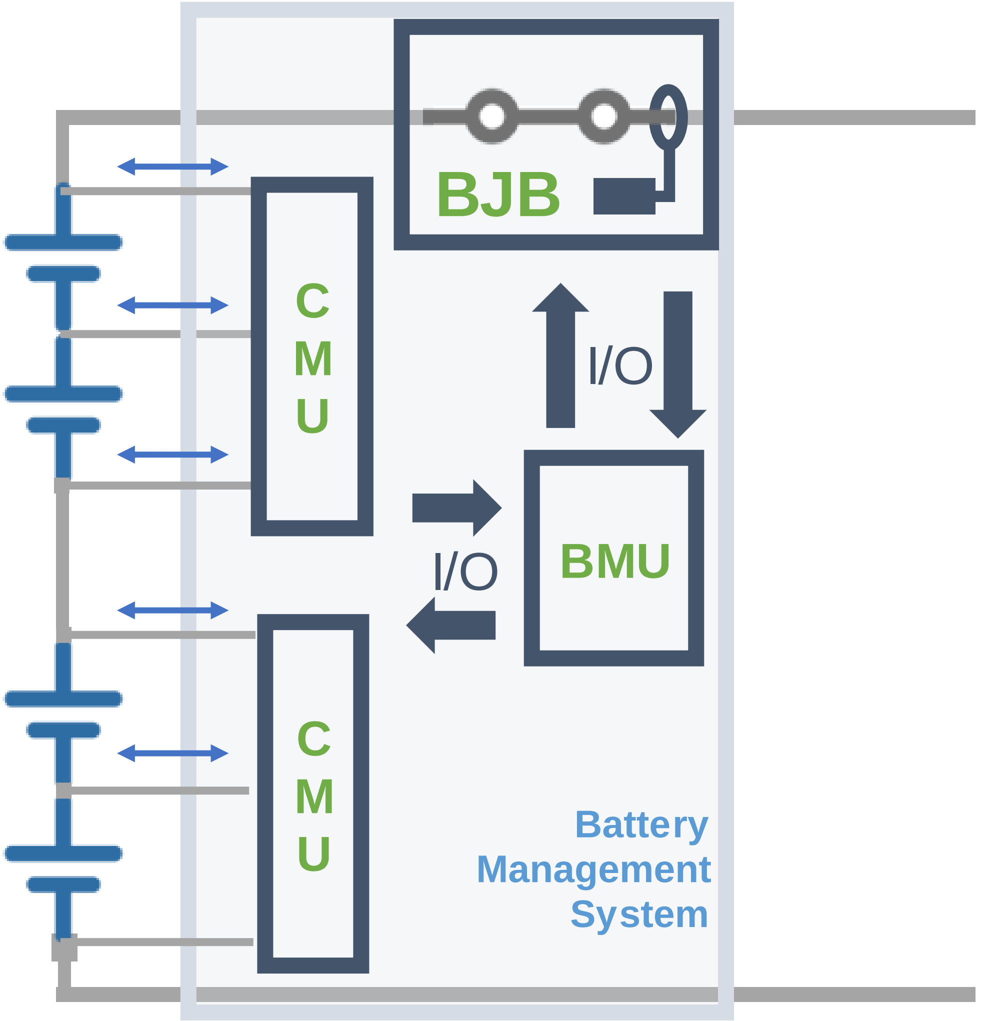
Typical Battery Management System Architecture

A BMS for a battery pack is typically composed of:

1) Battery Management Unit (BMU)
   Centralized control of battery pack. Includes state estimation (SoC, SoH, SoX). Typically uses CAN as well as proprietary protocols to interface to CMU

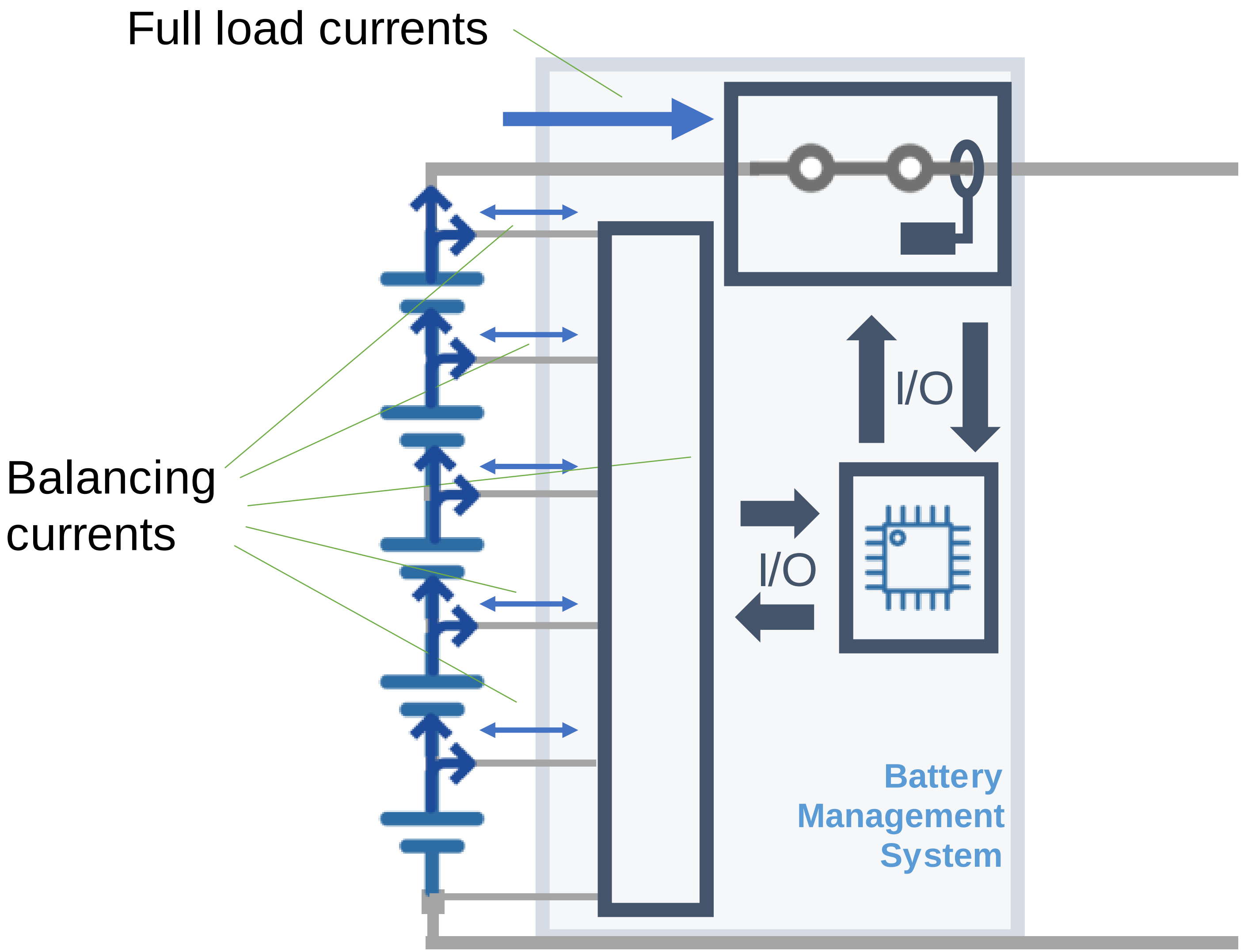
2) Cell Management Units (CMU)
   Takes care of cell balancing (active or passive) and measurement of individual cell voltages (1s) and temperatures.
   Typically interfaced using proprietary communication protocols.

3) Battery Junction Box (BJB)
   Switching unit connecting to the load that typically includes current sensors. May interface via CAN bus.



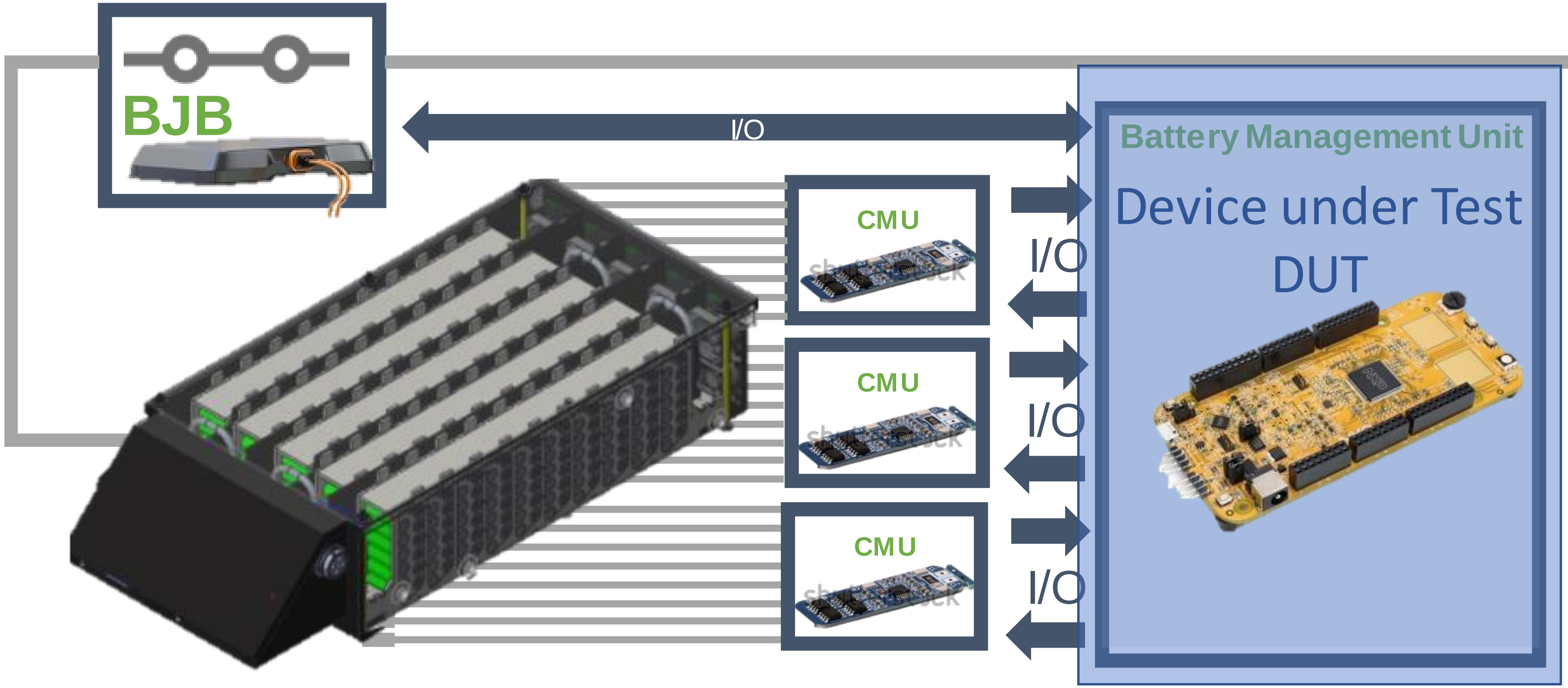
BMS Currents

- **Full load currents:** linked to load or charger. Typically in the range of hundreds of Amperes for EVs
- **Balancing currents:** Currents flowing through cell balancing circuit. Such circuit could be passive (discharge cells) or active (redistribute charge). Typically between 100mA and 5A.



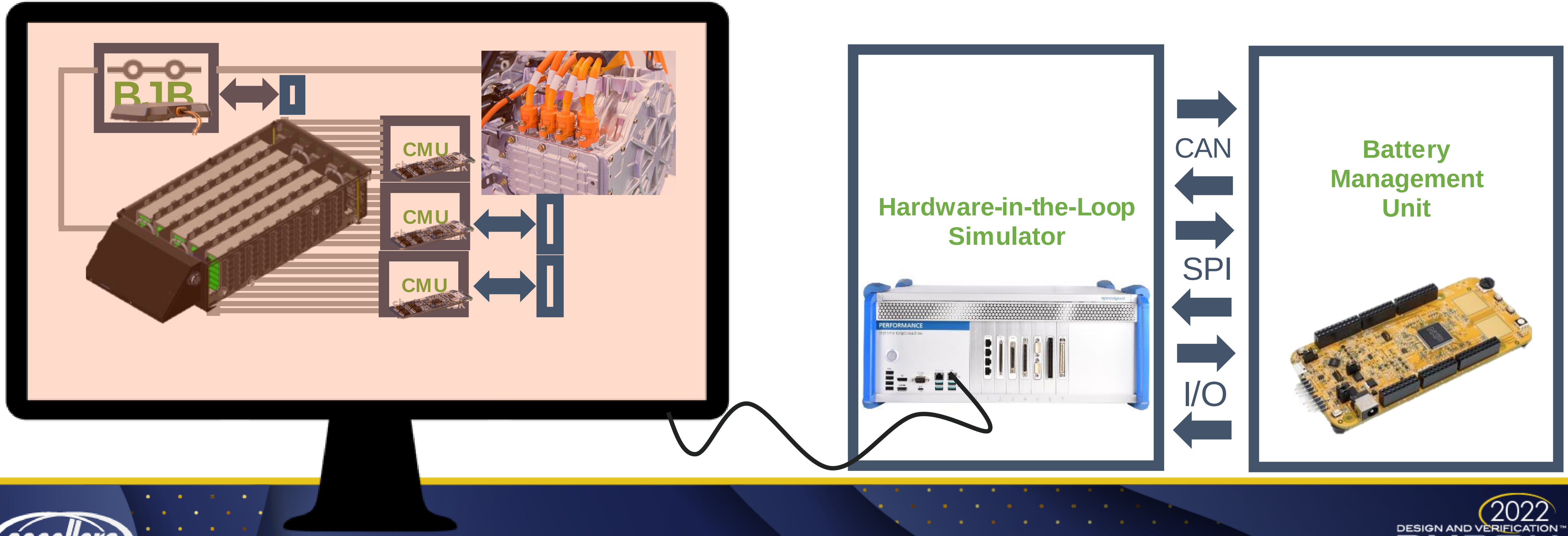
HIL Testing of BMU

- **Device under Test (DUT):** technique to test embedded control systems where part of the plant is simulated.



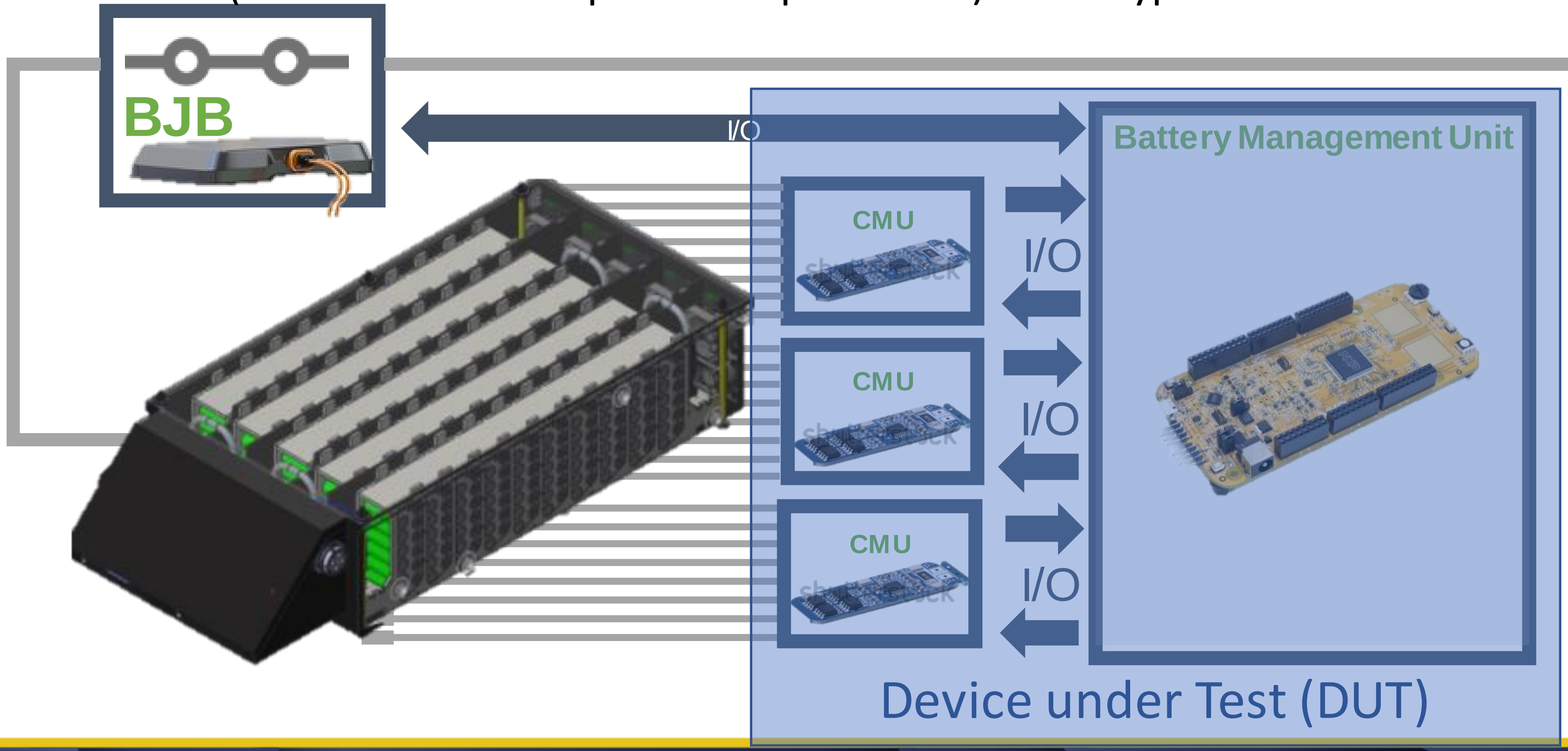
HIL Testing of BMU

- **Hardware-in-the-Loop Testing:** technique to test embedded control systems where part of the plant is simulated.



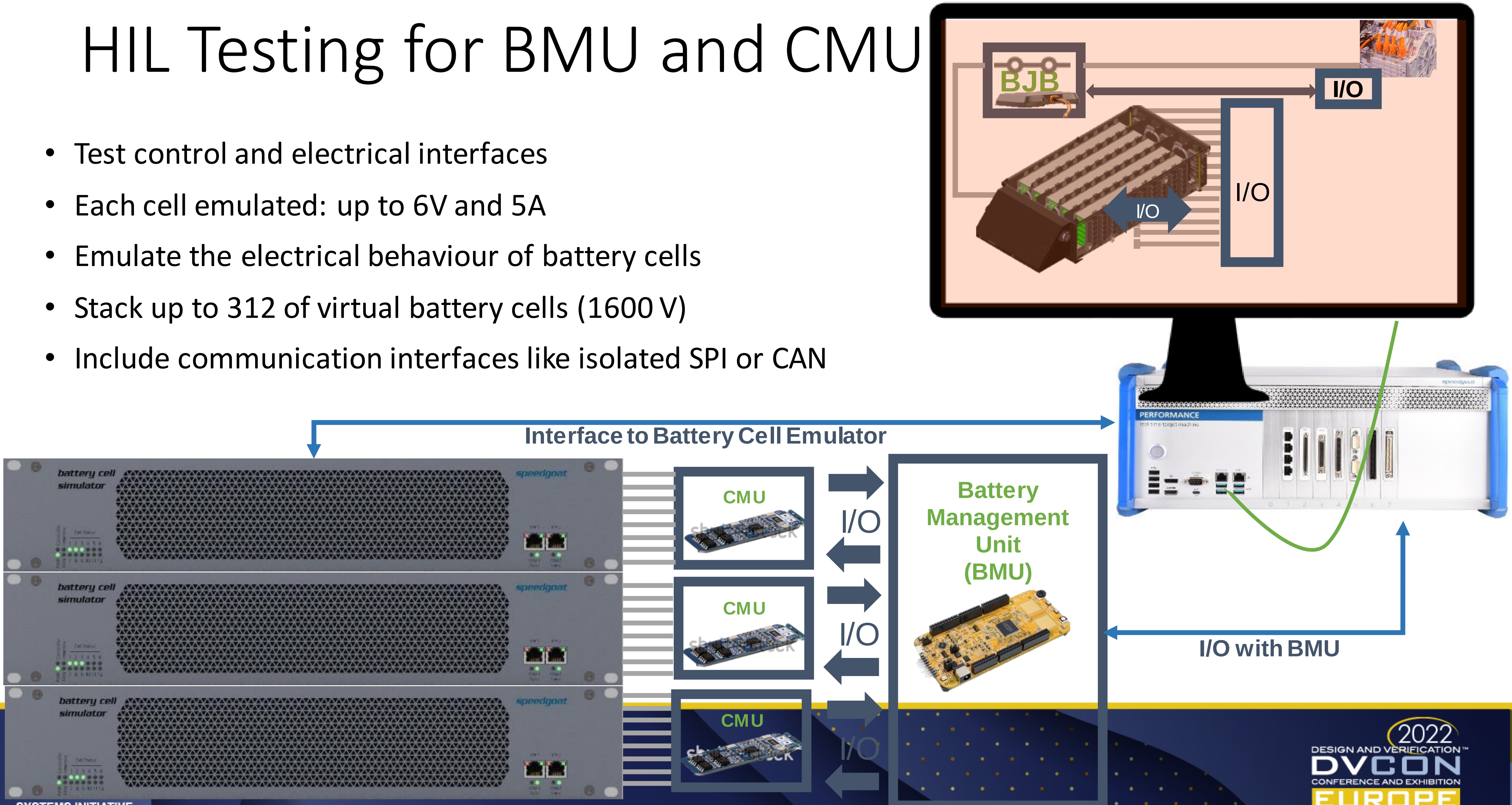
HIL Testing of BMU and CMU

- **Cell emulation:** mimic the battery cell electrical power (voltage and current) using a real-time simulation (HIL simulator and power amplification). It is a type of Power HIL.



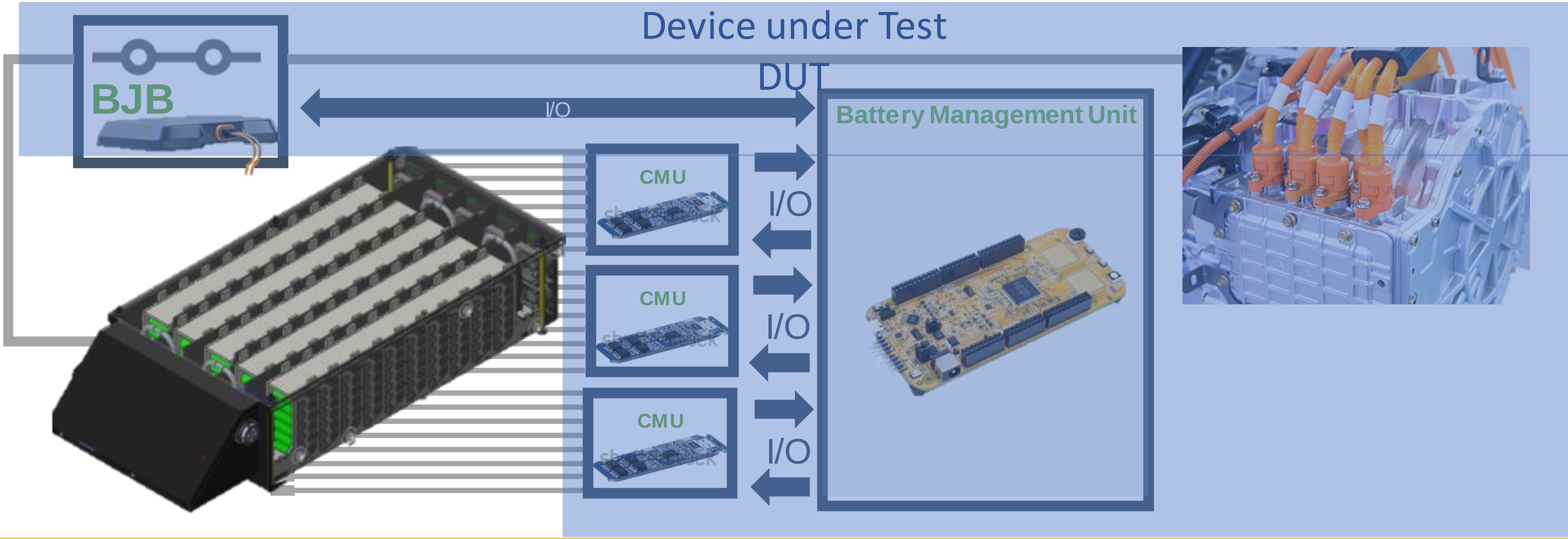
HIL Testing for BMU and CMU

- Test control and electrical interfaces
- Each cell emulated: up to 6V and 5A
- Emulate the electrical behaviour of battery cells
- Stack up to 312 of virtual battery cells (1600 V)
- Include communication interfaces like isolated SPI or CAN

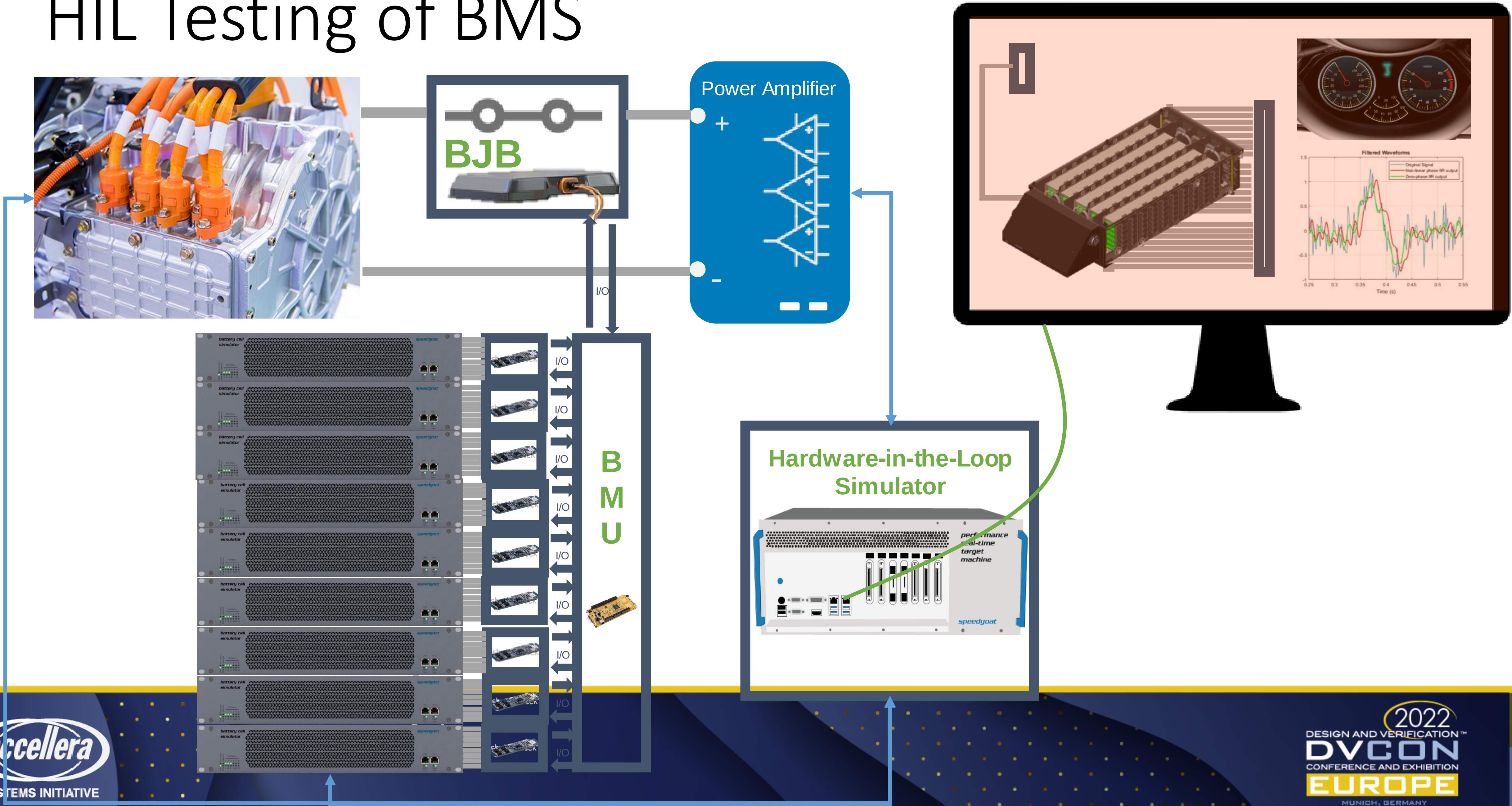


HIL Testing of full BMS and load

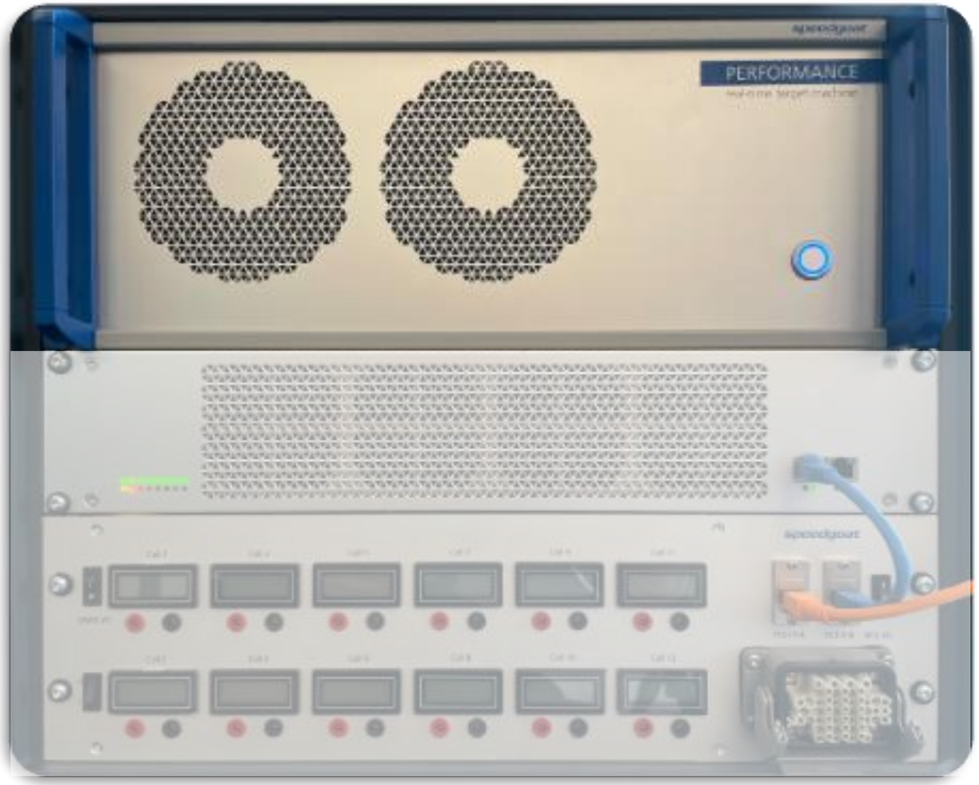
Device under Test can also include the real load (e.g. powertrain or EV charger). The interfaces include electrical power



HIL Testing of BMS

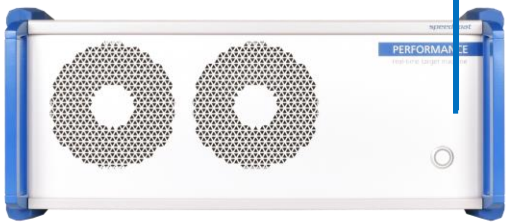


Real-Time Simulator



Built for High-Performance
- Multicore CPU
- Simulink-programmable FPGAs

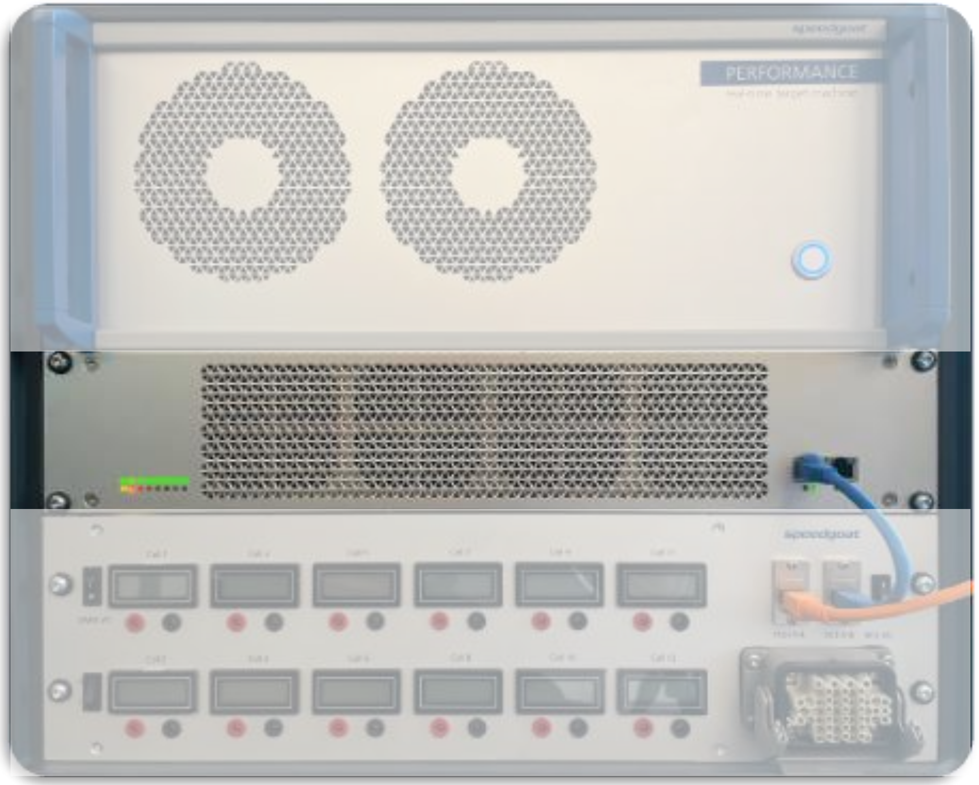
Front-view



Rear-view

Battery Emulation I/O
- Serial and bus communication (SPI, CAN, UART)
- Cell temperature emulation
- Shunt emulation
- Cell controller emulation
- Fault insertion

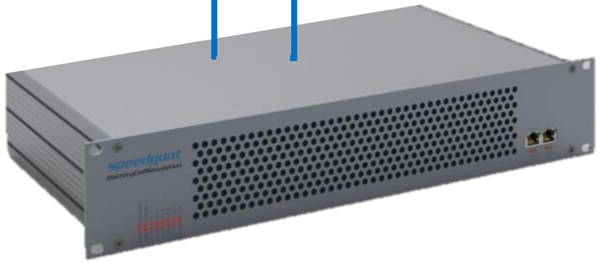
Battery Cell Emulator



Small to Large BMS test systems
- 12 cell per unit
- Stack up to 312 cells
- Voltage isolation of 1.6 kV

Cell-level emulation and measurement
- Simulate up to 8V
- Sink and source current up to 5A

Front

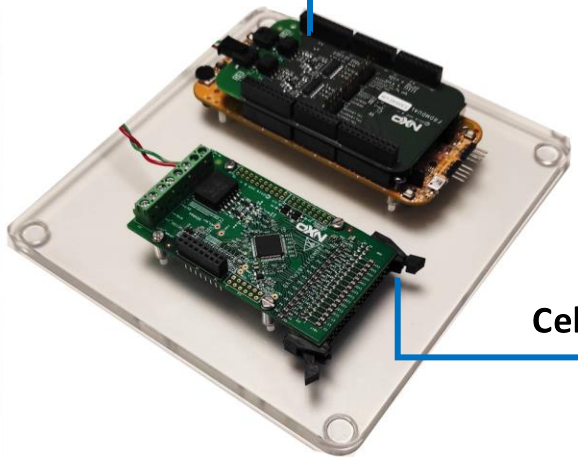


Series and Parallel connections
For optimized capacity and voltage ratings

Rear

Interlock
HW control of output voltage

Interface Panel & BMS Controller

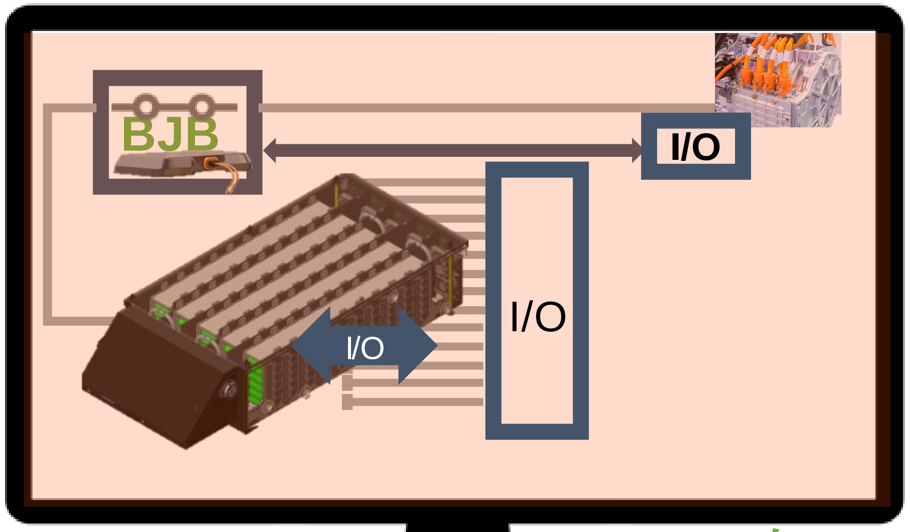


Battery Management Unit

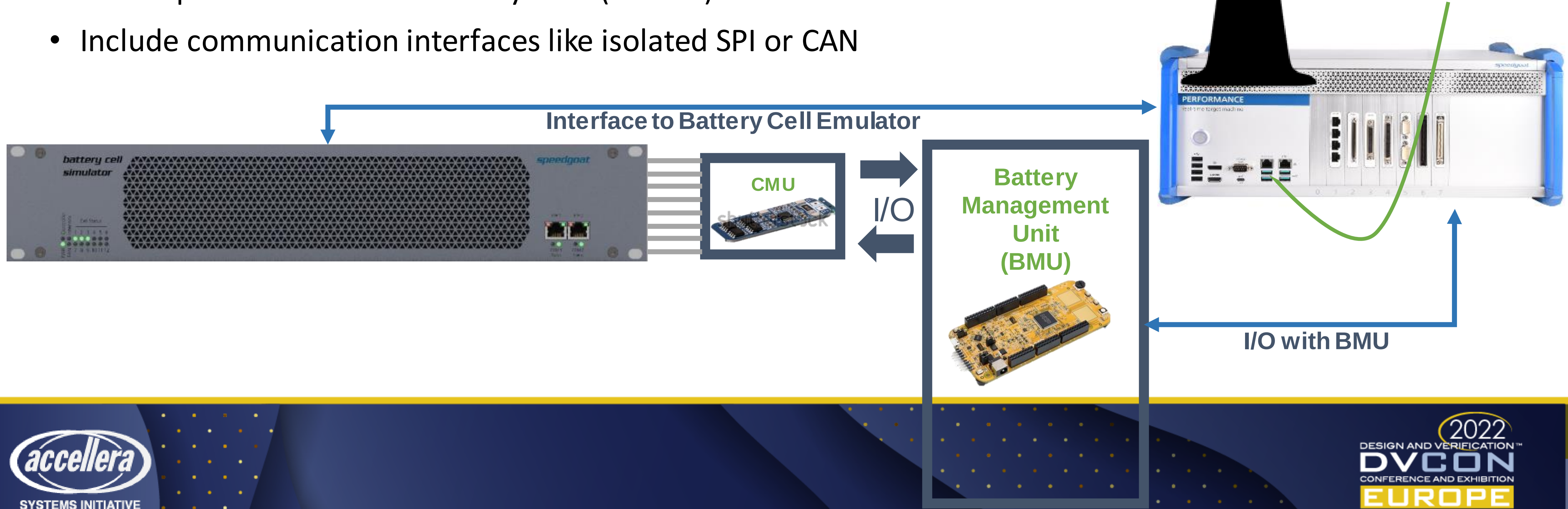
Cell Measurement Unit

Interface Cable

HIL Testing for BMU and CMU

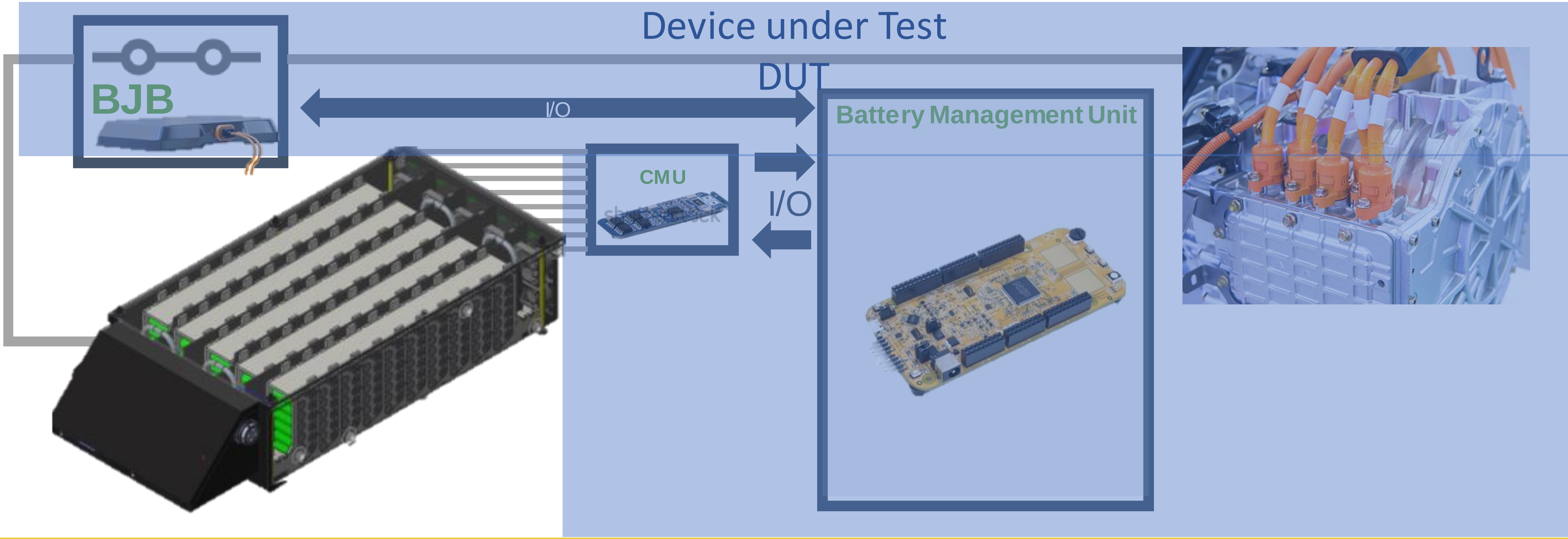


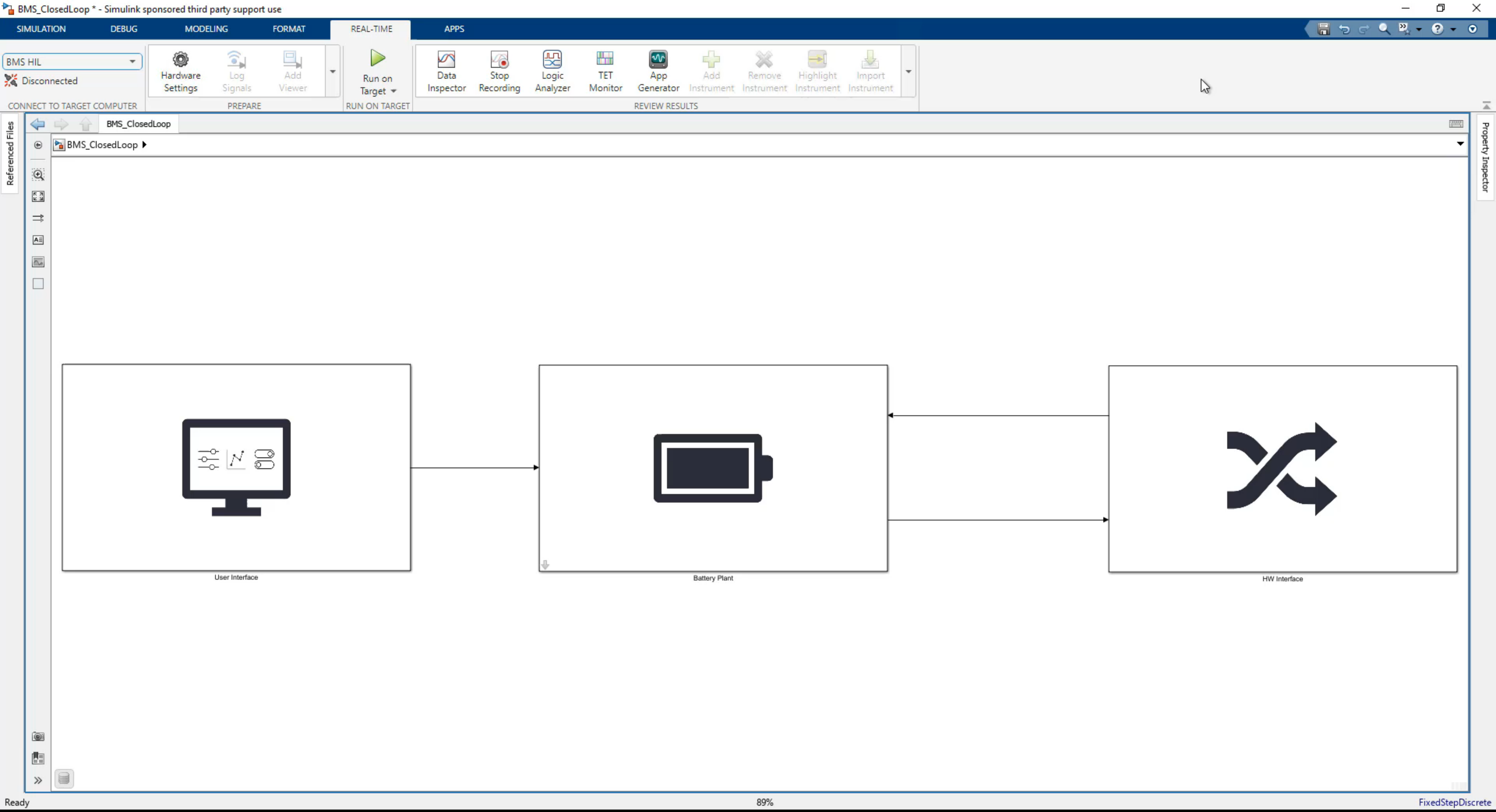
- Test control and electrical interfaces
- Each cell emulated: up to 6V and 5A
- Emulate the electrical behaviour of battery cells
- Stack up to 312 of virtual battery cells (1600 V)
- Include communication interfaces like isolated SPI or CAN

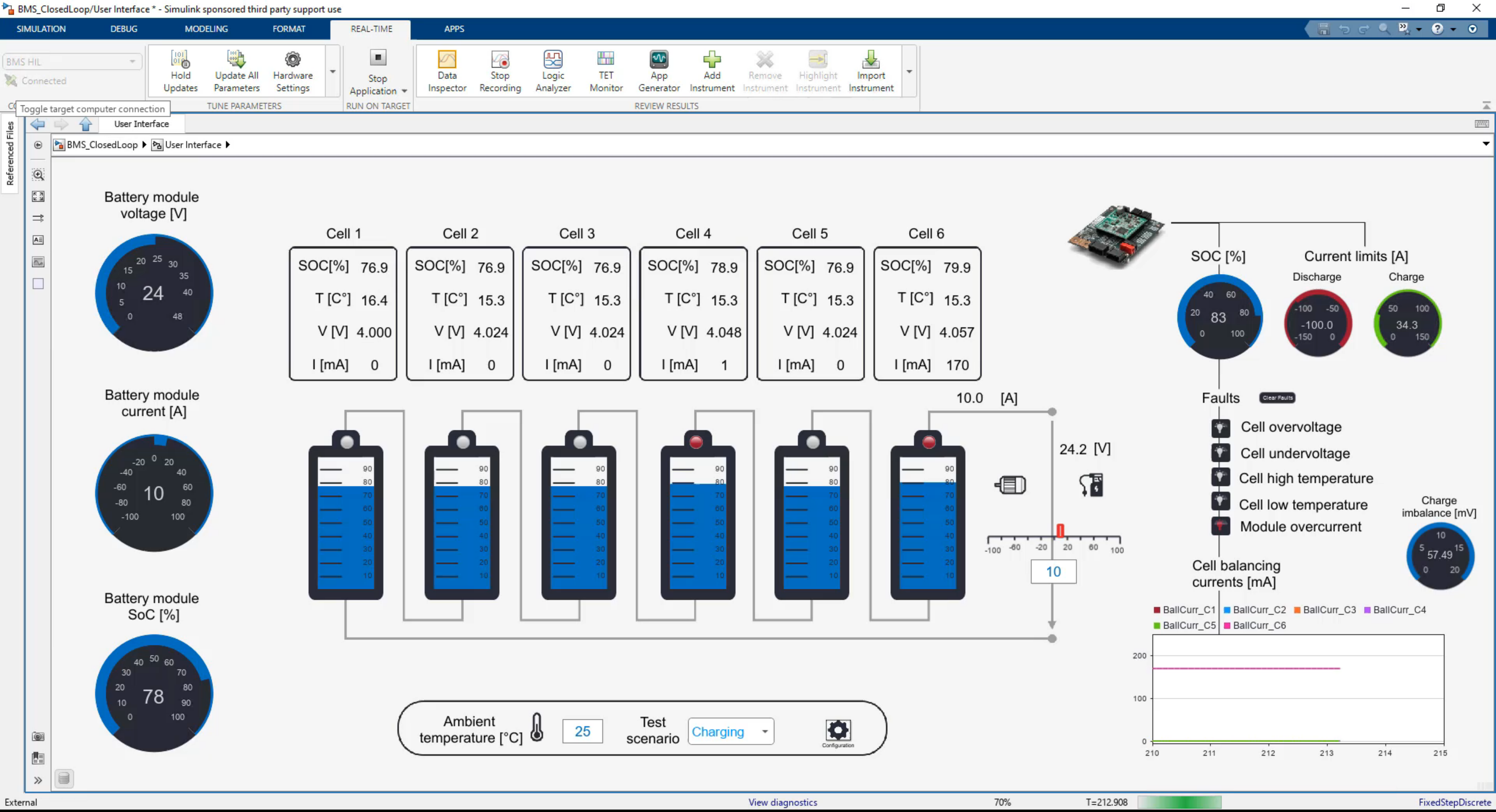


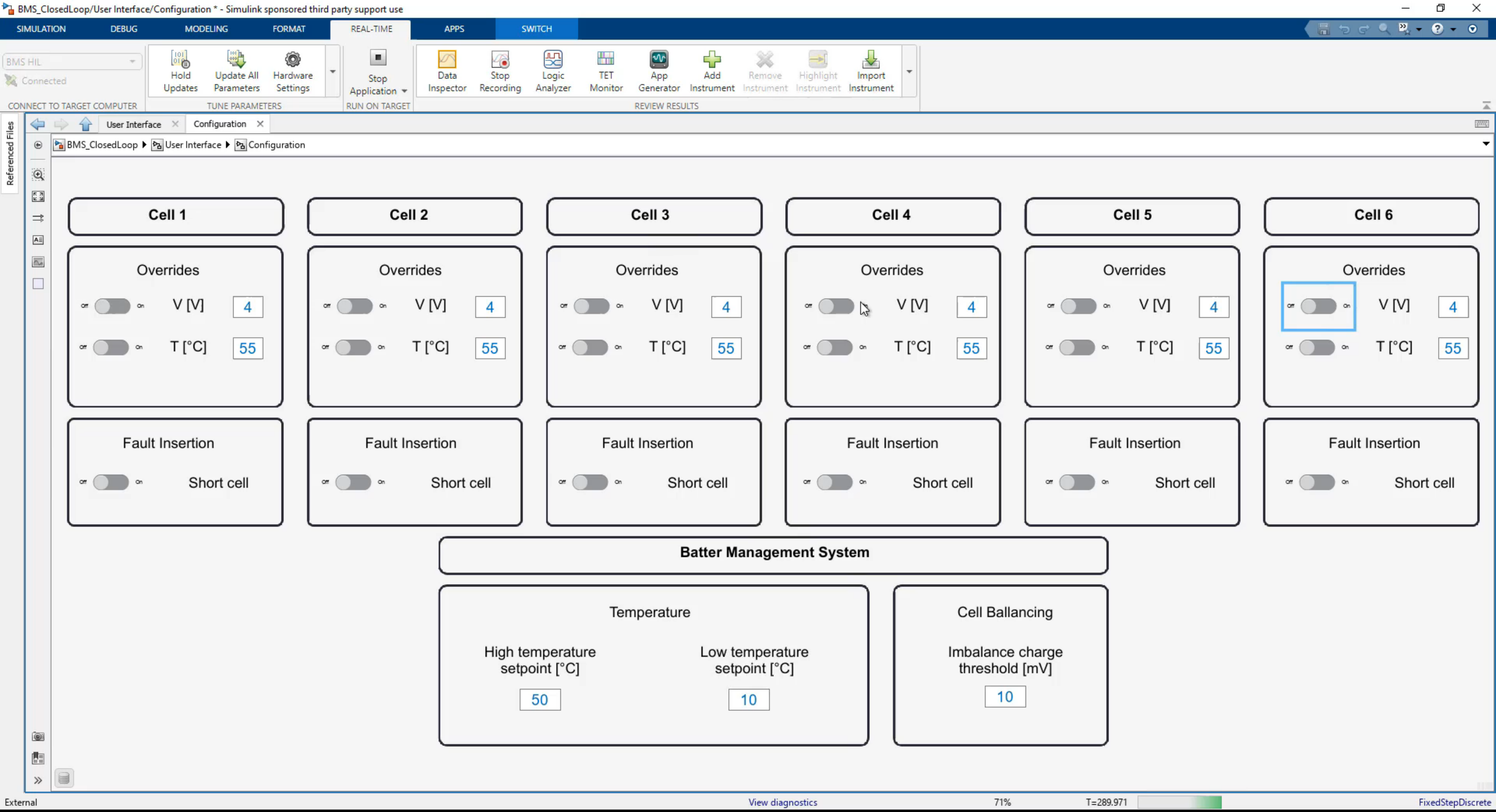
HIL Testing of full BMS and load

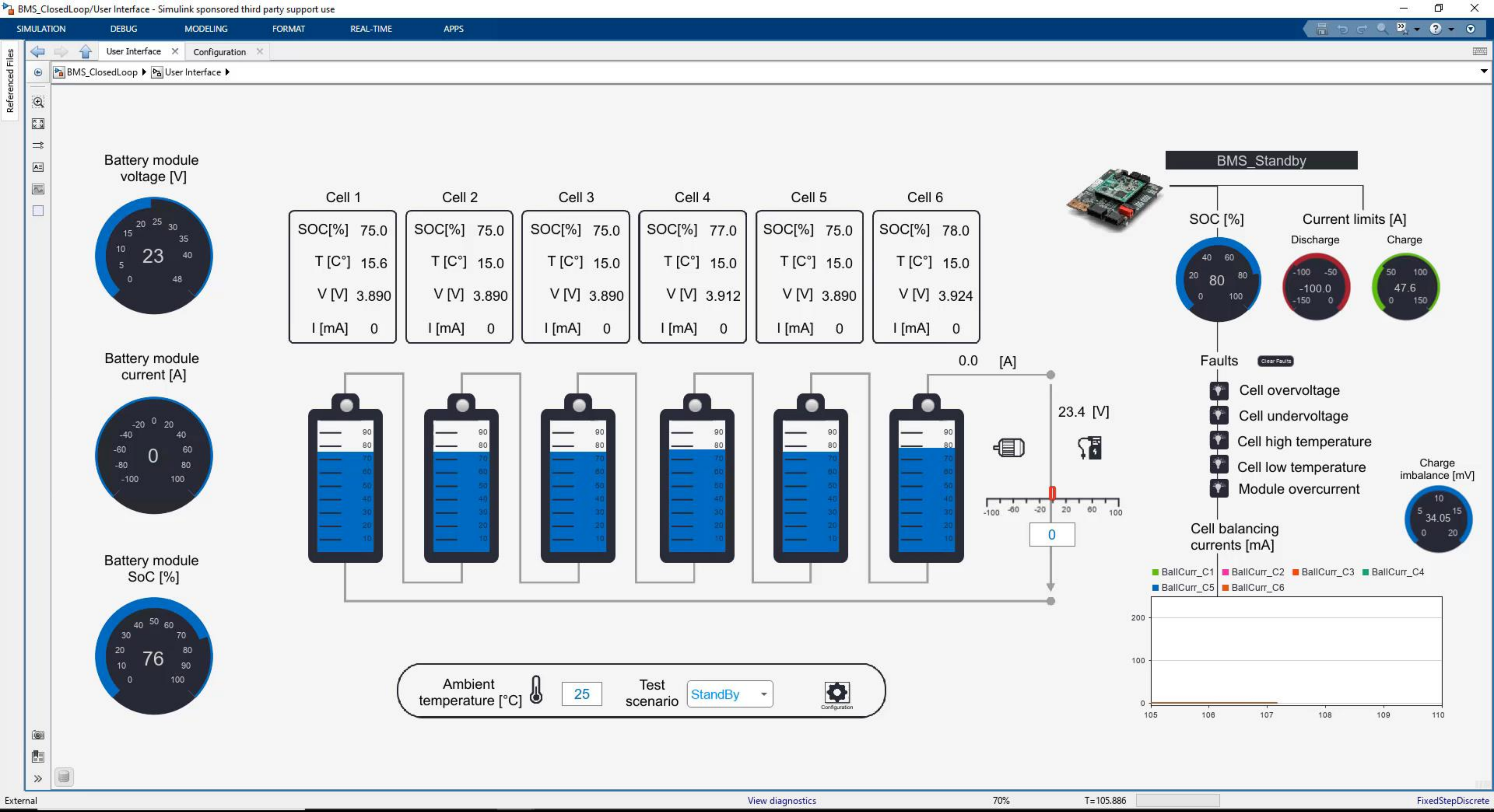
Device under Test can also include the real load (e.g. powertrain or EV charger). The interfaces include electrical power




BMS_ClosedLoop * - Simulink sponsored third party support use
SIMULATION
DEBUG
MODELING
FORMAT
REAL-TIME
APPS
BMS HIL
Disconnected
CONNECT TO TARGET COMPUTER
Hardware Settings
Log Signals
Add Viewer
PREPARE
Run on Target
RUN ON TARGET
Data Inspector
Stop Recording
Logic Analyzer
TET Monitor
App Generator
Add Instrument
Remove Instrument
Highlight Instrument
Import Instrument
REVIEW RESULTS
Referenced Files
BMS_ClosedLoop
BMS_ClosedLoop
Property Inspector
User Interface
Battery Plant
HW Interface
Ready
89%
FixedStepDiscrete


BMS_ClosedLoop/User Interface * - Simulink sponsored third party support use
SIMULATION
DEBUG
MODELING
FORMAT
REAL-TIME
APPS
BMS HIL
Connected
Hold Updates
Update All Parameters
Hardware Settings
TUNE PARAMETERS
Stop Application
RUN ON TARGET
Data Inspector
Stop Recording
Logic Analyzer
TET Monitor
App Generator
Add Instrument
Remove Instrument
Highlight Instrument
Import Instrument
REVIEW RESULTS
Toggle target computer connection
User Interface
BMS_ClosedLoop
User Interface
Referenced Files
Battery module voltage [V]
24
Battery module current [A]
10
Battery module SoC [%]
78
Cell 1
SOC[%] 76.9
T [C°] 16.4
V [V] 4.000
I [mA] 0
Cell 2
SOC[%] 76.9
T [C°] 15.3
V [V] 4.024
I [mA] 0
Cell 3
SOC[%] 76.9
T [C°] 15.3
V [V] 4.024
I [mA] 0
Cell 4
SOC[%] 78.9
T [C°] 15.3
V [V] 4.048
I [mA] 1
Cell 5
SOC[%] 76.9
T [C°] 15.3
V [V] 4.024
I [mA] 0
Cell 6
SOC[%] 79.9
T [C°] 15.3
V [V] 4.057
I [mA] 170
10.0 [A]
24.2 [V]
10
SOC [%]
83
Current limits [A]
Discharge
-100.0
Charge
34.3
Faults
Clear Faults
Cell overvoltage
Cell undervoltage
Cell high temperature
Cell low temperature
Module overcurrent
Charge imbalance [mV]
57.49
Cell balancing currents [mA]
BalCurr_C1
BalCurr_C2
BalCurr_C3
BalCurr_C4
BalCurr_C5
BalCurr_C6
Ambient temperature [°C]
25
Test scenario
Charging
Configuration
External
View diagnostics
70%
T=212.908
FixedStepDiscrete

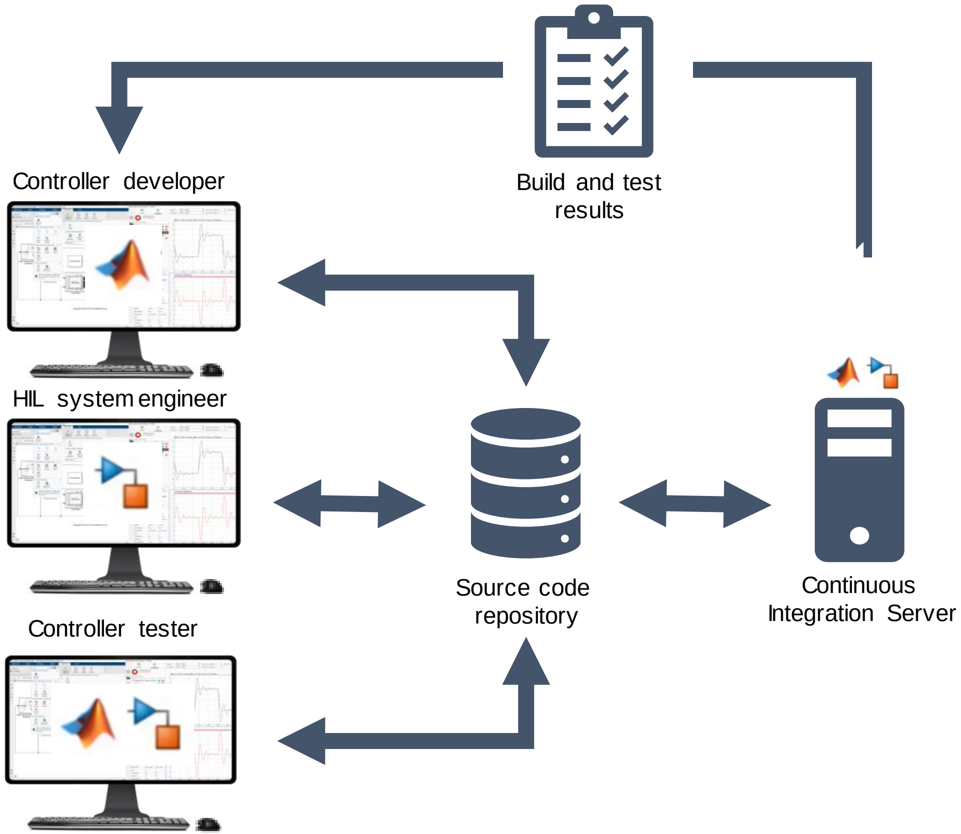

BMS_ClosedLoop/User Interface/Configuration * - Simulink sponsored third party support use
SIMULATION
DEBUG
MODELING
FORMAT
REAL-TIME
APPS
SWITCH
BMS HIL
Connected
Hold Updates
Update All Parameters
Hardware Settings
Stop Application
Data Inspector
Stop Recording
Logic Analyzer
TET Monitor
App Generator
Add Instrument
Remove Instrument
Highlight Instrument
Import Instrument
CONNECT TO TARGET COMPUTER
TUNE PARAMETERS
RUN ON TARGET
REVIEW RESULTS
User Interface
Configuration
BMS_ClosedLoop
User Interface
Configuration
Referenced Files
Cell 1
Cell 2
Cell 3
Cell 4
Cell 5
Cell 6
Overrides
V [V]
4
T [°C]
55
Fault Insertion
Short cell
Batter Management System
Temperature
High temperature setpoint [°C]
50
Low temperature setpoint [°C]
10
Cell Ballancing
Imbalance charge threshold [mV]
10
External
View diagnostics
71%
T=289.971
FixedStepDiscrete


BMS_ClosedLoop/User Interface - Simulink sponsored third party support use
SIMULATION
DEBUG
MODELING
FORMAT
REAL-TIME
APPS
User Interface
Configuration
BMS_ClosedLoop
User Interface
Referenced Files
Battery module voltage [V]
23
Battery module current [A]
0
Battery module SoC [%]
76
Cell 1
SOC[%] 75.0
T [C°] 15.6
V [V] 3.890
I [mA] 0
Cell 2
SOC[%] 75.0
T [C°] 15.0
V [V] 3.890
I [mA] 0
Cell 3
SOC[%] 75.0
T [C°] 15.0
V [V] 3.890
I [mA] 0
Cell 4
SOC[%] 77.0
T [C°] 15.0
V [V] 3.912
I [mA] 0
Cell 5
SOC[%] 75.0
T [C°] 15.0
V [V] 3.890
I [mA] 0
Cell 6
SOC[%] 78.0
T [C°] 15.0
V [V] 3.924
I [mA] 0
0.0 [A]
23.4 [V]
0
Ambient temperature [°C]
25
Test scenario
StandBy
Configuration
BMS_Standby
SOC [%]
80
Current limits [A]
Discharge
-100.0
Charge
47.6
Faults
Clear Faults
Cell overvoltage
Cell undervoltage
Cell high temperature
Cell low temperature
Module overcurrent
Charge imbalance [mV]
34.05
Cell balancing currents [mA]
BallCurr_C1
BallCurr_C2
BallCurr_C3
BallCurr_C4
BallCurr_C5
BallCurr_C6
External
View diagnostics
70%
T=105.886
FixedStepDiscrete


BMS_ClosedLoop/User Interface * - Simulink sponsored third party support use
SIMULATION
DEBUG
MODELING
FORMAT
REAL-TIME
APPS
COMBO BOX
User Interface
Configuration
BMS_ClosedLoop
User Interface
Referenced Files
Battery module voltage [V]
23
Battery module current [A]
0
Battery module SoC [%]
73
Cell 1
SOC[%] 72.1
T [C°] 21.2
V [V] 3.860
I [mA] 0
Cell 2
SOC[%] 72.1
T [C°] 19.7
V [V] 3.860
I [mA] 0
Cell 3
SOC[%] 72.1
T [C°] 19.4
V [V] 3.860
I [mA] 0
Cell 4
SOC[%] 74.0
T [C°] 19.3
V [V] 3.880
I [mA] 161
Cell 5
SOC[%] 72.1
T [C°] 19.3
V [V] 3.860
I [mA] 0
Cell 6
SOC[%] 75.0
T [C°] 19.3
V [V] 3.892
I [mA] 162
0.0 [A]
23.2 [V]
0
BMS_Standby
SOC [%]
77
Current limits [A]
Discharge
-100.0
Charge
50.0
Faults
Clear Faults
Cell overvoltage
Cell undervoltage
Cell high temperature
Cell low temperature
Module overcurrent
Charge imbalance [mV]
32.05
Cell balancing currents [mA]
BallCurr_C1
BallCurr_C2
BallCurr_C3
BallCurr_C4
BallCurr_C5
BallCurr_C6
Ambient temperature [°C]
25
Test scenario
StandBy
Configuration
External
View diagnostics
70%
T=676.802
FixedStepDiscrete

Continuous Integration with Hardware

Workflow



Benefits

Repeatability – repeatable, automated process

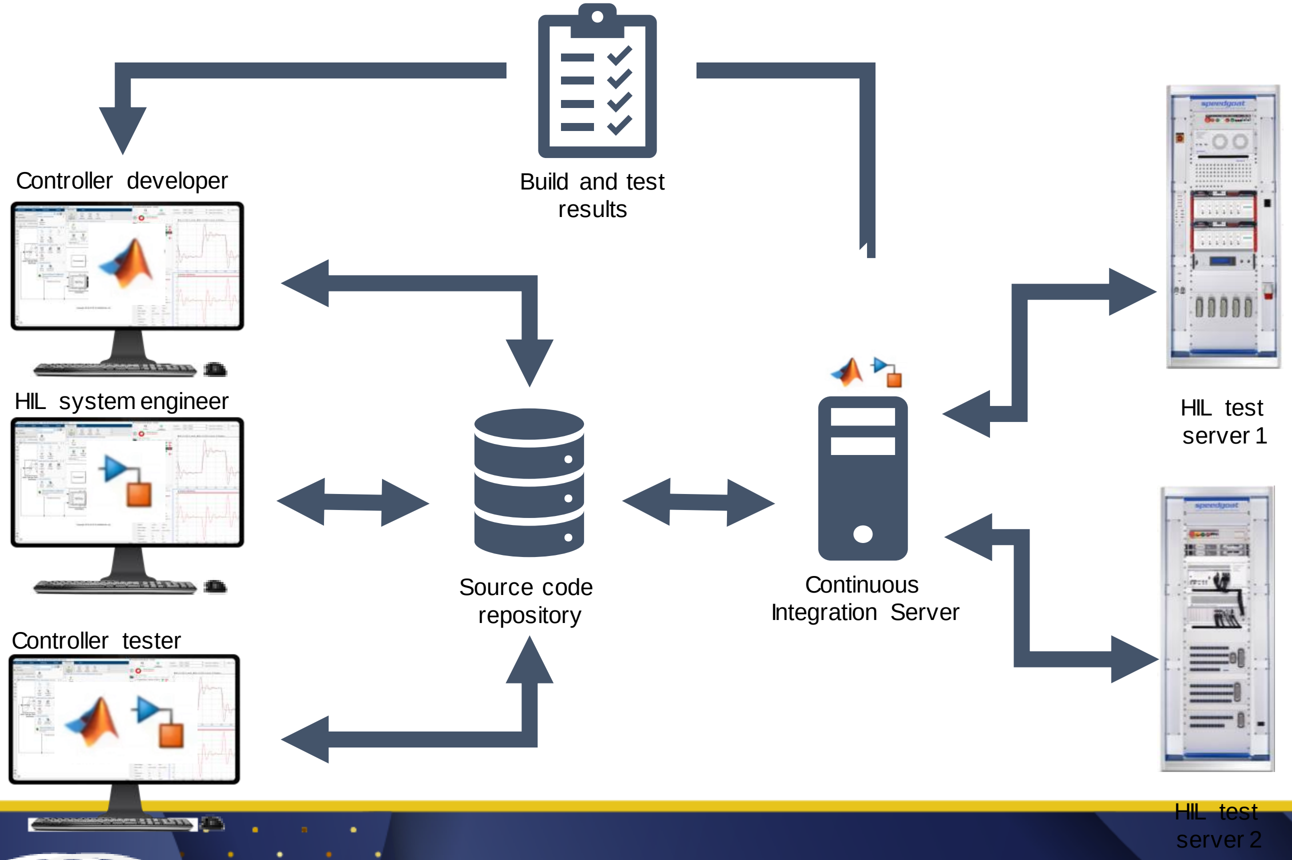
Quality – always test against latest changes

Speed – test early, test often

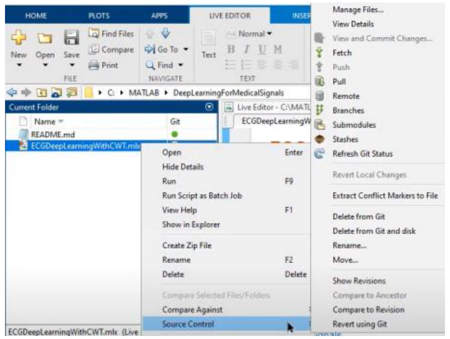
Collaboration – identify integration issues quickly

Audit-ready – trace issues to the source

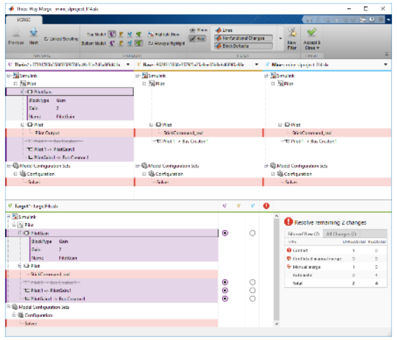
Continuous Integration with Hardware



Source control in projects



Compare changes



Check model quality and standard compliance

Support for main CI platforms

Jenkins GitLab GitHub Bamboo Travis CI Azure DevOps

Quickly visualize test reports and results

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DECEMBER 6 - 7, 2022

Questions

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