



Agentic AI in Action: Enhancing Debug, Diagnostics, and Decision-Making





Anika Sunda Product Marketing Director Cadence

Anika Sunda is a product marketing director in the Cadence System Verification Group. She has more than 16 years of semiconductor industry experience spanning product management, research development, and verification from prior roles at Synopsys and Agilent Technologies.

Sunda is a gold medalist and holds a master's from IIT Bangalore, India.



Amod Khandekar

Sr Principal Customer Engagement Engineer Cadence

Amod has been working with Cadence for past 20 years. He has worked as Pre Sales and Customer Support Engineer supporting all the verification related tools. Currently he is part of Product Engineering team with Focus on Verisium Apps.



Sundararajan Ananthakrishnan

Application Engineer Architect Cadence

Sundar has been at Cadence for 15 years, with an overall Experience of 25+ years in the field of SoC & IP Verification. Sundar leads the Cadence AVS field team for India region and drives the Advanced ML/AI and Verification Solutions in the region.



**Agentic AI in Action: Enhancing Debug,
Diagnostics, and Decision-Making**

DVCon India

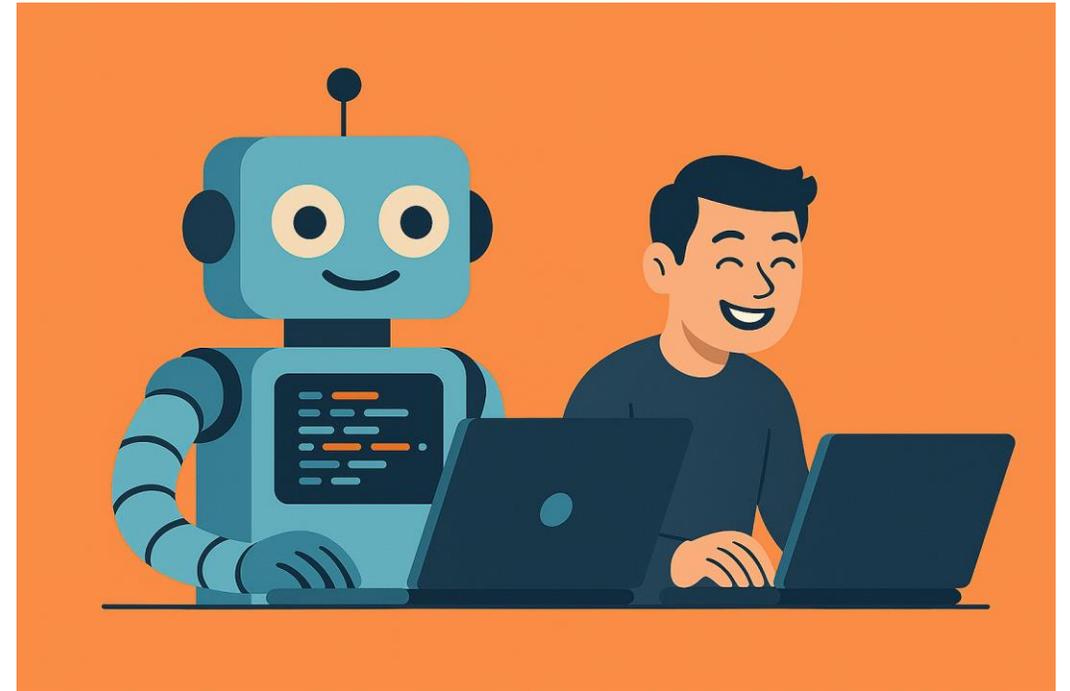
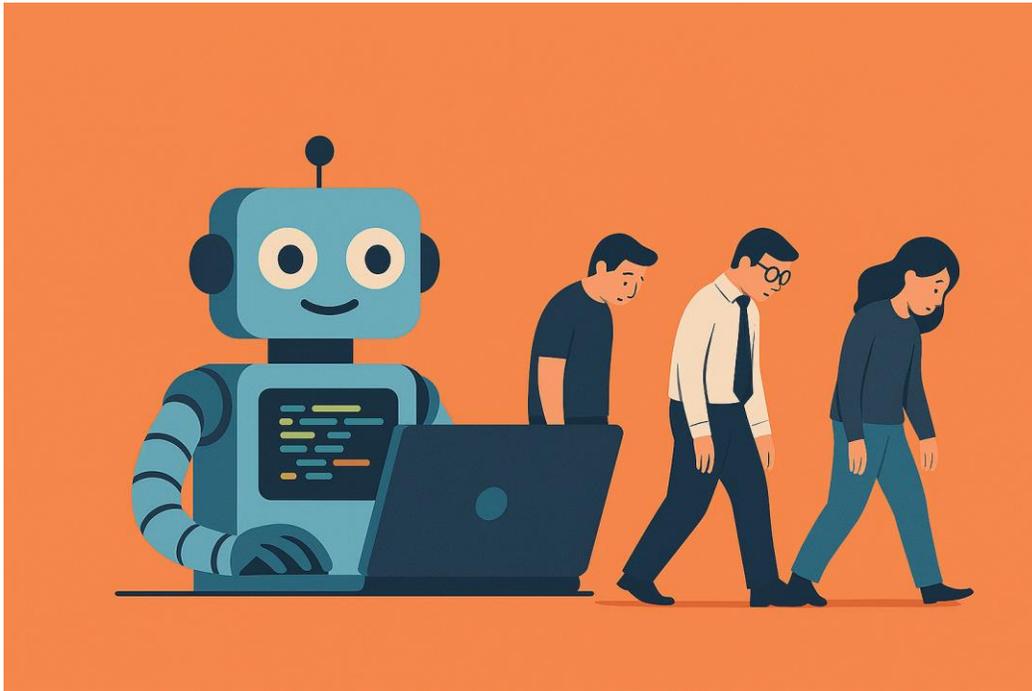
Anika Sunda, Amod Khandekar, Sundararajan Ananthakrishnan

Agenda

- AI in EDA
- AI Regression Optimization
- AI Workload Optimization
- AI Debug Optimization
- AI Resource Optimization
- Agentic AI Flows for Verification
- Q&A

Engineers won't lose their jobs to AI.

They will lose their jobs to another engineer using AI. – Jensen Huang



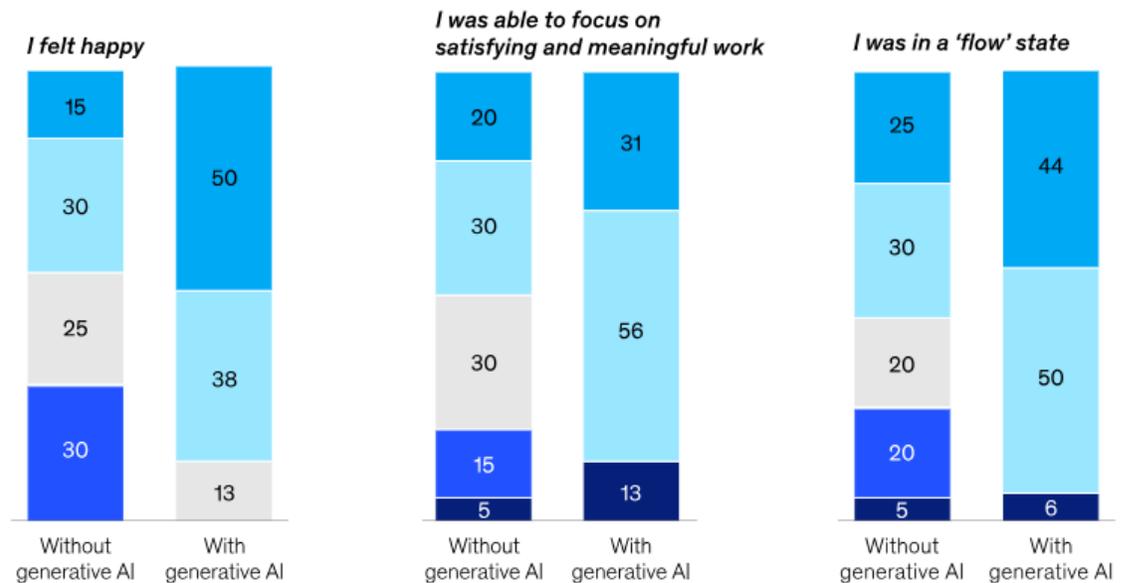
AI Coding – Making the world a better place?

- Automate tedious tasks
 - Boiler plate and syntax
 - Unit tests and edge cases
 - Debugging
 - Documentation
- Focus engineering time on creative problem-solving
- Improve morale and engagement – “Happy bees make sweeter honey.”

Generative AI tools have potential to improve the developer experience.

Agreement with statement,
% of respondents

Strongly disagree Somewhat disagree Neither agree or disagree Somewhat agree Strongly agree



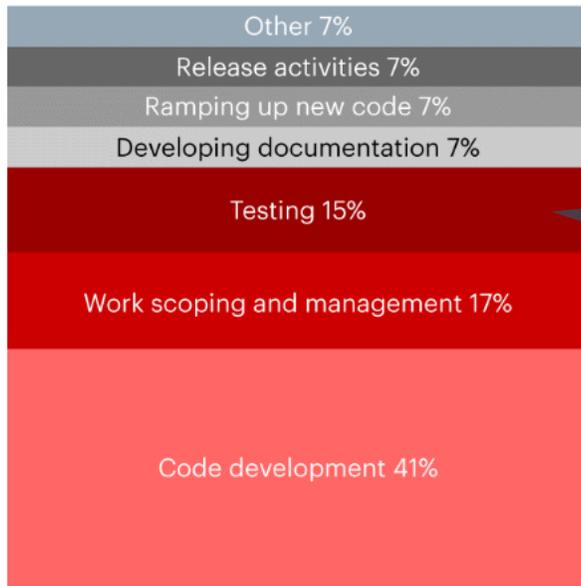
Note: Figures may not sum to 100%, because of rounding.

McKinsey & Company

AI Impact for Software Coding

Efficiency gains real, but uneven – challenge to monetize

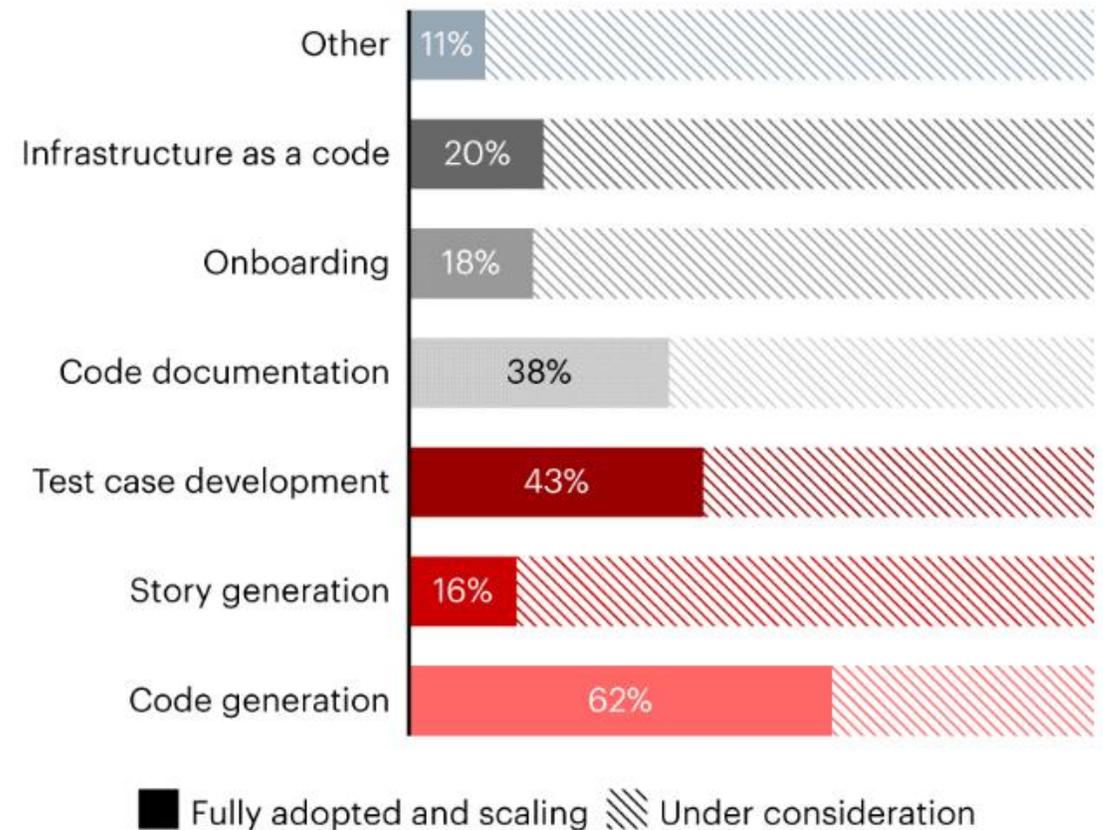
- GenAI improving coding productivity 10-15%
- Potential for 30% total improvement when expanded to other tasks
- Challenge to monetize – need to focus saved engineering time on high-impact work



Only 15% for testing?

Software development lifecycle activity

Q: Select the status of generative AI adoption for each use case



Source: Bain Software Developers Survey, 2024

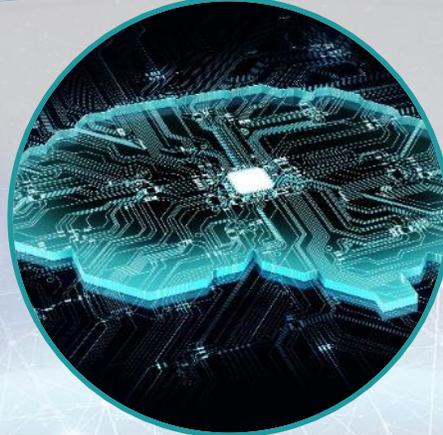
Computer Chips Are Powering Everything



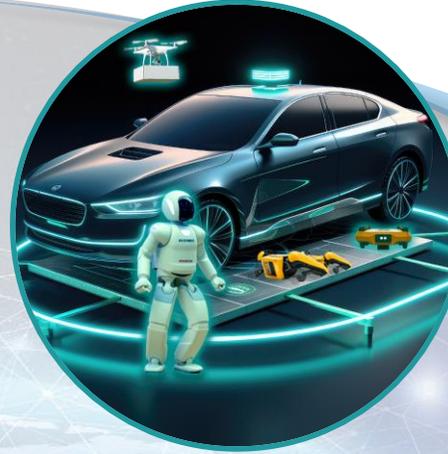
**Limitless
Connectivity**



**Cloud and
Big Data**



Agentic AI

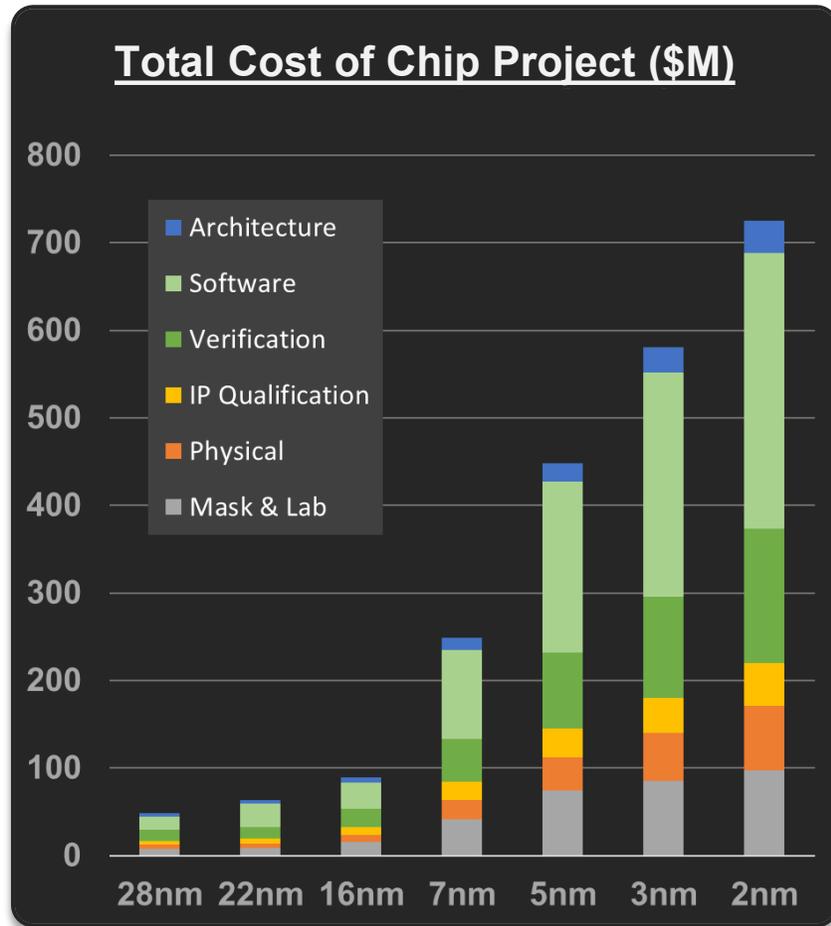


**Autonomy
Cars - Drones - Robots**



**Augmented and
Virtual Reality**

Verification is Still the Infinite Problem



IBS, Global Semiconductor Industry Service Report

- Verification costs largest in IC dev
- Advanced node and 3D-IC means more gates, more states, more potential bugs
- Dev schedules continue to tighten
- Engineering resource gap is growing

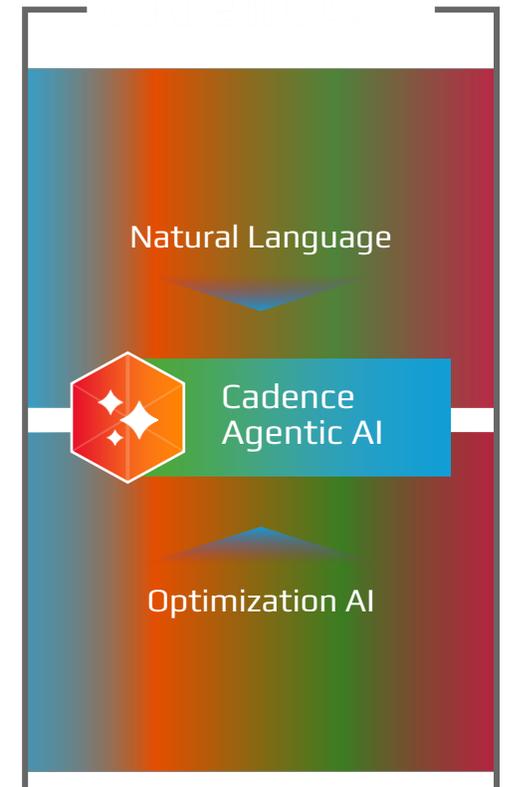
Agentic AI: Optimize Engines & Optimize Engineers

EDA's 40-Year History

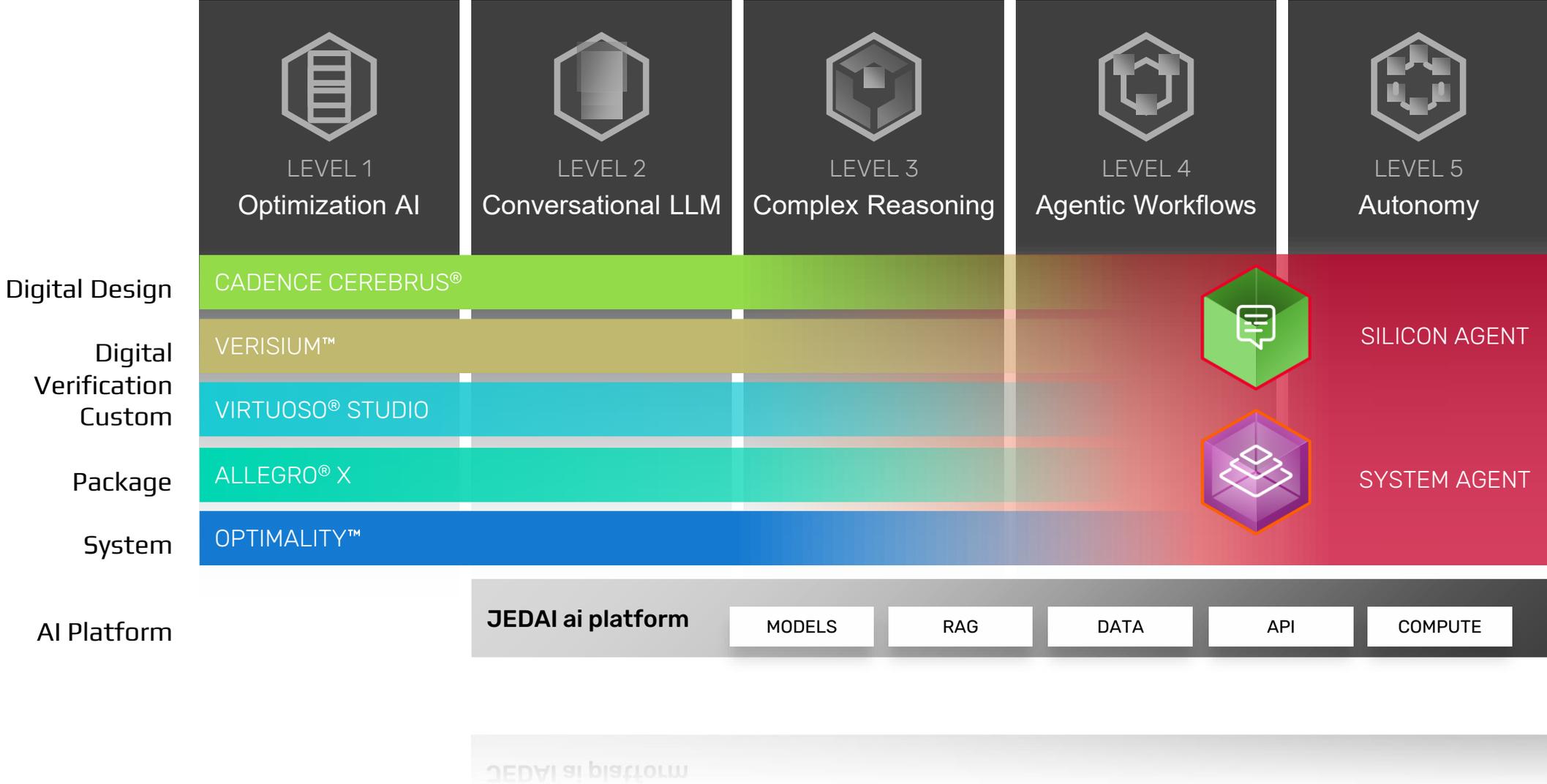


Excellence in Simulation and Optimization

NUMERICAL SOLVERS	SMT SOLVERS	GRAPH THEORY AND TOPOLOGY
BINARY DECISION DIAGRAMS	BOUNDED MODEL CHECKER	DISTRIBUTED PROCESSING
SAT SOLVERS	ADAPTIVE MESHING	NON-LINEAR SOLVERS
SYMBOLIC MODEL CHECKERS	MATRIX SOLVERS	COMPUTATIONAL GEOMETRY



The Journey to Autonomous Design

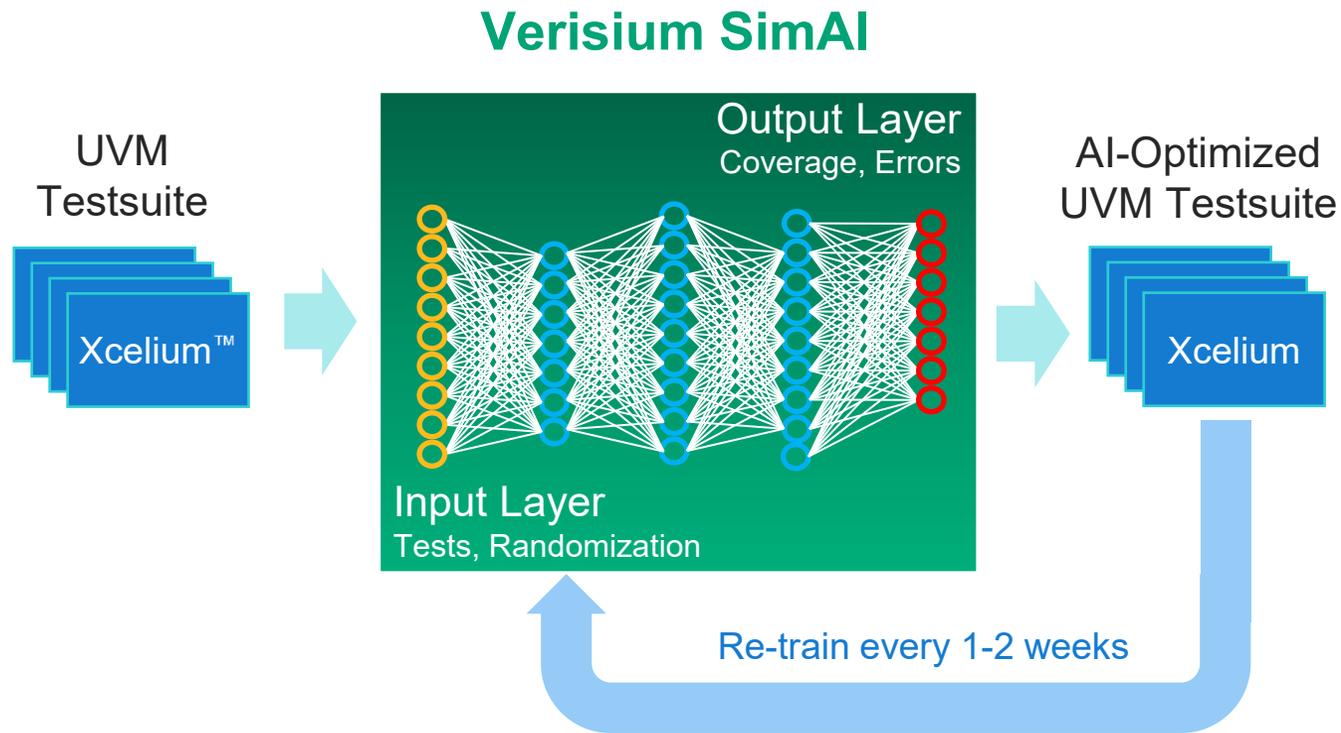




Verisium SimAI

AI-Driven Regression Optimization

AI-Driven Logic Simulation with Verisium SimAI



Design Type	Speed Up
Modem IP	20x
Mobile SoC	7x
AI IP	8x
AI IP	3x
Memory IP	5x
Base Station	18x
NOC IP	5x
Automotive SoC	5x
CPU IP	3x
Network IP	4x
CPU IP	9x

New! SimAI for Coverage

21K runs
this cover point has difficult bins

4 bins not hit even with multiple iterations

bin	hits
covpoint/bin[8]	13830
covpoint/bin[9]	75
covpoint/bin[10]	39
covpoint/bin[11]	14
covpoint/bin[12]	4
covpoint/bin[13]	0
covpoint/bin[14]	0
covpoint/bin[15]	0
covpoint/bin[16]	0

1st SimAI regression
14K runs

bins still not hit but other bins in CP hit at a much higher rate

bin	hits
covpoint/bin[8]	19126
covpoint/bin[9]	53
covpoint/bin[10]	22
covpoint/bin[11]	12
covpoint/bin[12]	10
covpoint/bin[13]	0
covpoint/bin[14]	0
covpoint/bin[15]	0
covpoint/bin[16]	0

2nd SimAI regression
14K runs

With iterative learning all bins reliably hit

bin	hits
covpoint/bin[8]	37103
covpoint/bin[9]	124
covpoint/bin[10]	50
covpoint/bin[11]	28
covpoint/bin[12]	18
covpoint/bin[13]	8
covpoint/bin[14]	4
covpoint/bin[15]	4
covpoint/bin[16]	2

bin	hits
covpoint/bin[8]	13830
covpoint/bin[9]	75
covpoint/bin[10]	39
covpoint/bin[11]	14
covpoint/bin[12]	4
covpoint/bin[13]	0
covpoint/bin[14]	0
covpoint/bin[15]	0
covpoint/bin[16]	0



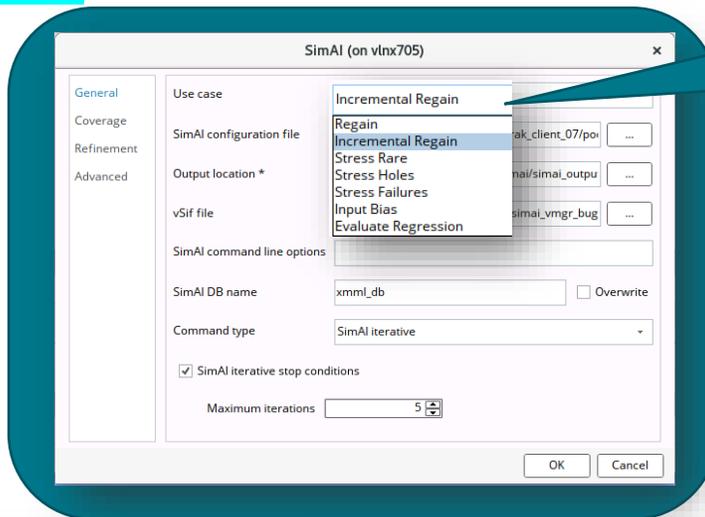
bin	hits
covpoint/bin[8]	19126
covpoint/bin[9]	53
covpoint/bin[10]	22
covpoint/bin[11]	12
covpoint/bin[12]	10
covpoint/bin[13]	0
covpoint/bin[14]	0
covpoint/bin[15]	0
covpoint/bin[16]	0



bin	hits
covpoint/bin[8]	37103
covpoint/bin[9]	124
covpoint/bin[10]	50
covpoint/bin[11]	28
covpoint/bin[12]	18
covpoint/bin[13]	8
covpoint/bin[14]	4
covpoint/bin[15]	4
covpoint/bin[16]	2

SimAI in vManager – Better Together

Launch SimAI



Review SimAI HTML Reports

Review SimAI Summary Metrics

Review SimAI Text Reports

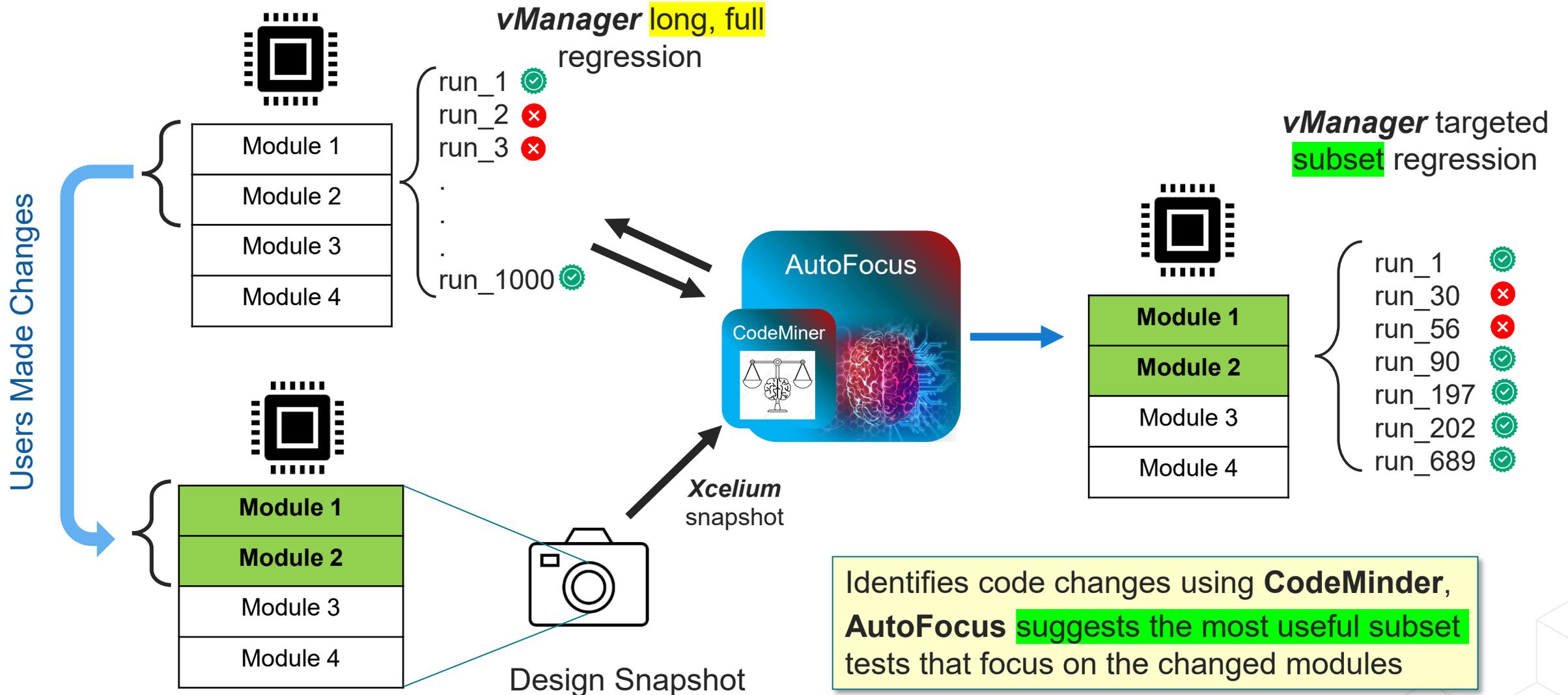
ID	Session Status	Description	Name	Total Runs	#Passed	#Failed	#Waiting	#Running	#Other	Duration (sec.)	Start Time	End Time	Owner
65644	completed		rak_simple_example_regain.glp.25.08.12.08.49...	1	1	0	0	0	0	51	12/08/25 08:49	12/08/25 08:50	glp
65642	completed	n/a	SimAI_incremental_regain_iter2_actions_accumul...	2	2	0	0	0	0	32	12/08/25 08:48	12/08/25 08:49	glp
65638	completed	n/a	rak_simple_example_regain.glp.25.08.12.08.47...	6	6	0	0	0	0	82	12/08/25 08:47	12/08/25 08:48	glp
65634	completed	n/a	SimAI_incremental_regain_iter1_actions_accumul...	6	6	0	0	0	0	58	12/08/25 08:46	12/08/25 08:47	glp
65630	completed	n/a	rak_simple_example_regain.glp.25.08.12.08.44...	50	50	0	0	0	0	73	12/08/25 08:44	12/08/25 08:45	glp
65626	completed	n/a	SimAI_incremental_regain_iter0_actions_accumul...	20	20	0	0	0	0	165	12/08/25 08:42	12/08/25 08:45	glp
65622	completed	SimAI_iterative.in...	SimAI_iterative.incremental_regain.glp.25.08.12...	400	400	0	0	0	0	n/a	12/08/25 08:41	12/08/25 08:41	glp



Verisium AutoFocus

AI-Driven Workload Optimization

AutoFocus: AI-Driven Focused Regression Generation



Auto Focus – Impact - Customer Success Stories

- Results from experiments with existing customers

Customer	Original Regression Runtime	AutoFocus-generated Regression Runtime	Runtime Improvement
Customer1	3 days	15 hours	> 4x
Customer2	47 hours	7 hours	> 6x
Customer3	166 minutes	80 minutes	~ 2x

Customer	Original Regression #runs	AutoFocus-generated Regression #runs	#runs Improvement
Customer4	W/ RTL bug 8893 runs (1756 fail) W/ RTL fix 9345 runs (2 fail)	<ul style="list-style-type: none">40 runs100% coverage regain on focus area	~230x

- Customer Profile:
 - Anyone affected by long regression runtime
 - Anyone looking to run smarter 'nightly' or 'smoke' type regressions



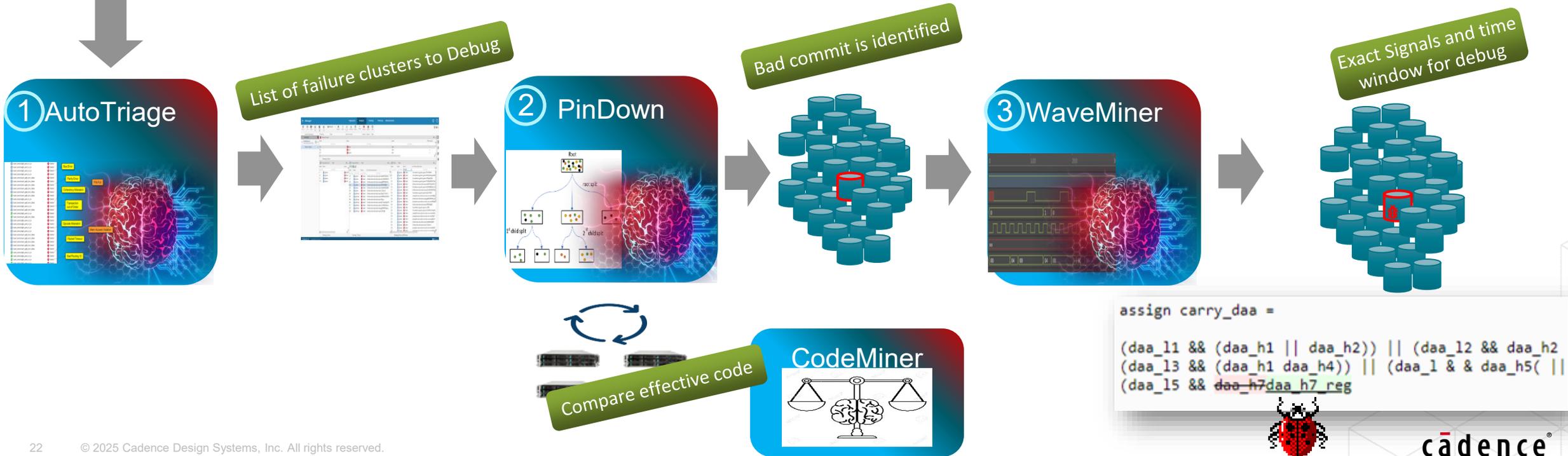
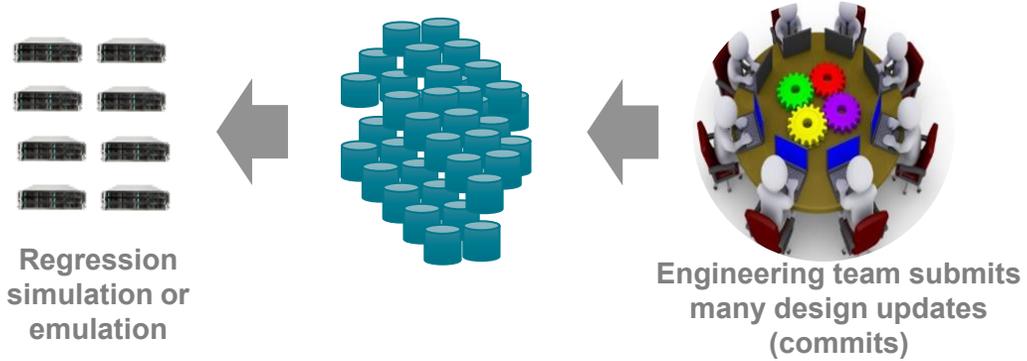


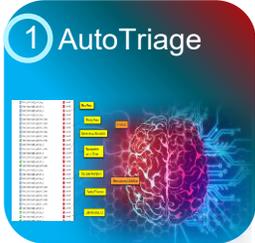
Verisium Debug Apps (AutoTriage, PinDown, WaveMiner, CodeMiner)

AI-Driven **Debug** Optimization

Verisium Apps – Used Standalone or in a

Given **two design versions** and **regression failure**,
predict/locate with high accuracy the **root-cause** at source code

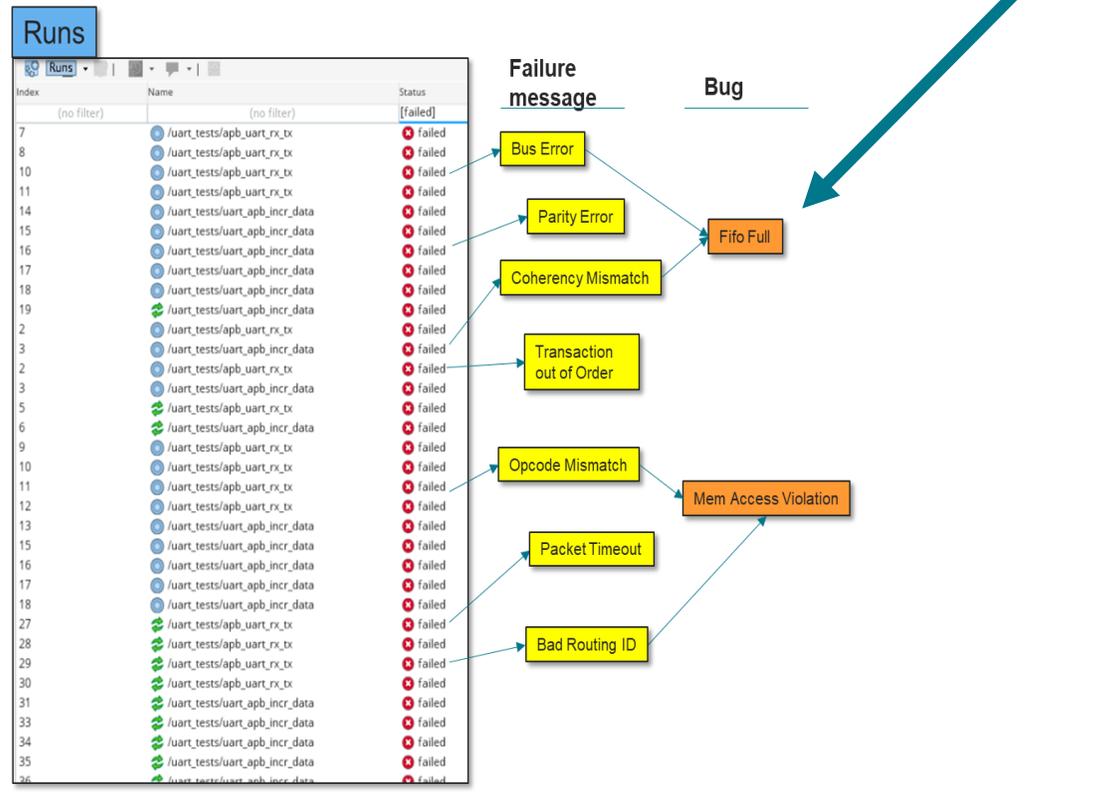




AutoTriage – Automated ML Bucketing of Regression Failures

- Manual failure analysis of regression is very costly and inefficient

- AutoTriage
 - Automate failure classification using Machine Learning
 - Recognize patterns in any run-based attributes
 - Error message, test name, run time, etc.



The screenshot shows the Verisium Manager interface with the following components:

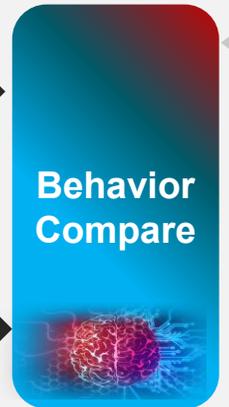
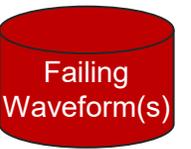
- User create Failure Cluster:** A button in the top navigation bar.
- Proposed Runs:** A table listing runs with columns for Name, First Failure Description, Failure Cluster Proposal Assurance, and Failure Cluster Proposal.
- ML based Recommendations for new Clusters:** A callout box pointing to the 'Propose Clusters' button.
- User Feedback to Recommendations:** A callout box pointing to the 'Associate to cluster' and 'Propose to another cluster' options.
- ML based Recommendations for existing Clusters:** A callout box pointing to the 'Edit each' and 'Attribute change history' options.

Index	Name	First Failure Description	Failure Cluster Proposal Assurance	Failure Cluster Proposal
51	/uart_tests/u...	##### FAIL : APB RECEIVED WRONG DATA 'h27...	50.15%	vManager
80	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
81	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
82	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
83	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
84	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
85	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
86	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
87	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
88	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
89	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
90	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager
91	/uart_tests/u...	Failed to submit DRM job	59.37%	vManager



WaveMiner: Smart Waveform Analysis

WaveMiner : Applies AI engines to analyze waveforms from multiple runs (same test/seed) and determine which signals, at which times, are most likely to represent the root cause of a test failure.



"Interesting" Behavior



Relevant Signals



Failing Tests

Verisium Debug

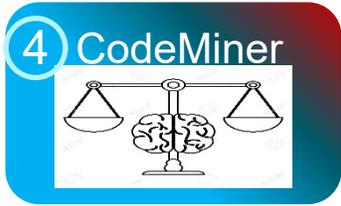
Back annotation to source code

Ranked simulation time point to debug

Navigation on culprit signals

Top ranked signals

Top Ranked Signals	Passing Waveform	Failing Waveform
tb.myFifo.rptr		
770ns	good_wave/da_fifo.shm	bad_wave/da_fifo.shm
790ns	good_wave/da_fifo.shm	bad_wave/da_fifo.shm
110ns	good_wave/da_fifo.shm	bad_wave/da_fifo.shm
tb.myFifo.DATAOUT		
790ns	good_wave/da_fifo.shm	bad_wave/da_fifo.shm
110ns	good_wave/da_fifo.shm	bad_wave/da_fifo.shm



CodeMiner

Identify and rank semantic changes between two RTL/TB versions

- Ignore harmless changes
- Rank “complexity” of genuine logic changes
- SystemVerilog (RTL + TB) and VHDL.

```

module cg (d, clk);
input d, clk;
reg orig;
reg clone;
reg g_latch;
wire w = orig ^ d;
wire gclk = clk & g_latch;

always @(clk or w)
  if (~clk) g_latch <= w;

always @(posedge gclk) clone <= d;

always @(posedge clone) orig <= d;

fd : assert property (
  @(posedge clk) orig == clone
);
Endmodule
  
```



```

module cg (d, clk);
input d, clk;
reg orig, clone, g_latch;

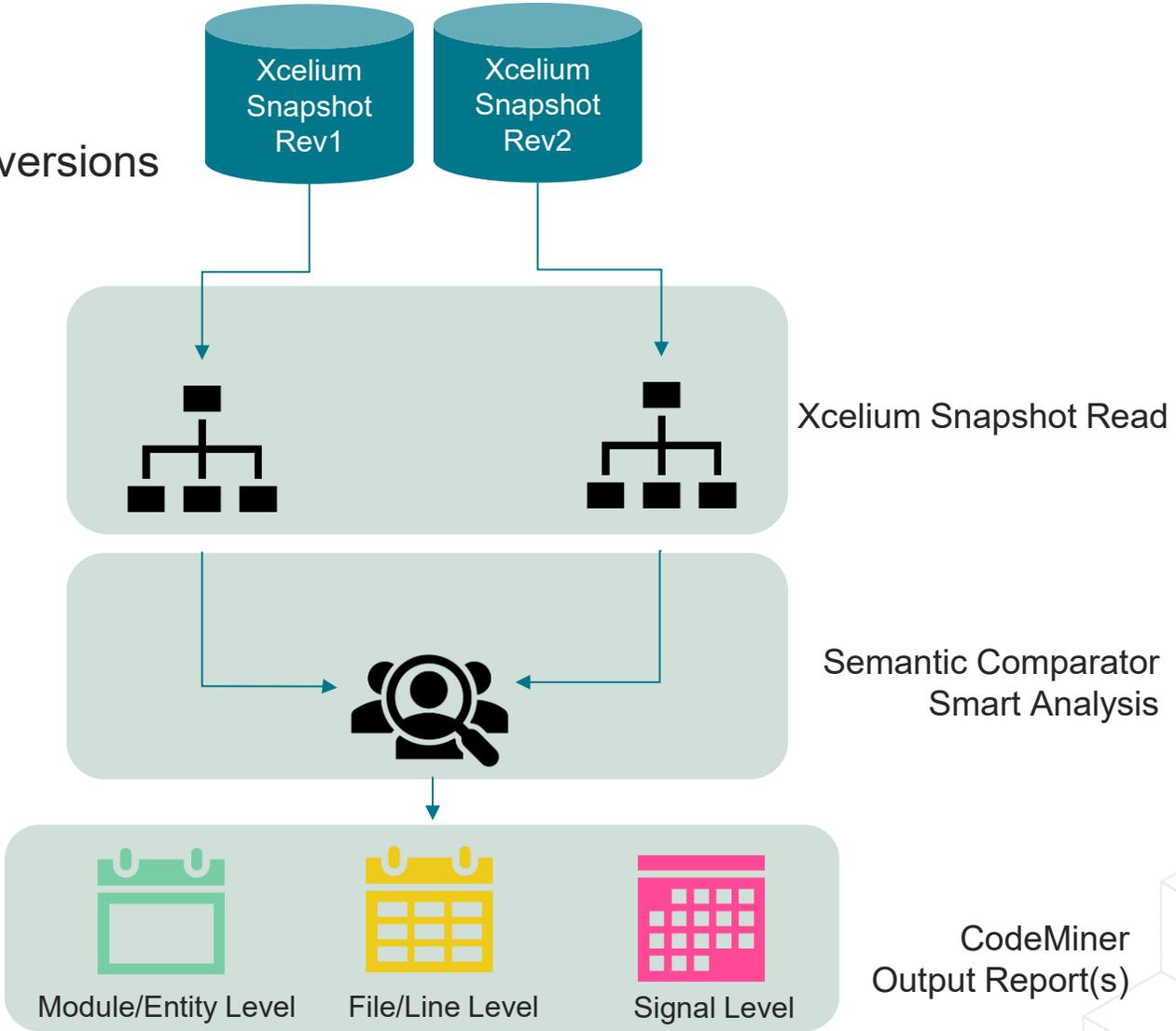
// Comments ...
wire w = orig ^ d;
wire gclk = clk & g_latch;

always @(clk or w)
  if (clk) g_latch <= w;

always @(posedge gclk)
  clone <= d;

always @(posedge clone)
  orig <= d;

fd : assert property (
  @(posedge clk) orig == clone
);
endmodule
  
```



CodeMiner Output in GUI Mode

Verisium Debug GUI in CodeMiner Mode

The screenshot displays the Verisium Debug GUI in CodeMiner Mode. The interface is divided into several sections:

- Entity View Table:** A table listing entities and their diff statistics. The 'Diff Complexity Rank' and 'Diff Complexity %' columns are highlighted with a yellow box and labeled 'Ranks and statistics for quick analysis'.

Entity Name	Diff Lines	Diff Constructs	Diff Complexity Rank	Diff Complexity %
b	1/5 (20.0%)	A:0, M:1, D:0	1	(31.15%)
n	1/7 (14.29%)	A:0, M:1, D:0	2	(17.44%)
topd	3/3 (100.0%)	A:1, M:0, D:0	3	(17.36%)
t1	2/9 (22.22%)	A:0, M:2, D:0	4	(12.27%)
interf	1/7 (14.29%)	A:0, M:1, D:0	5	(10.13%)
topc	1/3 (33.33%)	A:0, M:1, D:0	6	(5.82%)
topa	1/3 (33.33%)	A:0, M:1, D:0	7	(5.82%)
topb	3/3 (100.0%)	A:0, M:0, D:1	-	(17.36%)
- Diff Details Table:** A table showing the location of differences in source files. It is highlighted with a yellow box and labeled 'Click and analyze each of the diffs'.

Mode	Golden File	Start Position	End Position	New File	Start Position	End Position
Filter visible...	Filter visible rows	Filter visible rows	Filter visible rows	Filter visible rows	Filter visible rows	Filter visible rows
	./testg.sv	(42, 12)	(42, 17)	/servers/noiv.../testn.sv	(42, 12)	(42, 17)
	./testg.sv	(43, 6)	(43, 7)	/servers/noiv.../testn.sv	(43, 6)	(43, 7)
- Code Comparison:** Two side-by-side code editors showing the source code for ./testg.sv and ./testn.sv. The differences between the two files are highlighted in yellow. Arrows point from the 'Diff Details' table to these highlighted sections, with a label 'Diffs between the sources is highlighted appropriately for further analysis'.

Ranks and statistics for quick analysis

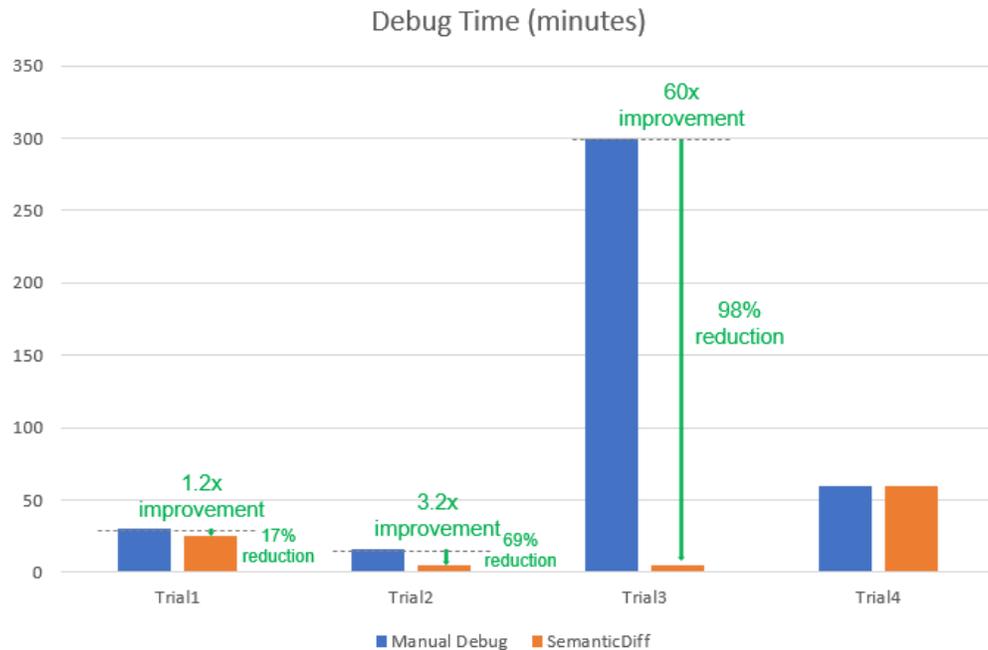
Click and analyze each of the diffs

Diffs between the sources is highlighted appropriately for further analysis

Verisium Apps – Customer Feedback

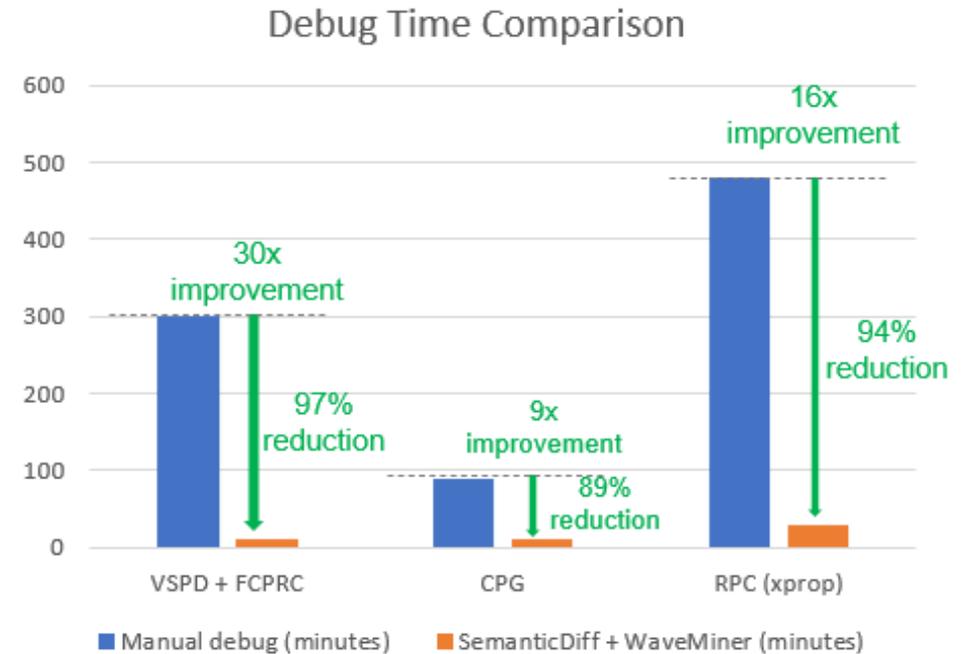
- **CodeMiner**

1.2x, 3.2x, and 60x efficiency improvement
17%, 69%, and 98% reduction in debug time



- **CodeMiner + WaveMiner**

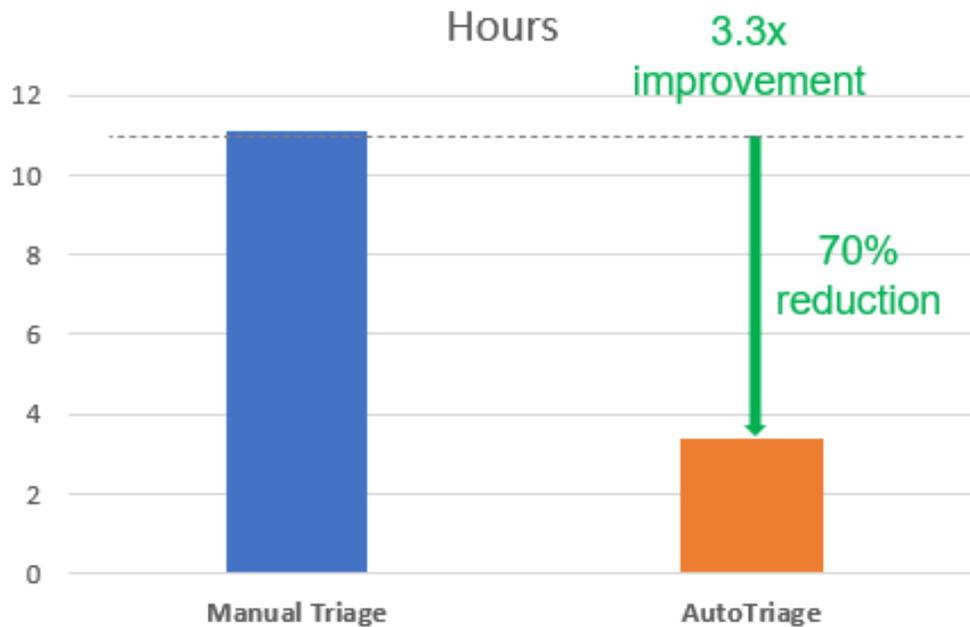
30x, 9x, and 16x efficiency improvement
97%, 89%, and 94% reduction in debug time



Verisium Apps – Customer Feedback (con't)

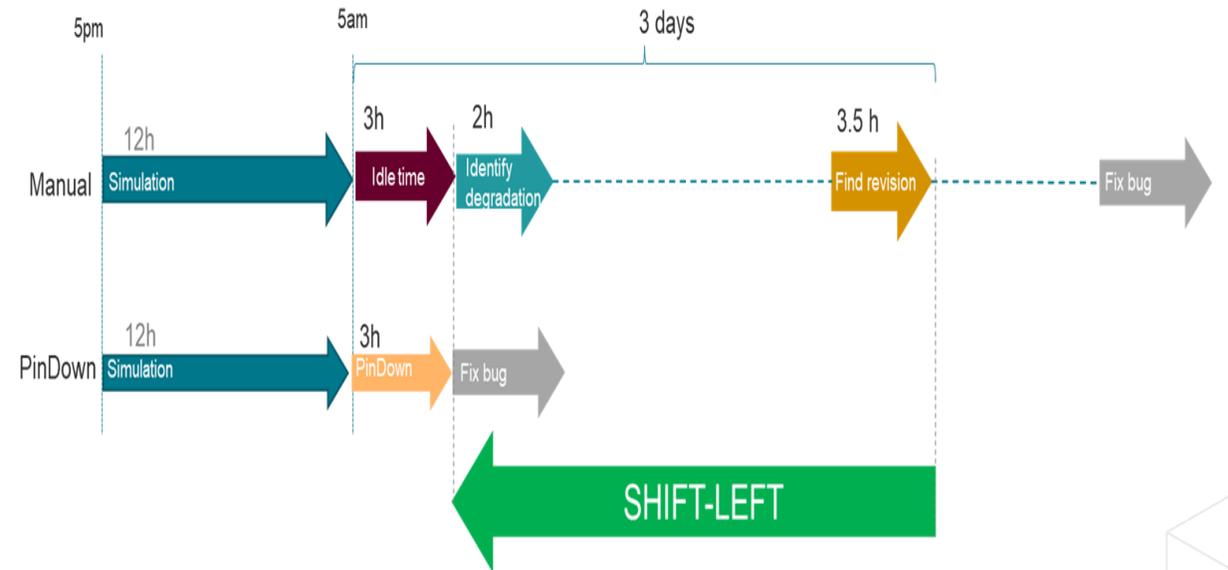
- **AutoTriage**

3.3x efficiency improvement
70% reduction of effort in triage



- **PinDown**

7x improvement in RCA efficiency across regression
4x reduction in total TaT per each bug



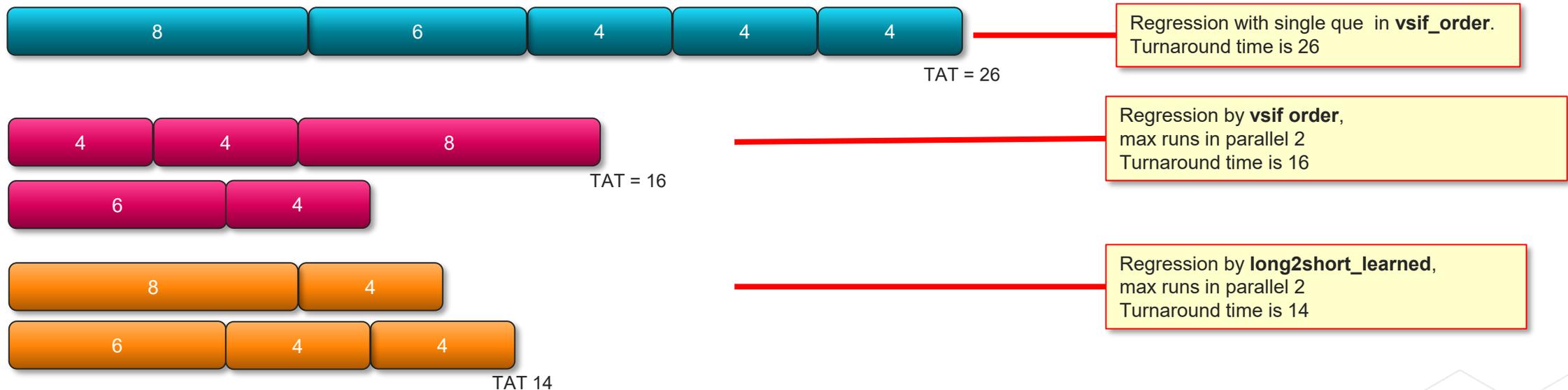


SmartRun, DataMining

AI-Driven **Resource** Optimization

SmartRun

- The goal of **Smart Run** is to provide the fastest turn around time for a regression and improving verification throughput
- Flow
 - **Learning** the typical run durations for tests
 - **Reports** that allow the user to decide what queuing policy and farm resources to apply to optimize the regression throughput.
 - **Reshuffle** and launch new regressions using the new queuing policies.



Resource DataMining – Currently supported



1 Monitor Memory usage and Run-time for runs and tests



2 Calculate Memory usage and Run-time statistics



3 Provide Memory and Run-time report per vsif/specific test



Resource DataMining – Coming Next

1



Enhanced
Performance
Monitoring and
Prediction

2



Performance
Prediction for
Randomized
environments

3



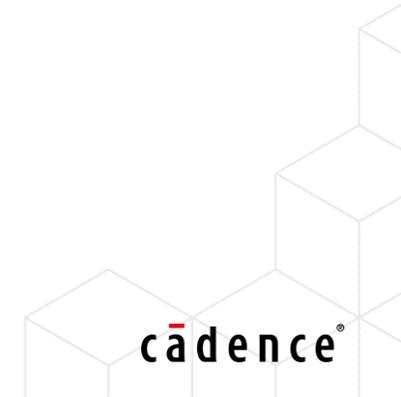
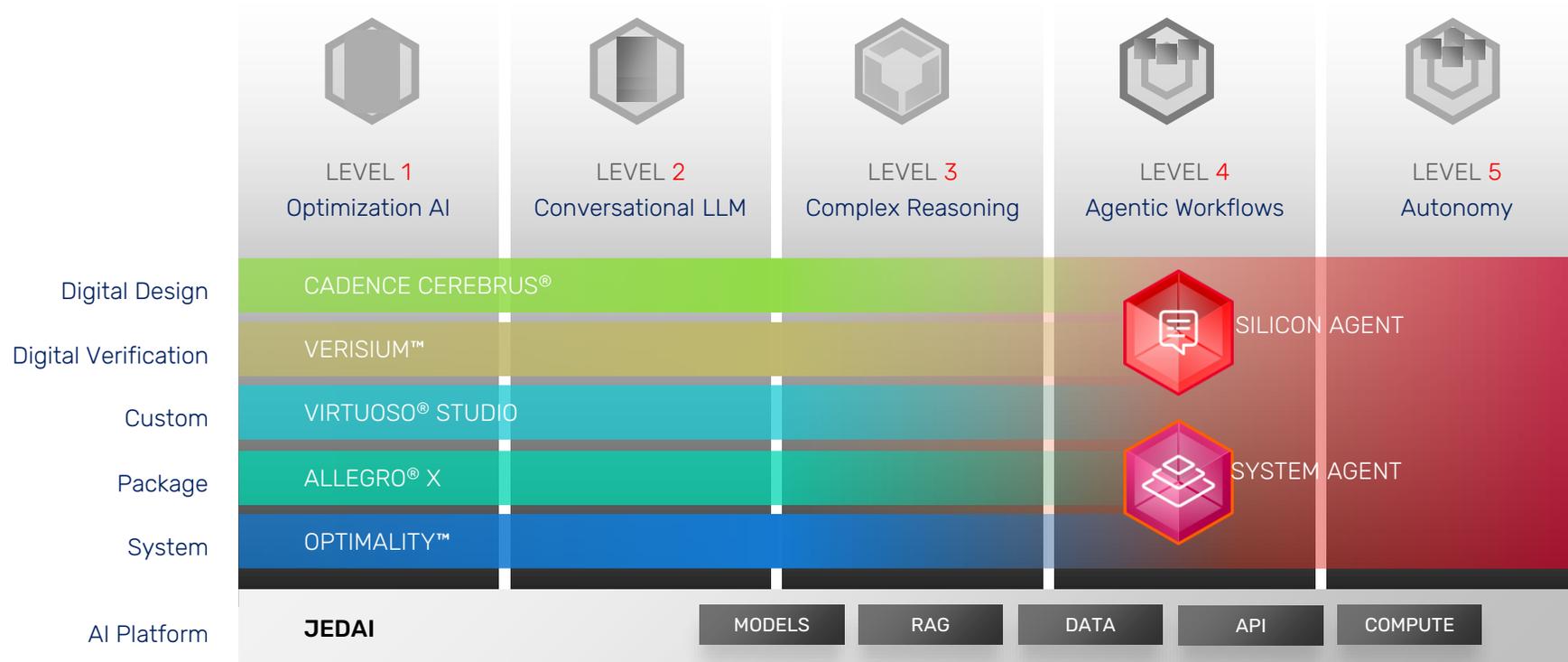
Anomaly
detection for
Performance and
Statuses

Machine Learning



Verisium AI Assistants

The Journey to Autonomous Chip Design

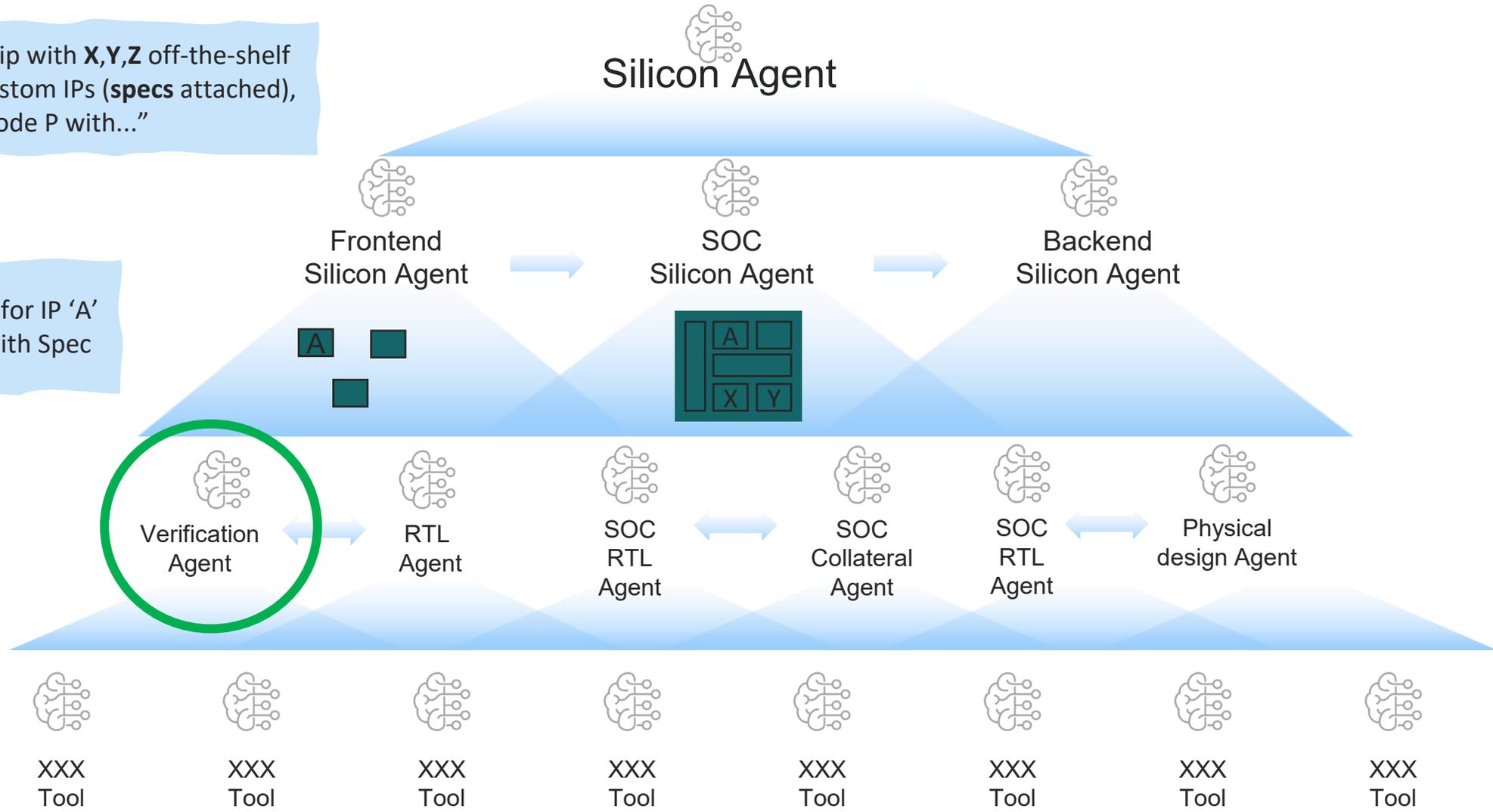




Silicon Agents – from Spec to Chip

“Create a chip with X,Y,Z off-the-shelf IPs, A,B,C custom IPs (specs attached), in process node P with...”

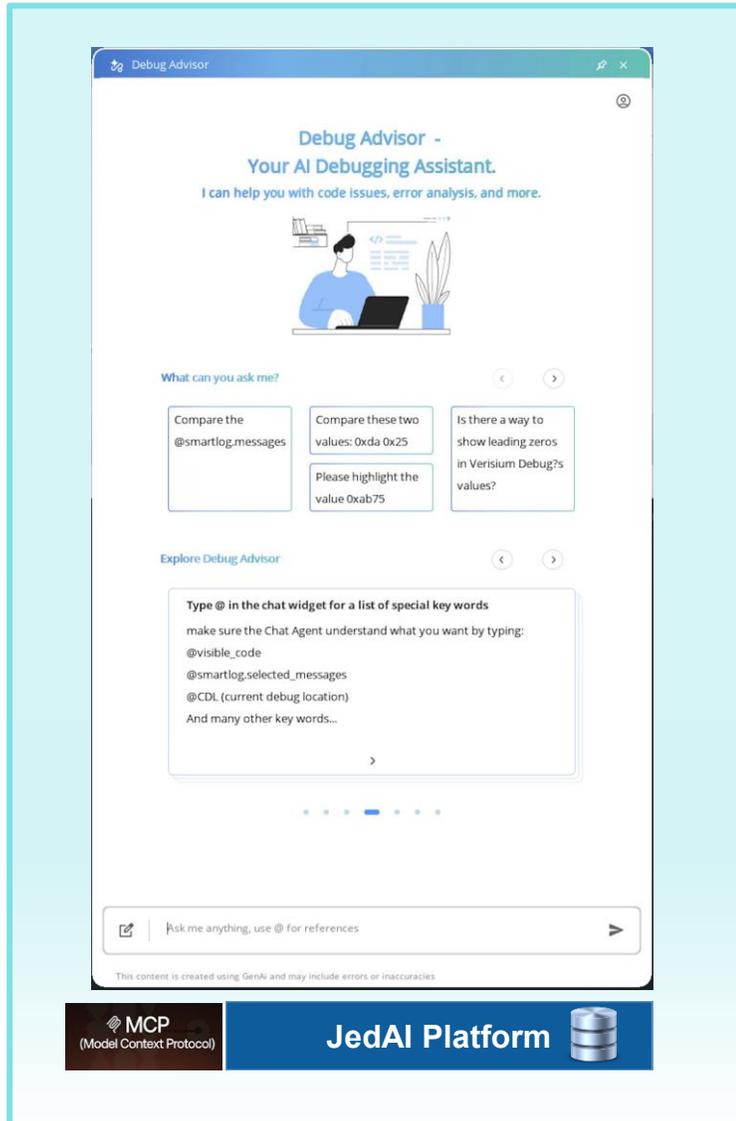
“Create RTL for IP ‘A’ compliant with Spec”





Verisium AI Assistant (Chat)

Verisium AI Assistant - Debug



AI Chat

- Asking questions and getting information from your design (Design, TB, LP, etc.)
- Operating Verisium Debug and summarizing information: Smartlog, Search, Waveform, Randomization, UVM tools
- Answers from Tool help and Setting options

...

AI-Powered Tools

- Code inspection - Read code and suggest potential issues
- Explain signal - collect data about signal and summarize it's functionality
- Complex waveform expression - Use natural language to describe the expression
- Randomization contradiction AI summary

...

Debug Chat examples

DEBUG ADVISOR CHAT

please find all smartlog configuration messages and summarize them for me in a table format

I found several messages that might be relevant to this question. After analyzing the messages, I've extracted the_smartlog configuration messages and summarized them for you in a table format:

Configuration Name	Value
Audio_en	ENABLE
chnl_A_en	ENABLED
chnl_B_en	ENABLED
swap_ab_inmux	NO_SWAP
swap_ab_outmux	NO_SWAP
chnl_A_muter	DISABLED
chnl_B_muter	DISABLED
chnl_A_limiter	DISABLED
chnl_B_limiter	DISABLED
chnl_A_parity	DISABLED
chnl_B_parity	DISABLED
chnl_A_limit_value	35
chnl_B_limit_value	6f
chnl_A_inverter	DISABLED

Please note that all configuration messages were reported at 0fs, indicating they were configured at the beginning of the simulation. [click here](#) to see the messages on which the answer was based

+ | Ask me anything, use @ for references

This content is created using GenAI and may include errors or inaccuracies



Verisium AI Assistant - Management

- High scale by running the Chat on Client
- Persisting the results for future re-use and sharing among multiple users
- Non-textual feedback (e.g.: Ad-hoc table structure)

Verisium AI Assistant

Regression Analysis Results

Variable	Coefficient	Standard Error	t-statistic	p-value	95% Confidence Interval
Intercept	2.5000	0.5000	5.0000	0.0000	1.5000, 3.5000
Age	0.1000	0.0200	5.0000	0.0000	0.0600, 0.1400
Income	0.0500	0.0100	5.0000	0.0000	0.0300, 0.0700
Education	0.2000	0.0500	4.0000	0.0000	0.1000, 0.3000

table please!

one more table please

Variable	Coefficient	Standard Error	t-statistic	p-value	95% Confidence Interval
Intercept	2.5000	0.5000	5.0000	0.0000	1.5000, 3.5000
Age	0.1000	0.0200	5.0000	0.0000	0.0600, 0.1400
Income	0.0500	0.0100	5.0000	0.0000	0.0300, 0.0700
Education	0.2000	0.0500	4.0000	0.0000	0.1000, 0.3000

Ask me anything

MCP (Model Context Protocol) | **JedAI Platform**

Verisium Manager

Regression Analysis Results

Variable	Coefficient	Standard Error	t-statistic	p-value	95% Confidence Interval
Intercept	2.5000	0.5000	5.0000	0.0000	1.5000, 3.5000
Age	0.1000	0.0200	5.0000	0.0000	0.0600, 0.1400
Income	0.0500	0.0100	5.0000	0.0000	0.0300, 0.0700
Education	0.2000	0.0500	4.0000	0.0000	0.1000, 0.3000

table please!

one more table please

Variable	Coefficient	Standard Error	t-statistic	p-value	95% Confidence Interval
Intercept	2.5000	0.5000	5.0000	0.0000	1.5000, 3.5000
Age	0.1000	0.0200	5.0000	0.0000	0.0600, 0.1400
Income	0.0500	0.0100	5.0000	0.0000	0.0300, 0.0700
Education	0.2000	0.0500	4.0000	0.0000	0.1000, 0.3000

Ask me anything

Example

In the last nightly regression, the overall coverage dropped; what is the reason for that?

Summary analysis shows that the function coverage dropped in 20% and the code coverage dropped in 9% with [10 new tests](#) that failed. Do you like to perform further analysis? it would take few minutes.

Yes

Here are potential causes for the coverage drop:
File: [SOC_123.sv](#), line 112 was modified
Tests: X Y Z had lower coverage vs. previous runs

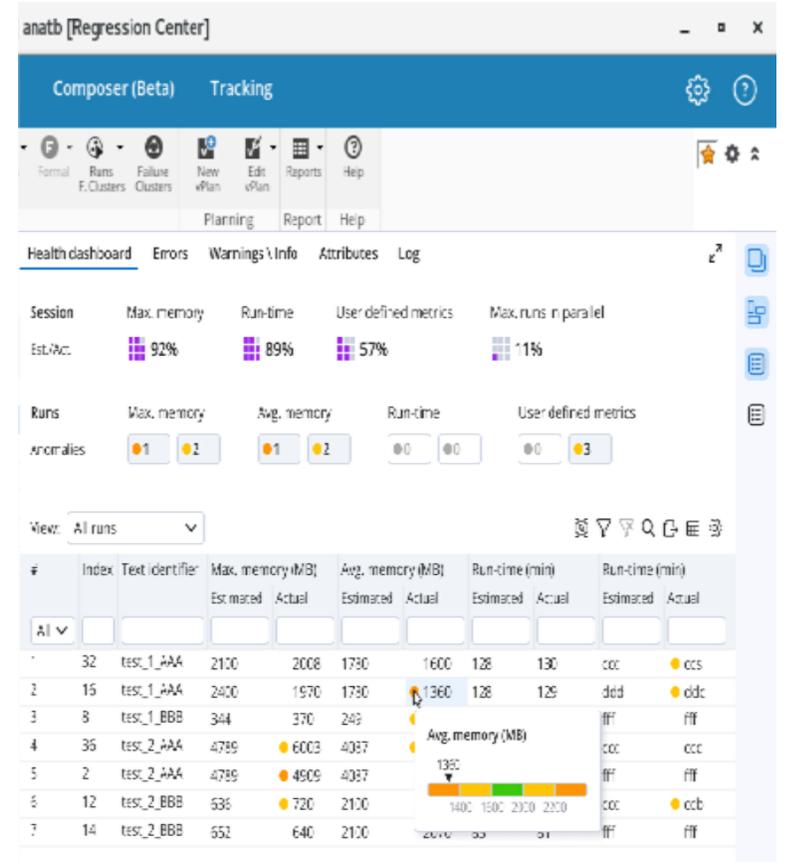


Verisium AI Assistant Automated Flows

Regression Health

Optimized regression and real-time analysis

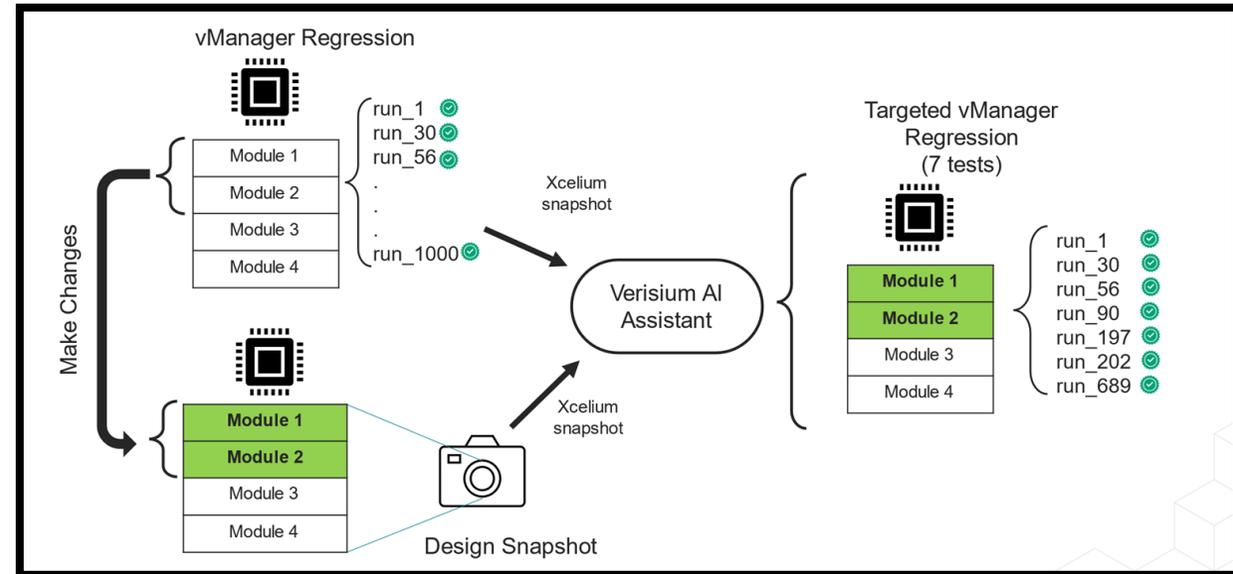
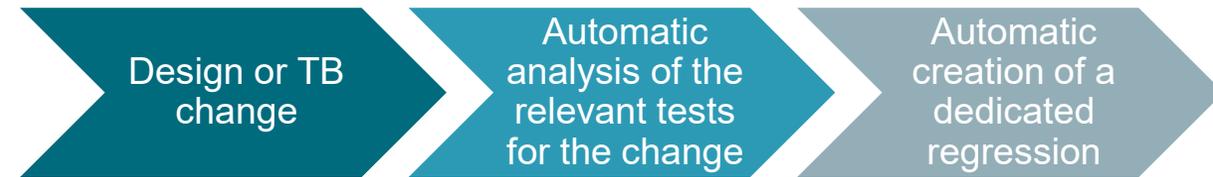
- User Action: User initiates a full regression
- System's Response:
 - Optimize **scheduling (TAT)** for test execution
 - Based on priority, dependencies, and resource availability.
 - Optimize **compute resources** consumption
 - Recommend potential cost saving
 - Predict **estimated completion time, memory** consumption
 - Identify **anomalies**
 - Provide **real-time dashboard**
 - Regression status, resource usage, anomalies, ..

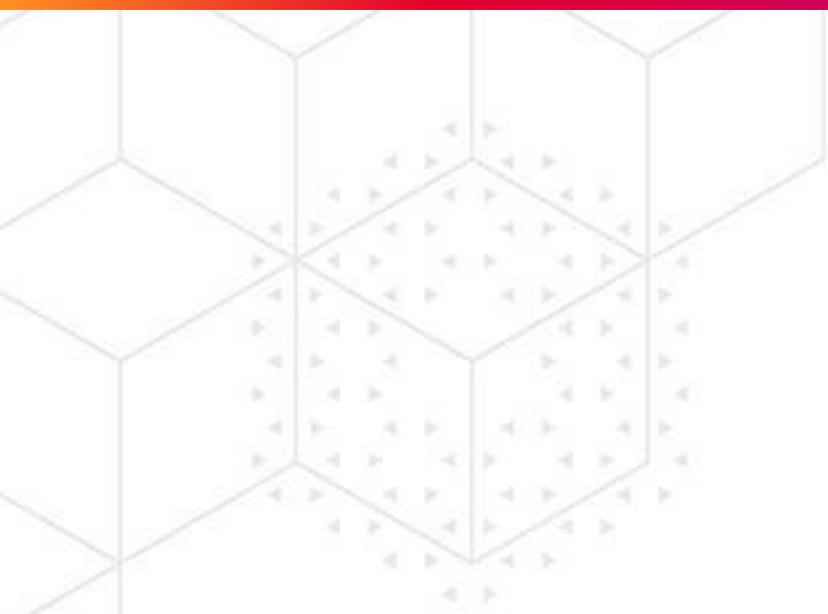


Target Design Change

Tailored testing for design and testbench updates

- User Action: User fixes a bug and wants to verify the fix
- Solution:
 - Automatically **create** and launch a change-related **sanity regression**
 - Seamless and fluent integration btw Verisium Manager, SimAI and AutoFocus
 - The launched regression may be [constraints] random regression, or a subset of the golden regression provided by the user.





cādence[®]

© 2025 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at <https://www.cadence.com/go/trademarks> are trademarks or registered trademarks of Cadence Design Systems, Inc. Accellera and SystemC are trademarks of Accellera Systems Initiative Inc. All Arm products are registered trademarks or trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All MIPI specifications are registered trademarks or service marks owned by MIPI Alliance. All PCI-SIG specifications are registered trademarks or trademarks of PCI-SIG. All other trademarks are the property of their respective owners.