Acceleration of product and test environment using SystemC-TLM

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Agenda

• Overview

• Virtual Platform of the Product (VP-P)

• Virtual Platform of the Testers (VP-T)

• Proof Of Concept with TestStand

• Conclusions
Overview (1)
Overview (1)

Hardware

Software

Wait
Overview (1)

Hardware ➔ Wait ➔ Software ➔ Provide ➔ Product or Prototype

Product Development

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Overview (1)

Product Development → Test Equipment + Sequences Development

Hardware → Software → Product or Prototype → Product Verification

Wait → Provide → Wait

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Problem Statement: Can we optimize this engineering flow?
Overview (2)
Overview (2)
Prototype or Product Under Test

Firmware

Test Equipment

Controllers
Signal Generators
Counters

Custom Libs

PICTURE_Lib
Injection_Lib
BinaryIO_Lib

TestStand

Test Sequences

Drive the test equipment

Classical approach
Overview (2)

Prototype or Product Under Test

Firmware

Test Equipment

Controllers

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Custom Libs

PICTURE_Lib

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Test Stand

Generate test signals

Drive the test equipment

Test Sequences

Classical approach
Overview (2)

Prototype or Product Under Test

- Firmware

Test Equipment

- Controllers
- Signal Generators
- Counters

Custom Libs

- PICTURE_Lib
- Injection_Lib
- BinaryIO_Lib

TestStand

Classical approach

Receive test signals

Generate test signals

Drive the test equipment

Test Sequences
Overview (2)

Prototype or Product Under Test
- Firmware

Test Equipment
- Controllers
  - Signal Generators
  - Counters
- Custom Libs
  - PICTURE_Lib
  - Injection_Lib
  - BinaryIO_Lib
- TestStand

Receive test signals
Generate test signals
Drive the test equipment
Test Sequences

Testbench

Classical approach

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Prototype or Product Under Test
- Firmware

Test Equipment
- Controllers
- Signal Generators
- Counters

Custom Libs
- PICTURE_Lib
- Injection_Lib
- BinaryIO_Lib

TestStand

Overview (3)

Virtual Platforms (VP)

VP-Product (VP-P)
- Firmware

Virtual Platform of the Test Equipment (VP-T)

Receive test signals

Generate test signals

Drive the test equipment

Test Sequences

Testbench

Classical approach

Proposed approach
Prototype or Product Under Test

Test Equipment
- Controllers
- Signal Generators
- Counters

Custom Libs
- PICTURE_Lib
- Injection_Lib
- BinaryIO_Lib

TestStand

Virtual Platforms (VP)

VP-Product (VP-P)

Firmware

Virtual Platform of the Test Equipment (VP-T)

TestStand

Generate test signals

Test Sequences

Test Equipment

Controllers

Signal Generators

Counters

Custom Libs

PICTURE_Lib

Injection_Lib

BinaryIO_Lib

Classical approach

Proposed approach

Receive test signals

Generate test signals

Drive the test equipment

Test Sequences

Prepare

Testbench

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Overview (4)

Wait

Hardware

Software

Provide

Product or Prototype

Wait

Product Verification

Product development

Test Equipment + Sequences Development
Overview (4)

Test Sequences AND Product Development in parallel

Hardware

VP-P

Parallel

Software

Parallel

Test Sequences Preparation

VP-T

Verification

And

Test

Integration

H/W Design

S/W Design

Specification
Parallel Test Sequences Preparation

Start preparing product AND test sequences in anticipation
Virtual Platform of the Product (VP-P)

• QEMU model CPUs

• SystemC model peripherals

• QEMU + SystemC Handshake

• Some Models can communicate to the real-world (ethernets, UARTs)
Virtual Platform of the Testbench (VP-T)

- Generates signals on models
- Triggered through JSON Command Line
- Accessible with TCP
Demonstrator to prove the concept

Real-World TestStand sends test sequences and command test equipments on the real product.
Demonstrator to prove the concept

Real-World TestStand sends test sequences and command test equipments on the real product

Using Virtual Platforms TestStand Communicates with a remote PC w/VPs.
Demonstrator to prove the concept

Real-World TestStand sends test sequences and command test equipments on the real product.

Config change to switch between the two configs.

Using Virtual Platforms TestStand Communicates with a remote PC w/VPs.
Results

• Engineering Optimized on a 6 months project
  – 1 month gain for software bugs tracked in advance (VP-P gain)
  – 2 month gain for test sequences preparation (VP-T gain)

• Bonus: Same advantages as classical VP-P approach but with virtual verification included:
  – Reusability
  – Verbosity
  – No risk for human
  – Unlimited instantiation of VPs (**10k€ - 70k€ of hw for testbench duplication**)
Limitations

- SystemC-TLM LT models $\Leftrightarrow$ Timing Inaccurate $\Leftrightarrow$ Limited to **functional** product verification.

- Tests limited to firmware functions of the product (no mechanics, hydraulic tests)
Questions

Finalize slide set with questions slide