Acceleration of product and test environment using SystemC-TLM

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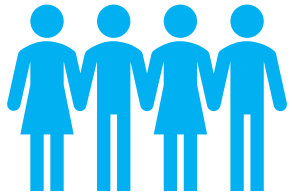
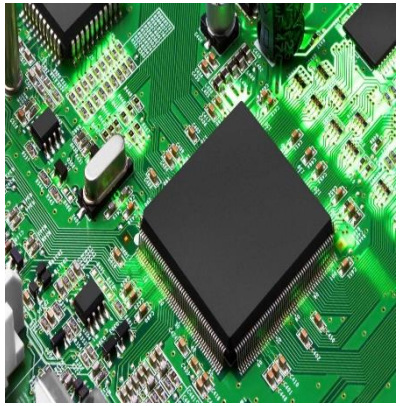
2018 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

Agenda

- Overview
- Virtual Platform of the Product (VP-P)
- Virtual Platform of the Testers (VP-T)
- Proof Of Concept with TestStand
- Conclusions

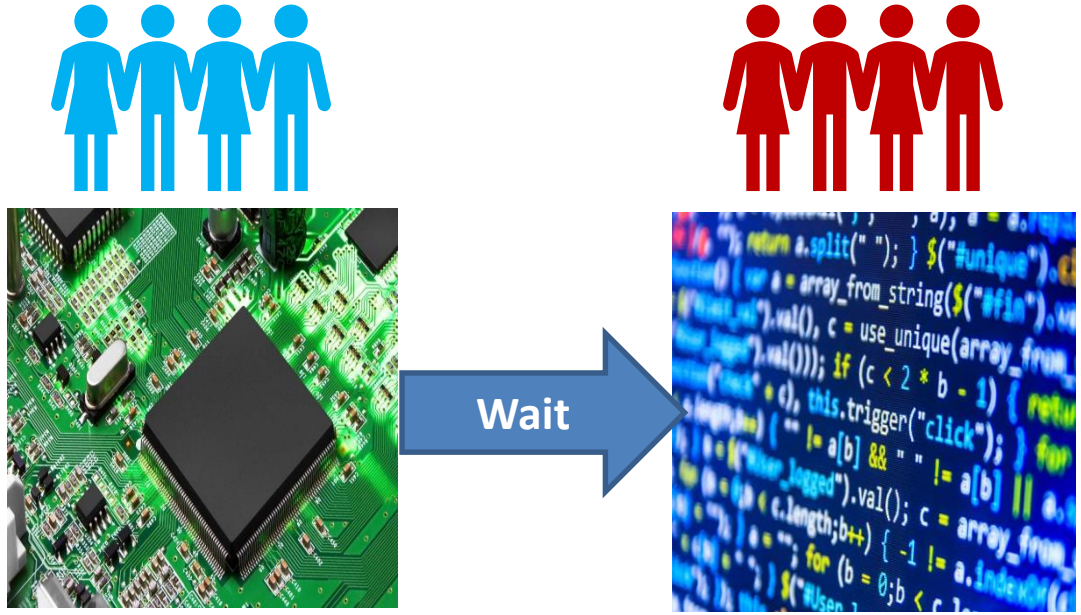
Overview (1)





Hardware

Overview (1)



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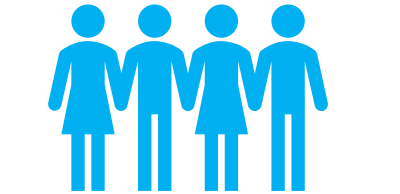

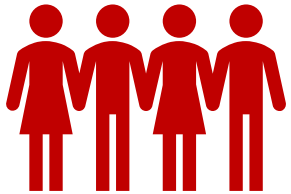

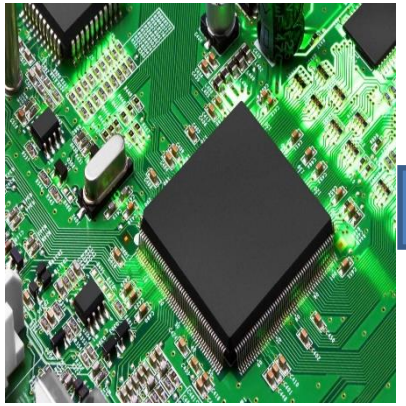

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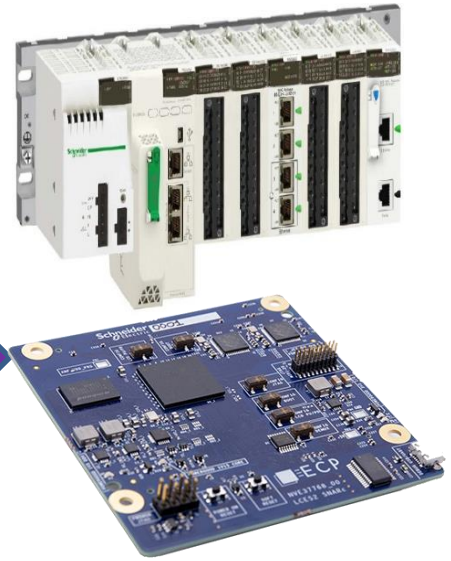


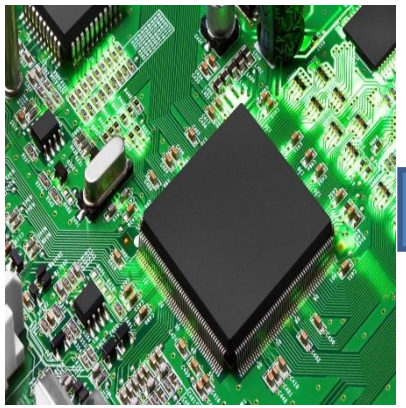
Hardware

Software

Product or Prototype

Product Development

Overview (1)



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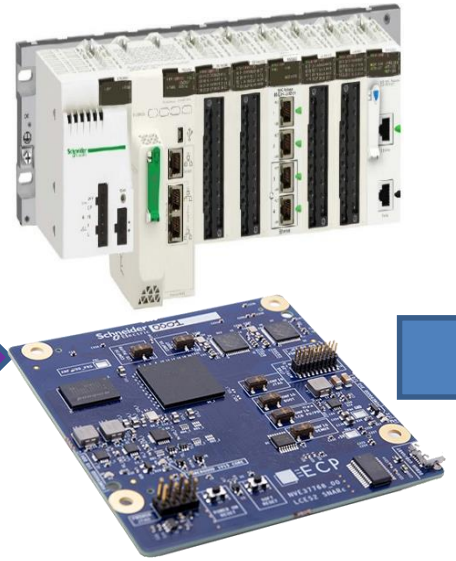

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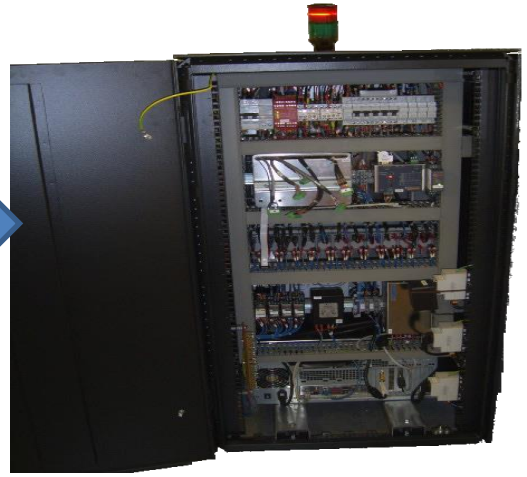


Hardware

Software

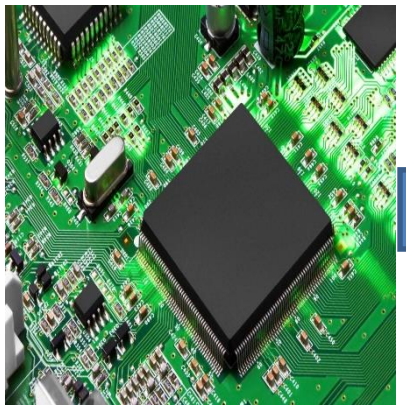
Product or Prototype

Product Verification

Product Development

Test Equipment + Sequences Development

Overview (1)



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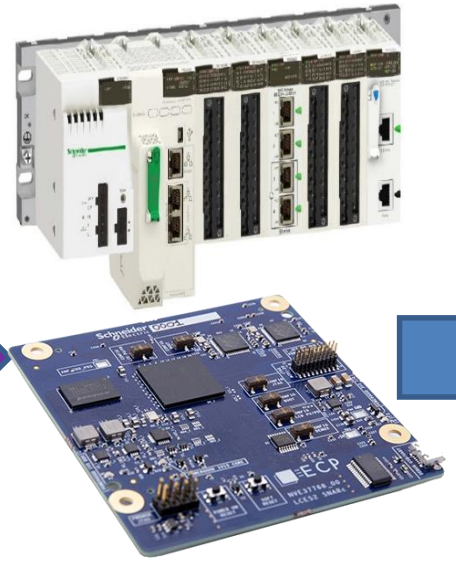

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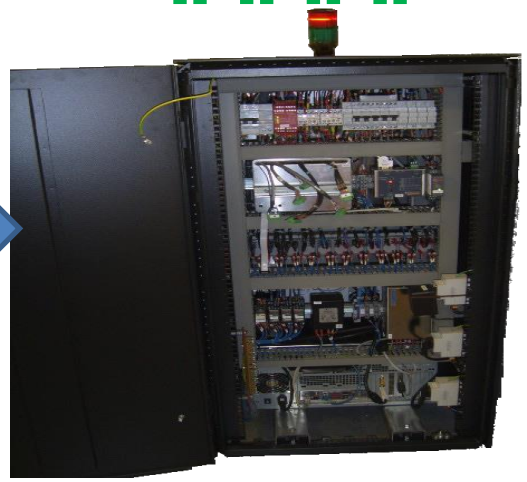


Hardware

Software

Product or Prototype

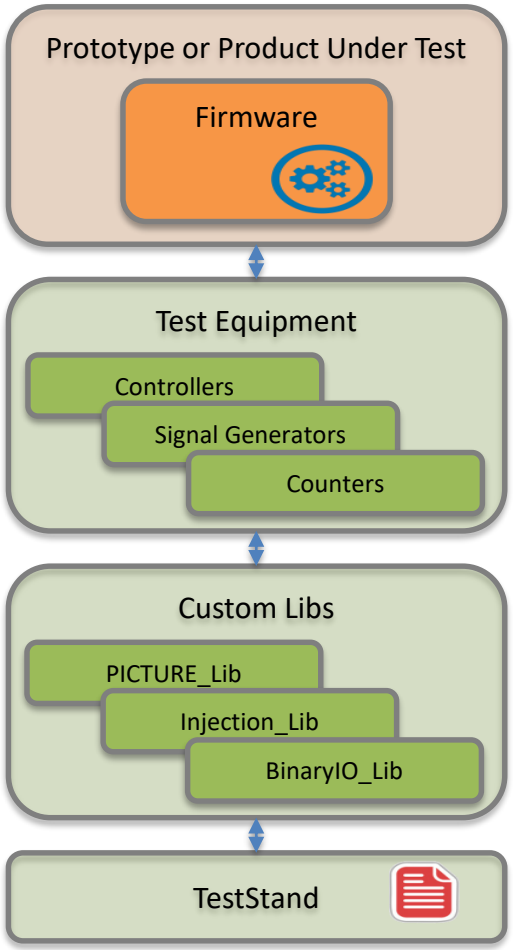
Product Verification

Product Development

Test Equipment + Sequences Development

Problem Statement : Can we optimize this engineering flow ?

Overview (2)



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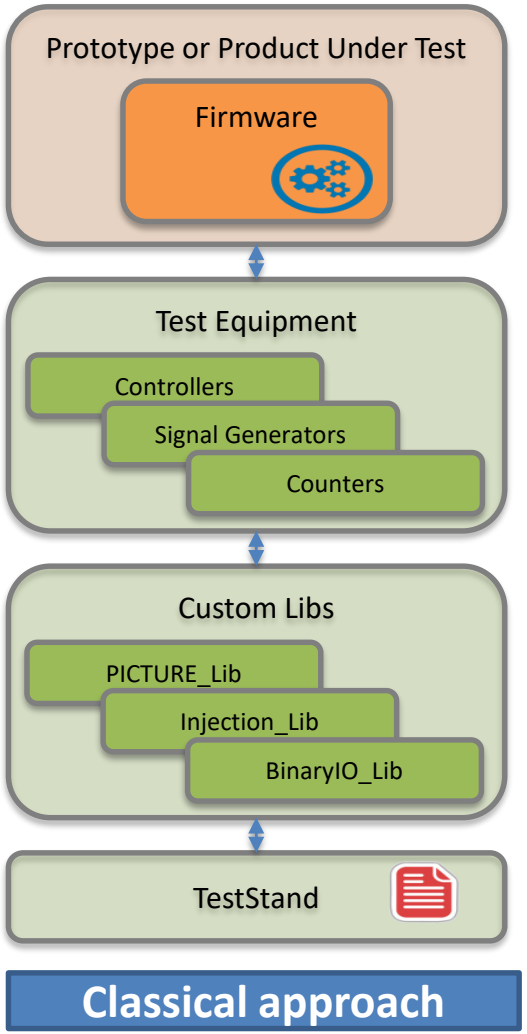
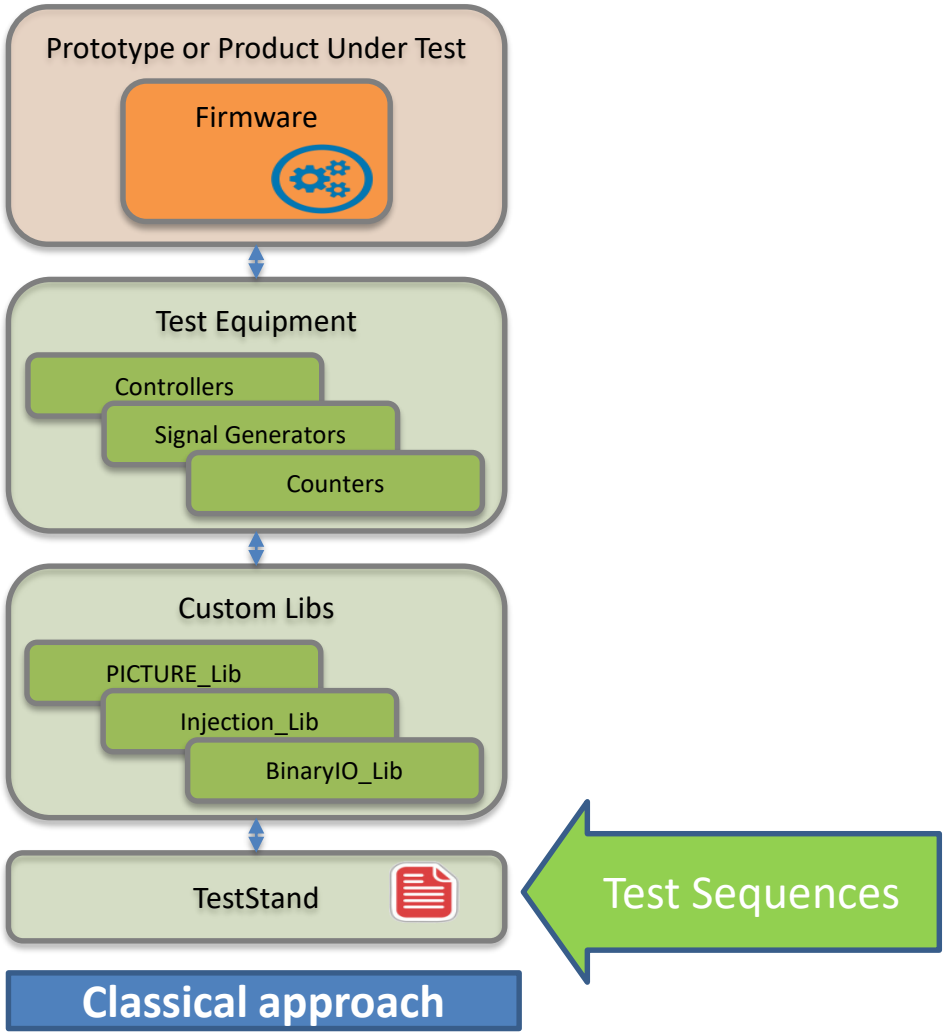


Classical approach

Overview (2)



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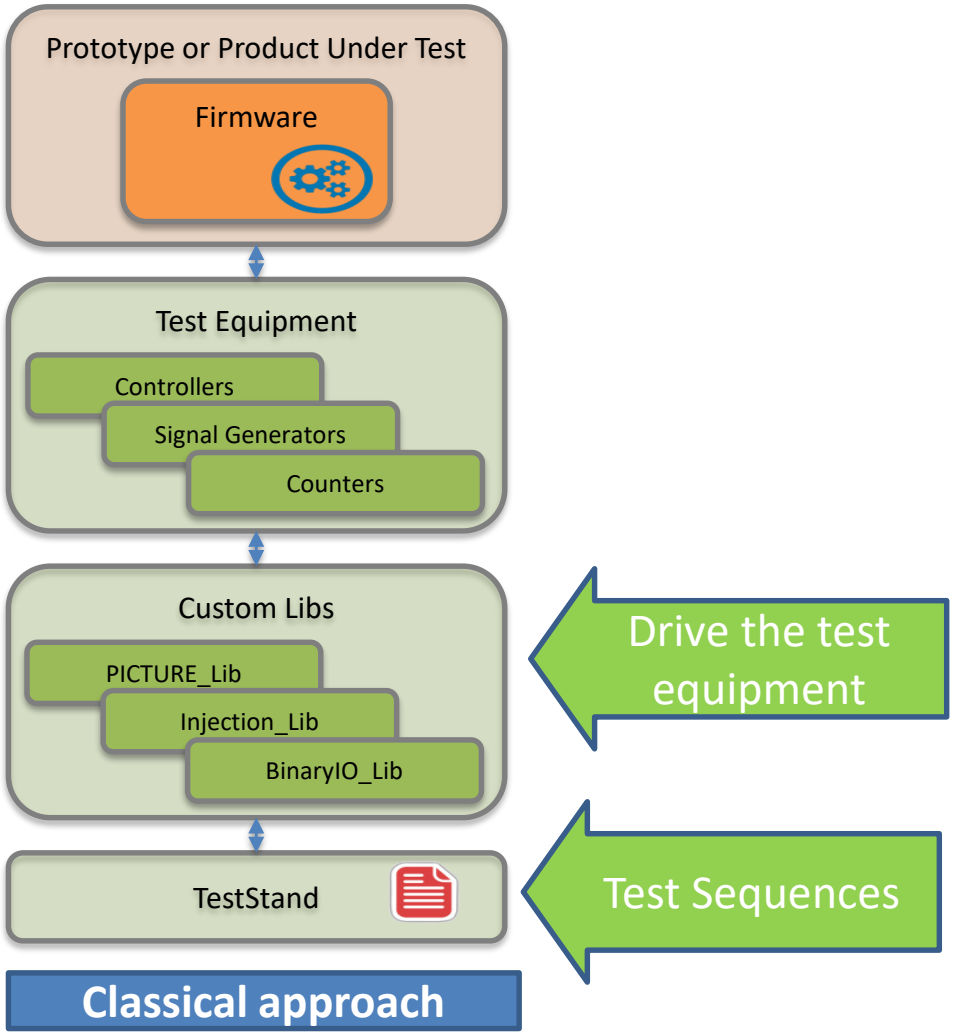

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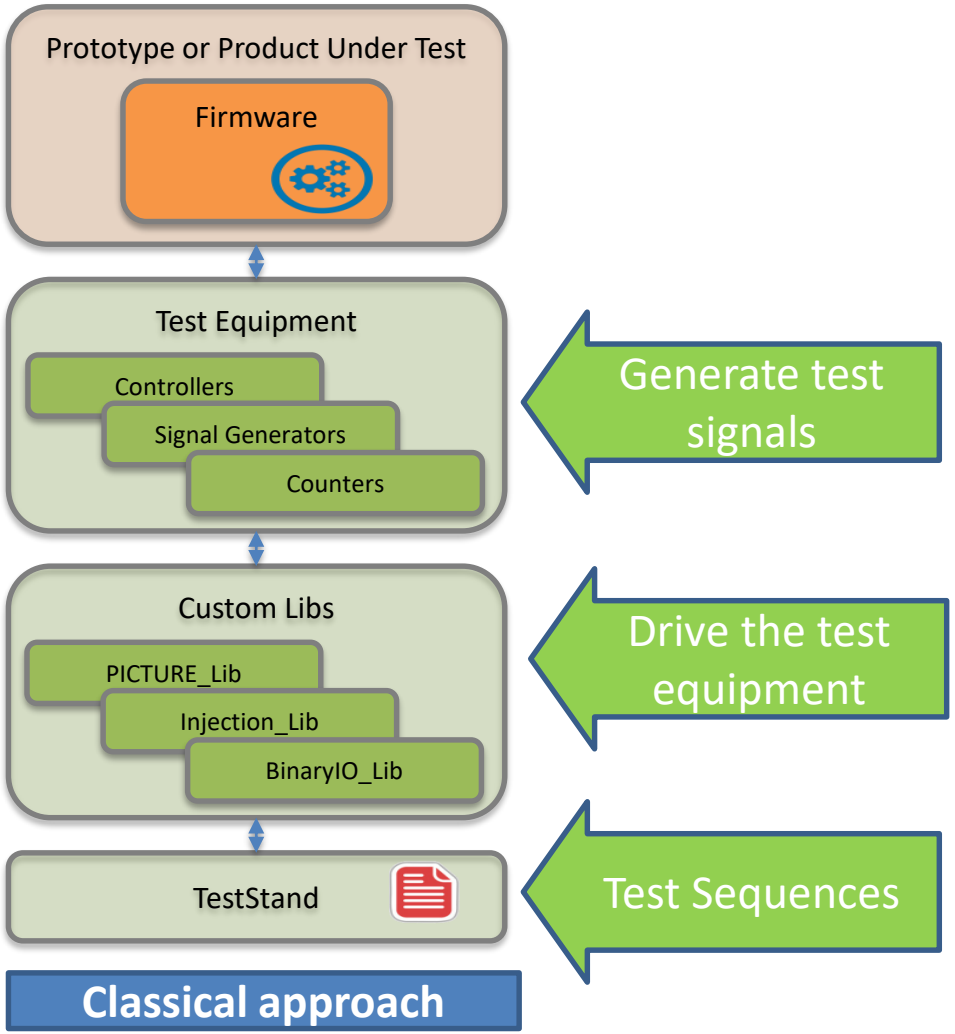
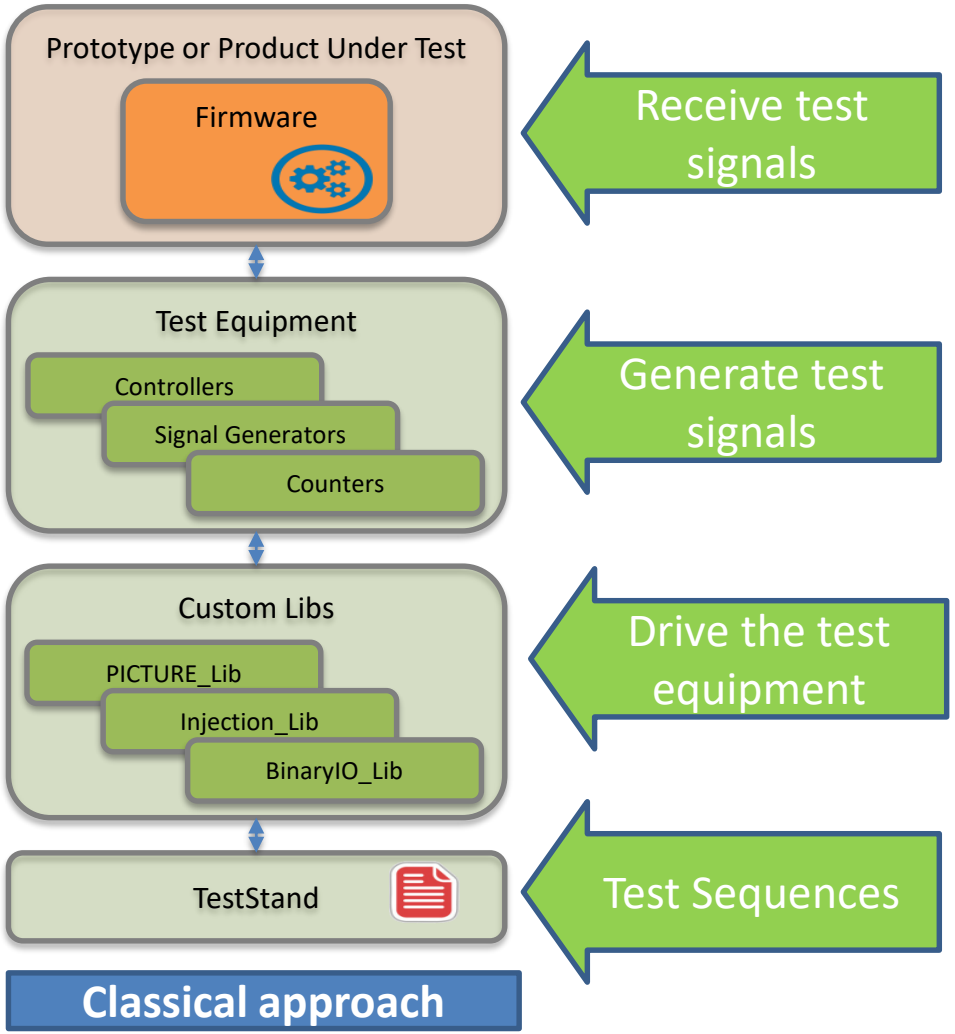


Generate test signals

Drive the test equipment

Test Sequences

Overview (2)



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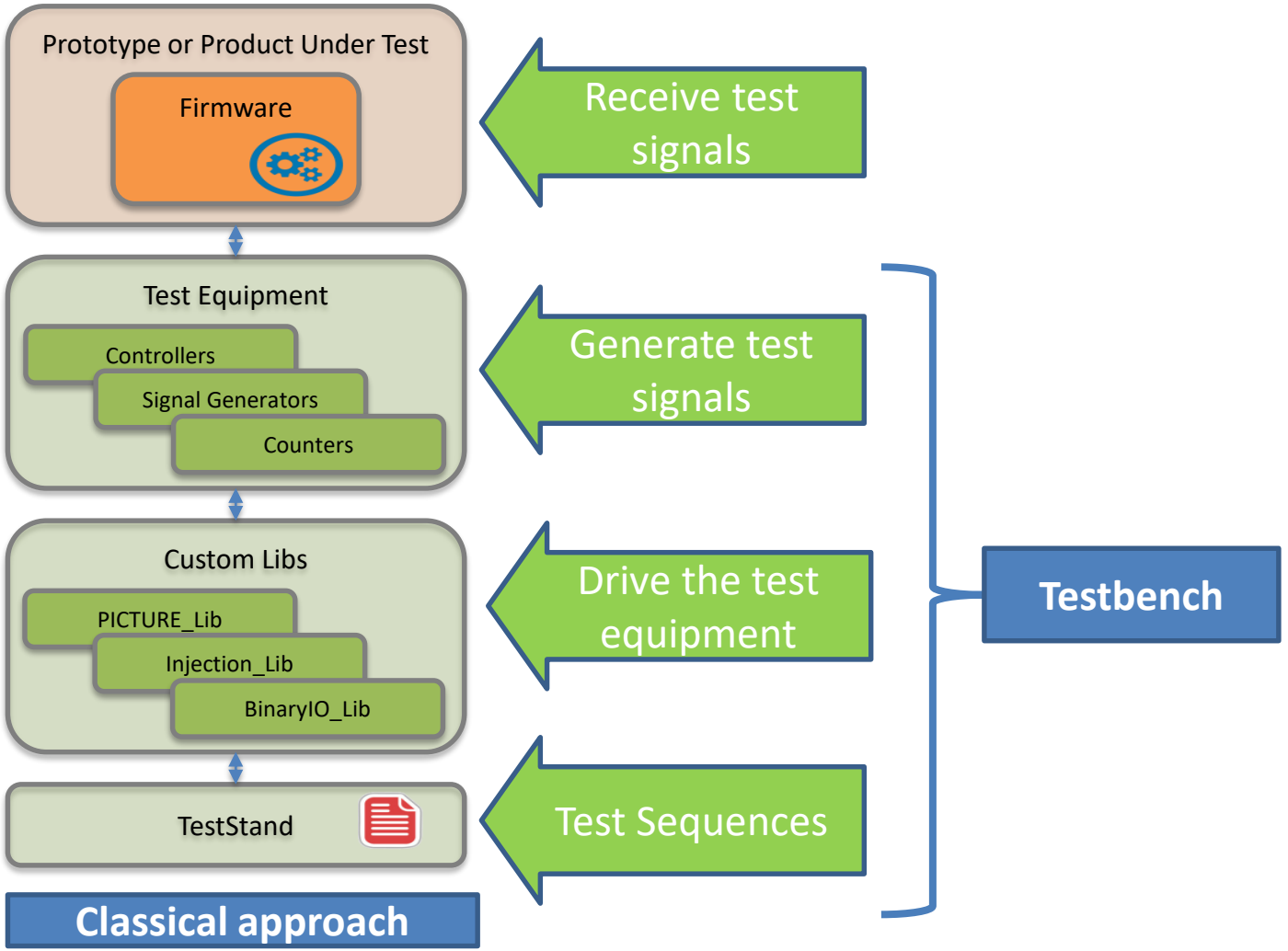
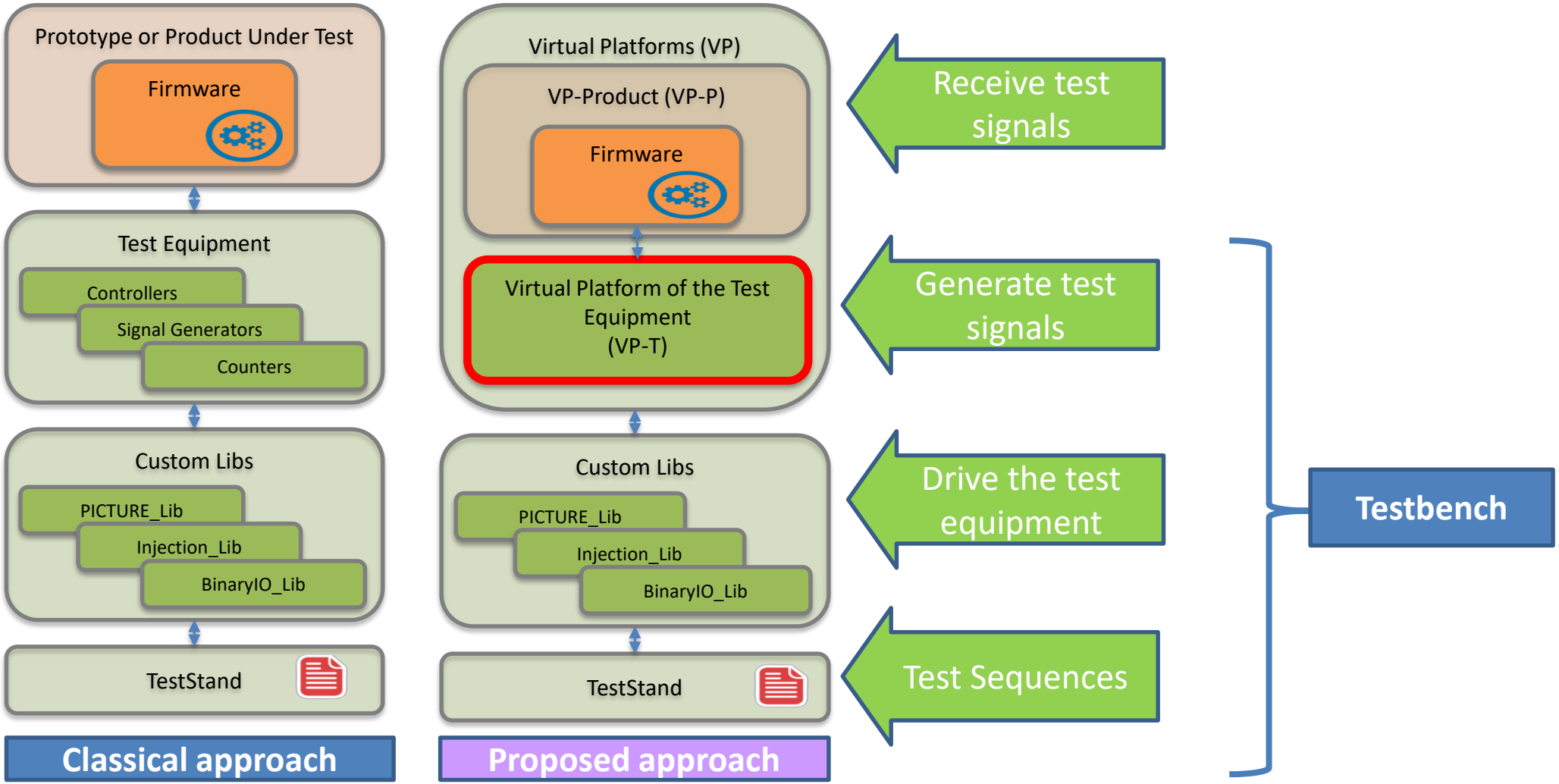


Overview (3)



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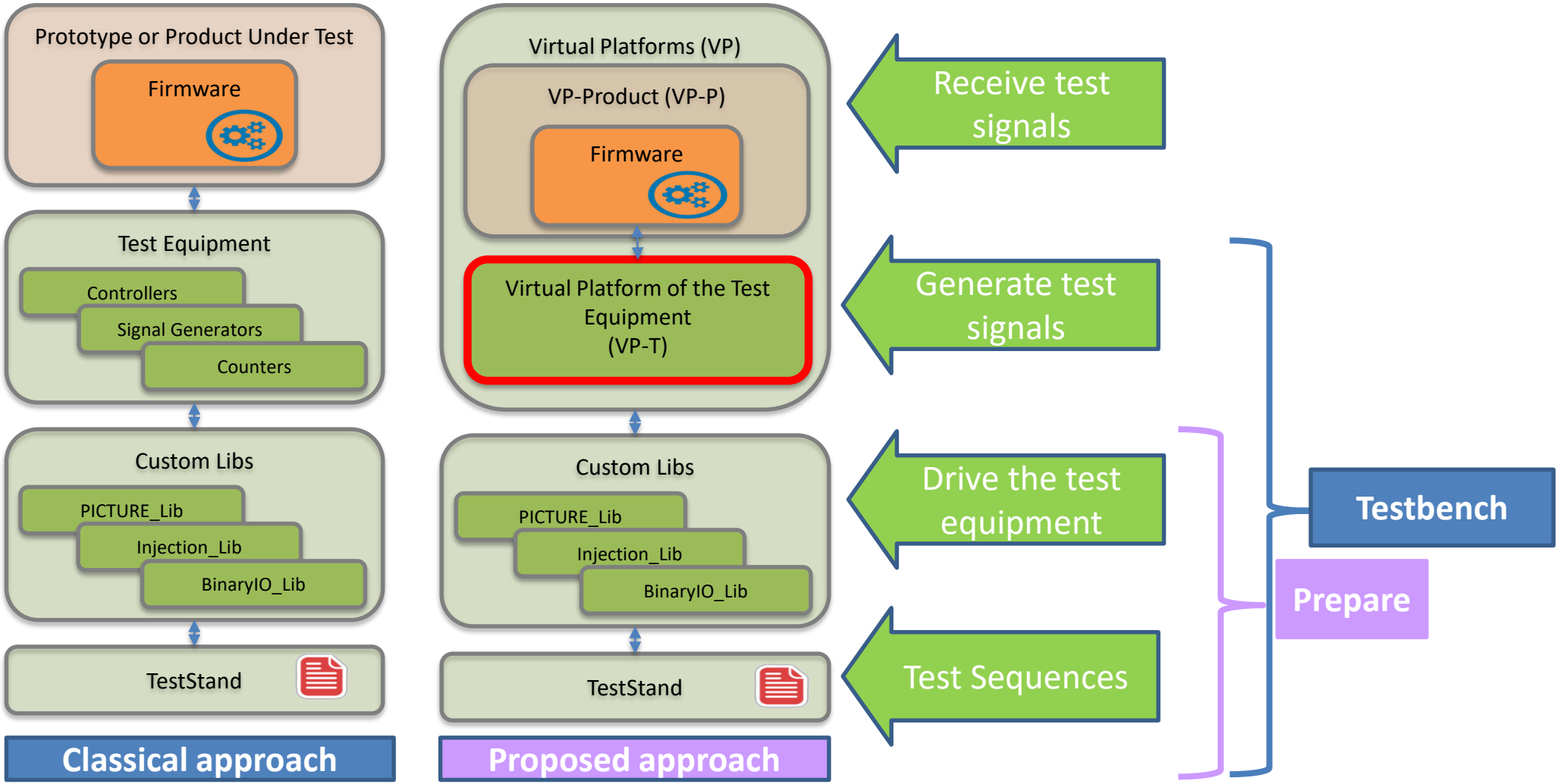
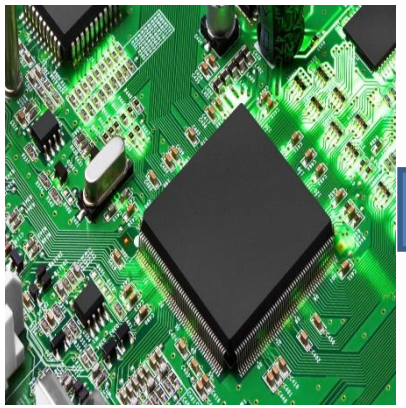

Prototype or Product Under Test
Firmware
Test Equipment
Controllers
Signal Generators
Counters
Custom Libs
PICTURE_Lib
Injection_Lib
BinaryIO_Lib
TestStand
Classical approach
Virtual Platforms (VP)
VP-Product (VP-P)
Firmware
Virtual Platform of the Test Equipment (VP-T)
Custom Libs
PICTURE_Lib
Injection_Lib
BinaryIO_Lib
TestStand
Proposed approach
Receive test signals
Generate test signals
Drive the test equipment
Test Sequences
Testbench
Prepare

Overview (4)



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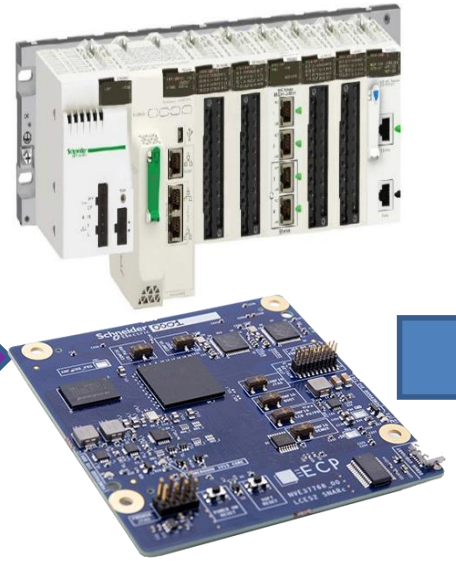

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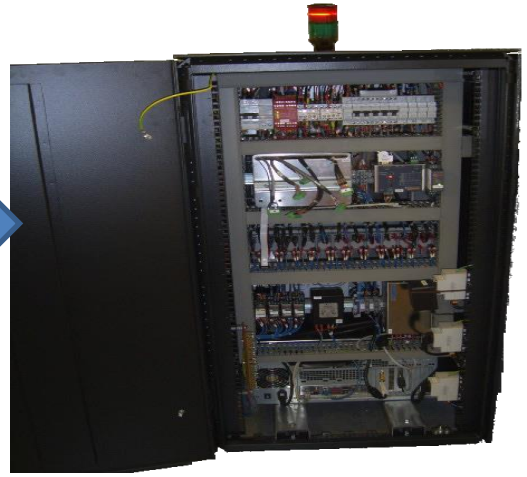
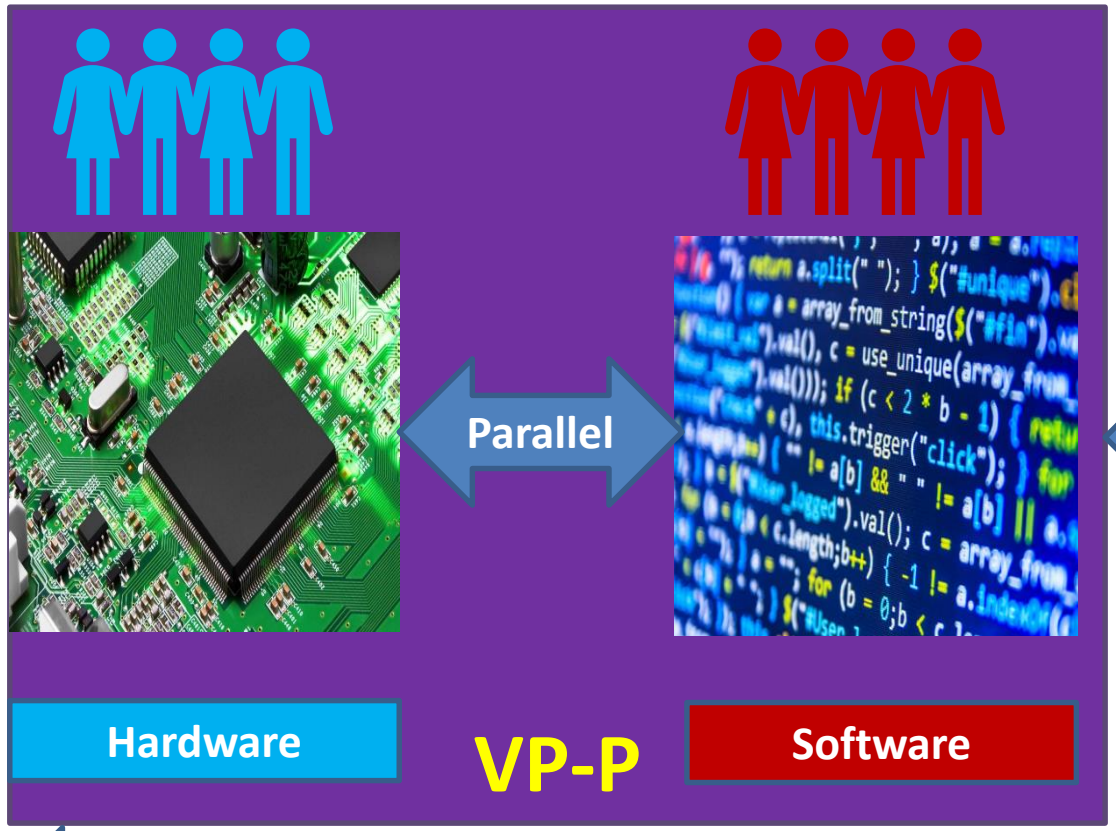


Hardware | Software | Product or Prototype | Product Verification

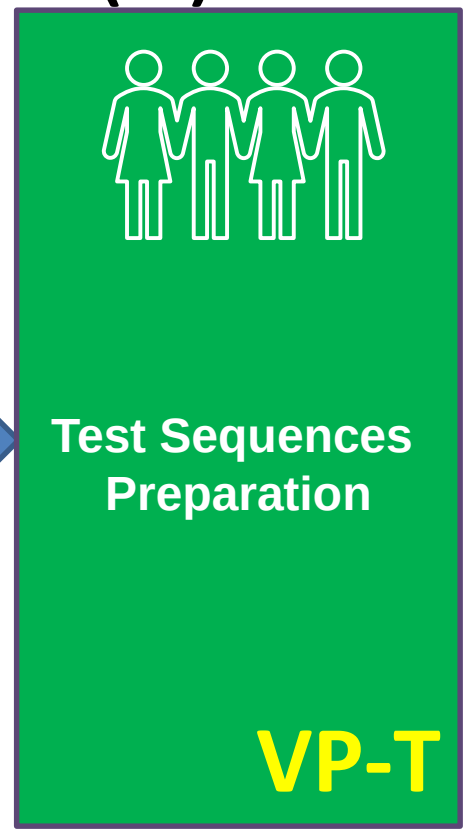
Product development → Test Equipment + Sequences Development

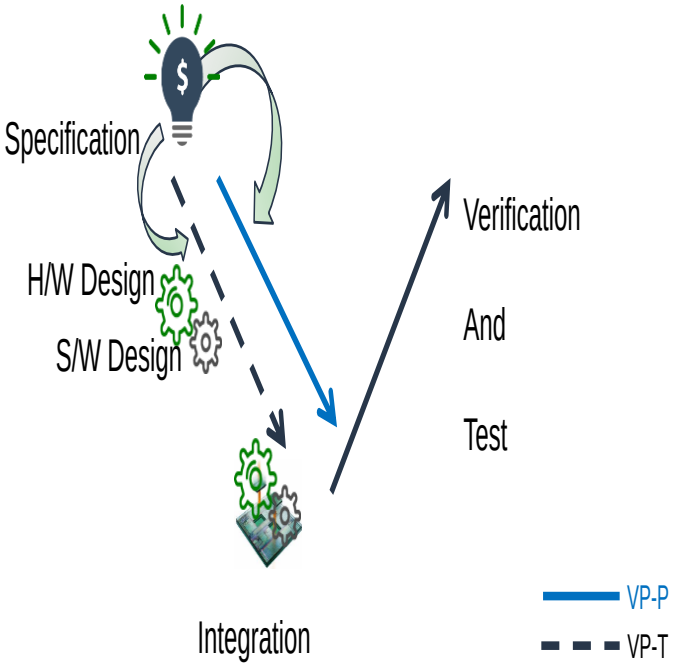
Overview (4)



Parallel

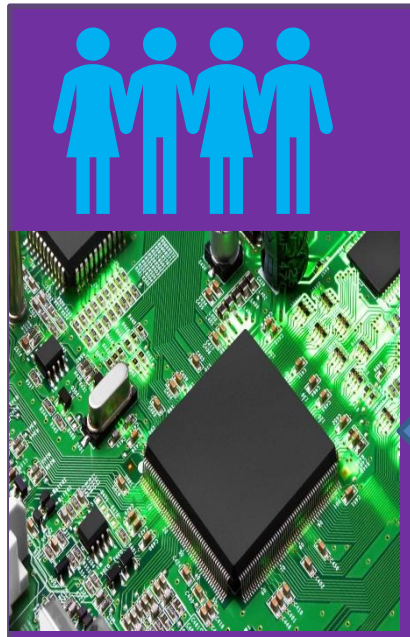
Parallel





Test Sequences AND Product Development in parallel

Overview (4)



Hardware

Parallel

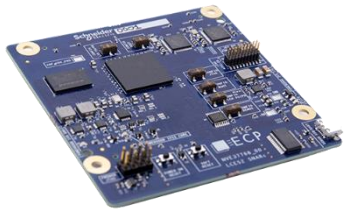
Software

VP-P

Parallel

Test Sequences Preparation

VP-T

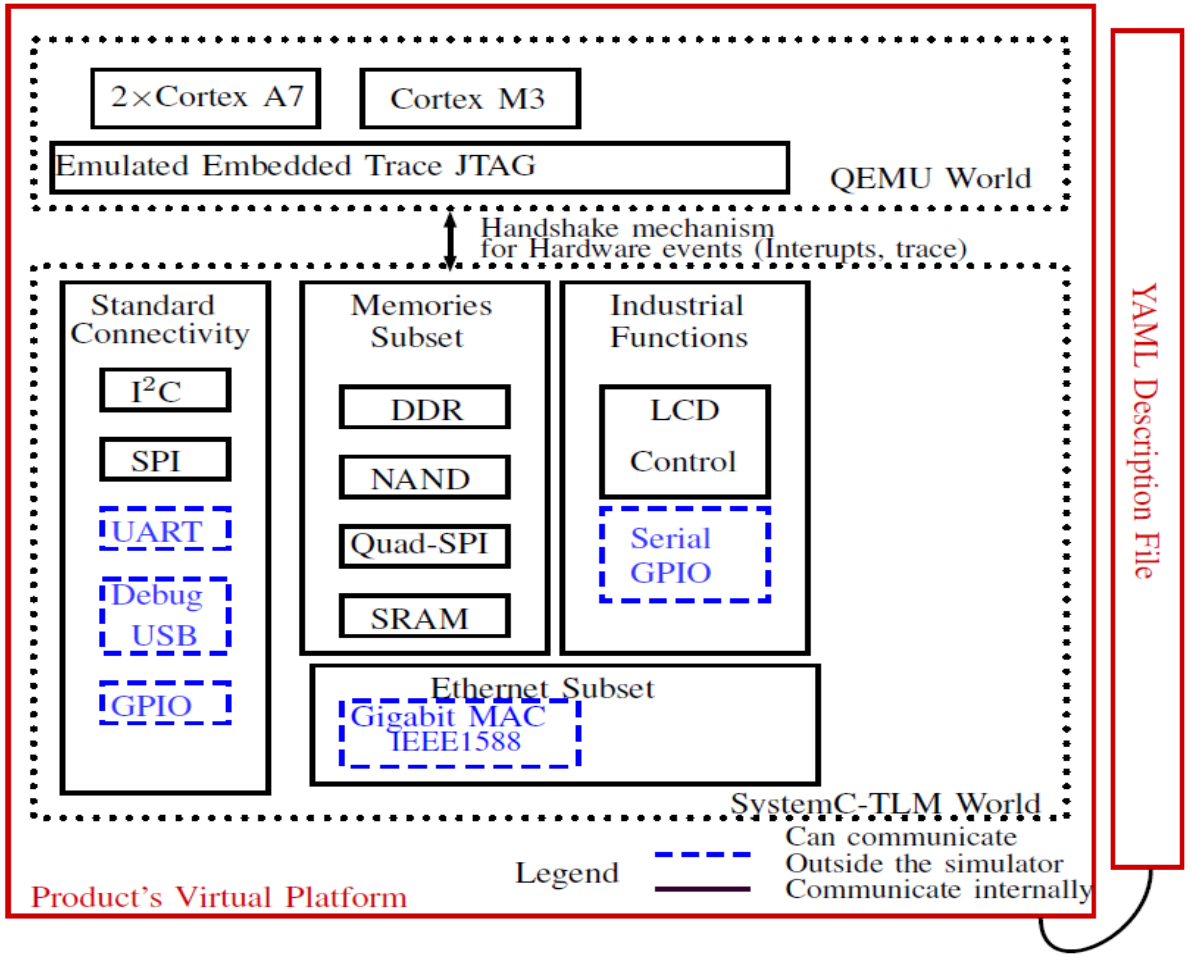


Test Sequences AND Product Development in parallel

Start preparing product AND test sequences in anticipation

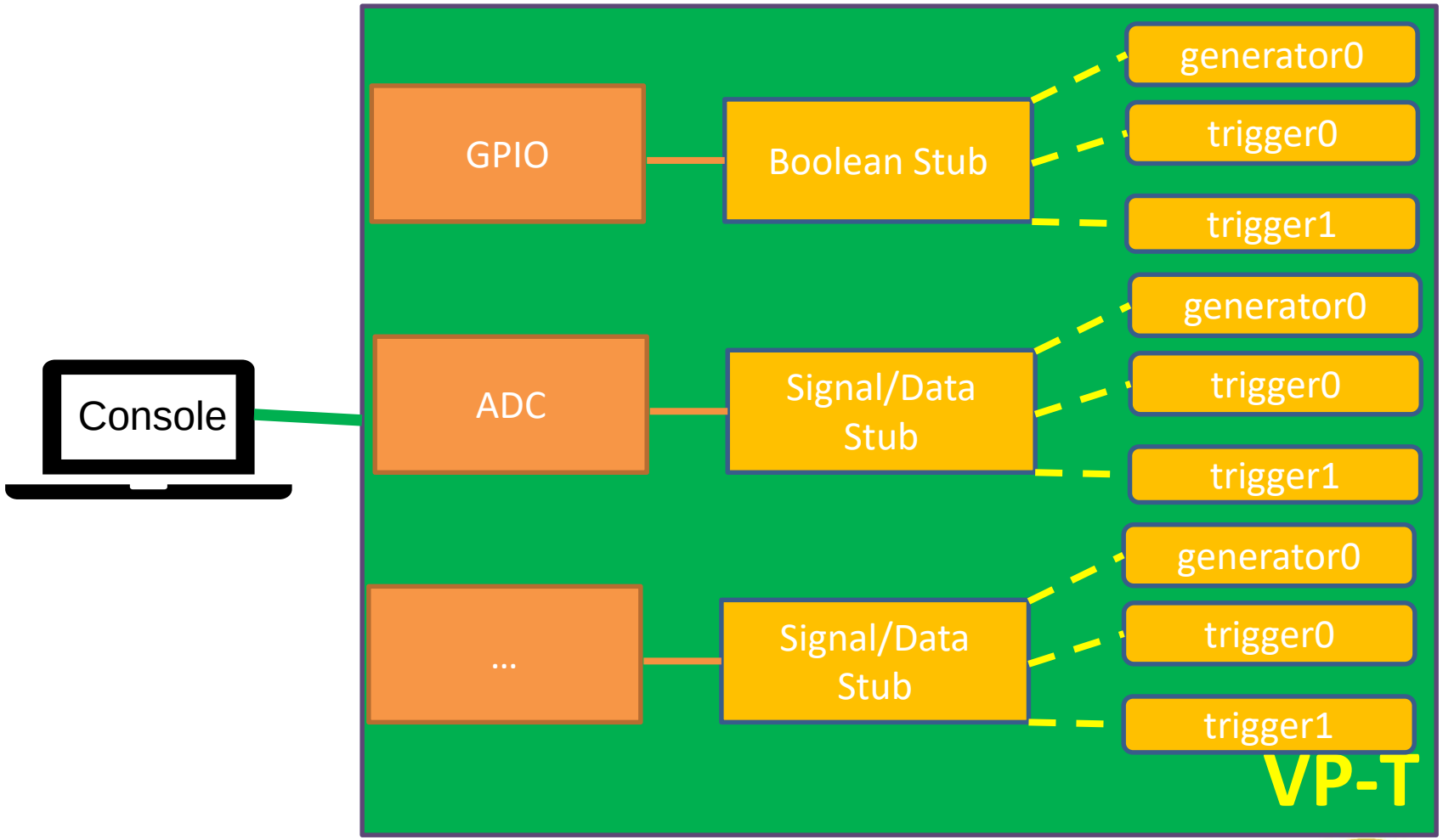
Virtual Platform of the Product (VP-P)

- QEMU model CPUs
- SystemC model peripherals
- QEMU + SystemC Handshake
- Some Models can communicate to the real-world (ethernets,UARTs)



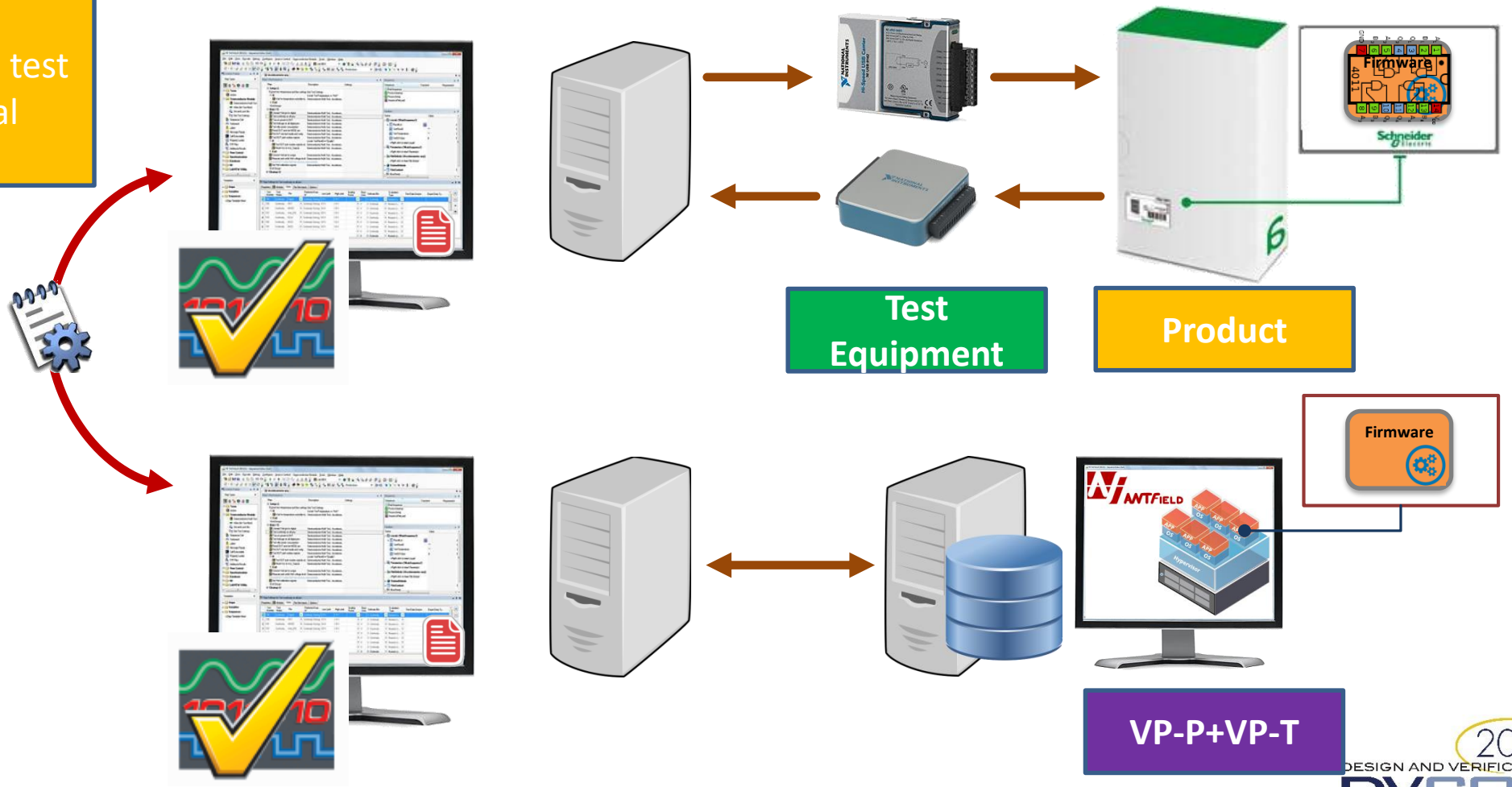
Virtual Platform of the Testbench (VP-T)

- Generates signals on models
- Triggered through JSON Command Line
- Accessible with TCP



Demonstrator to prove the concept

Real-World
TestStand sends test sequences and command test equipments on the real product



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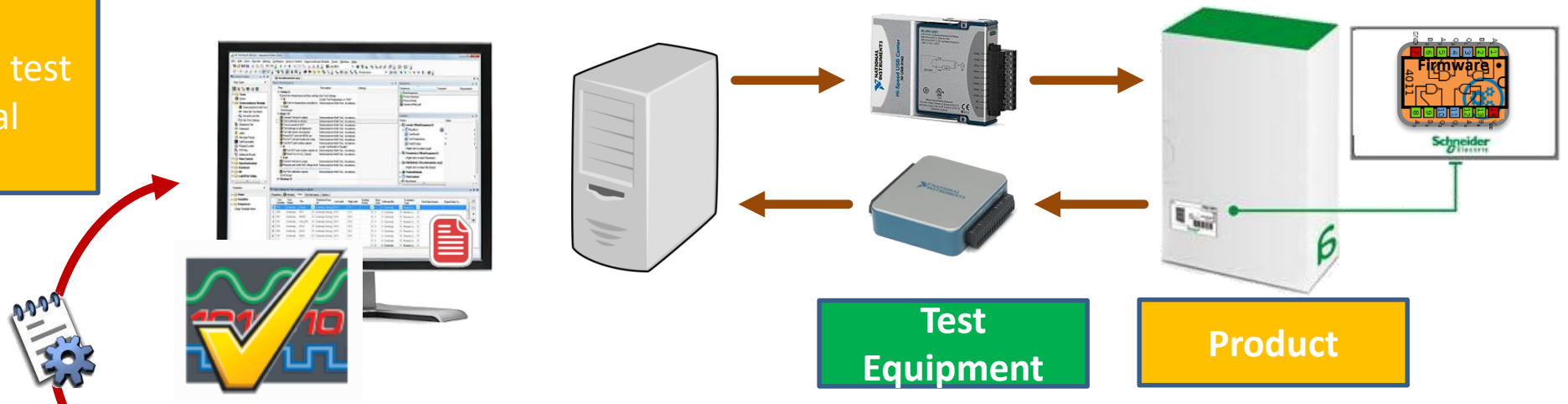
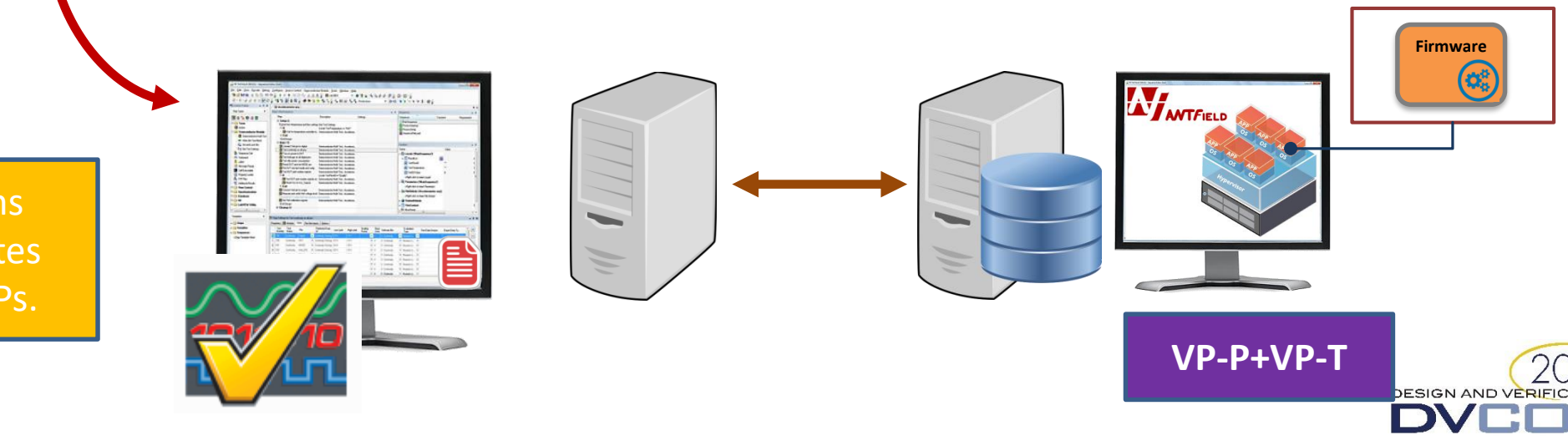


Using Virtual Platforms
TestStand Communicates with a remote PC w/VPs.

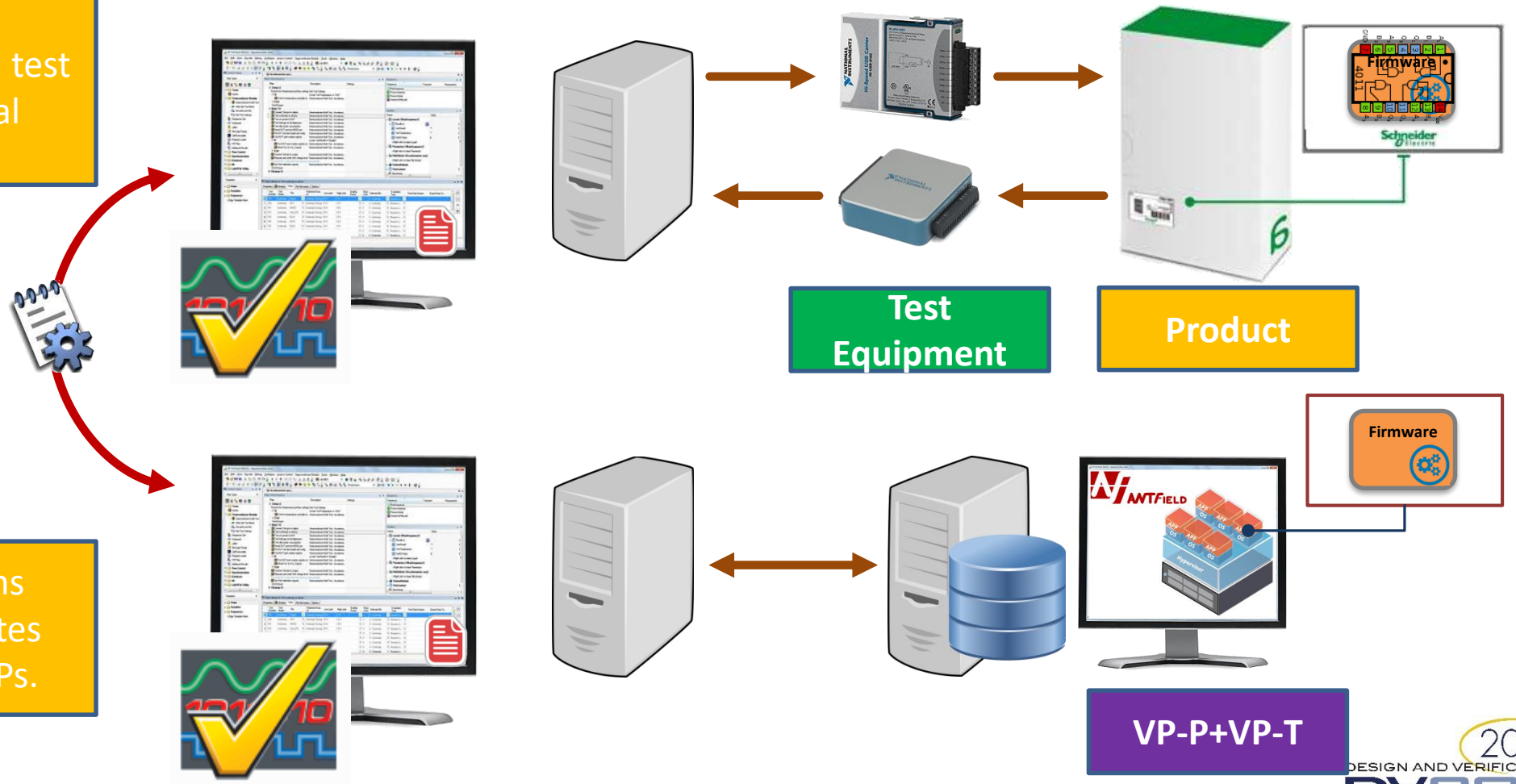


Demonstrator to prove the concept

Real-World
TestStand sends test sequences and command test equipments on the real product

Config change to switch between the two configs

Using Virtual Platforms
TestStand Communicates with a remote PC w/VPs.



Results

- Engineering Optimized on a 6 months project
  - 1 month gain for software bugs tracked in advance (VP-P gain)
  - 2 month gain for test sequences preparation (VP-T gain)

- Bonus : Same advantages as classical VP-P approach but **with virtual verification included** :
  - Reusability
  - Verbosity
  - No risk for human
  - Unlimited instantiation of VPs (**10k€ - 70k€ of hw for testbench dupplication**)

Limitations

- SystemC-TLM LT models ⇔ Timing Inaccurate ⇔ Limited to **functional** product verification.

- Tests limited to firmware functions of the product (no mechanics, hydraulic tests)

Questions

Finalize slide set with questions slide