2023 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE 10 YEAR ANNIVERSARY

Accelerating Complex System Simulation using Parallel SystemC and FPGAs

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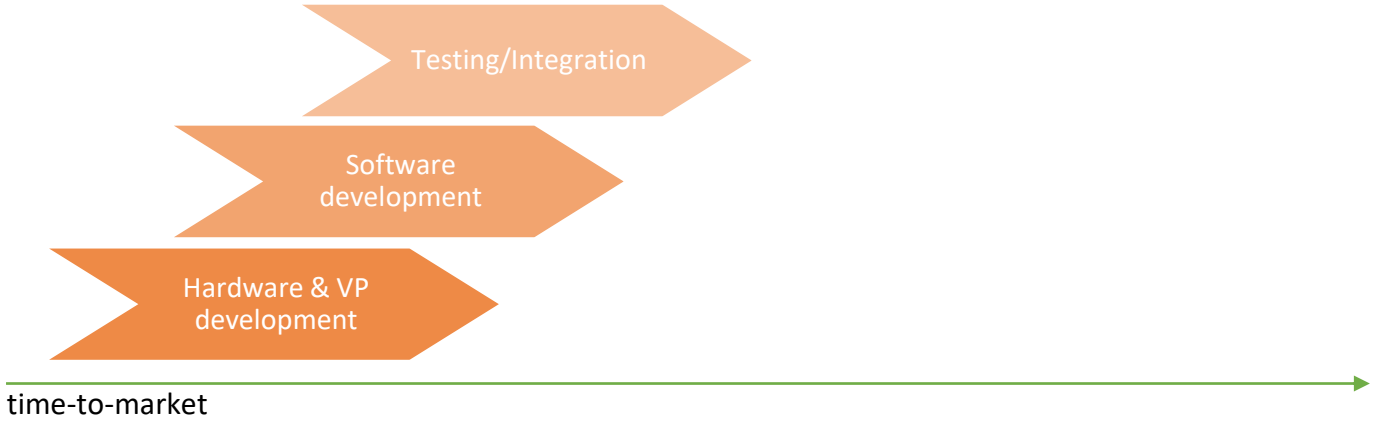
Classical SoC Development

- **Sequential workflow**
- **Late firmware integration**
- **Late issue discovery**
- **Protracted timelines**

The Shift-Left Concept

- **Virtual Prototypes (VPs)**
  - Very early availability
  - Powerful debugging tools
  - No resource limitations
- **Physical Prototypes (FPGAs)**
  - Real hardware interaction
  - Very fast simulation
  - Accurate timing



Limitations

- Virtual Prototype:
  - Single-threaded SystemC bottlenecks complex systems
  - Model accuracy with respect to Hardware
  - Simulation Trade-off: Speed vs. Accuracy
- Physical Prototype:
  - FPGA simulation requires complete synthesizable RTL

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RAVEN as a solution

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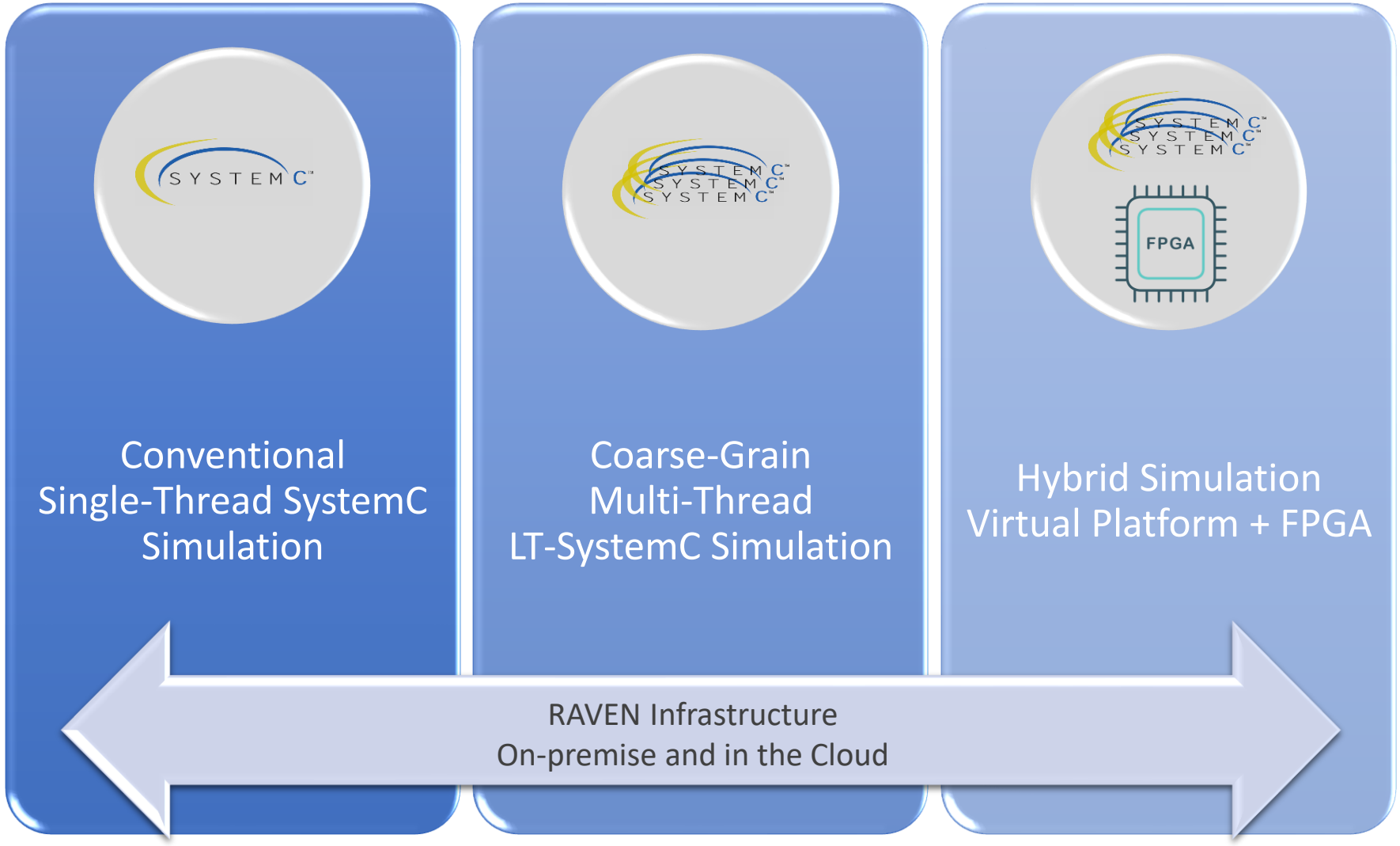
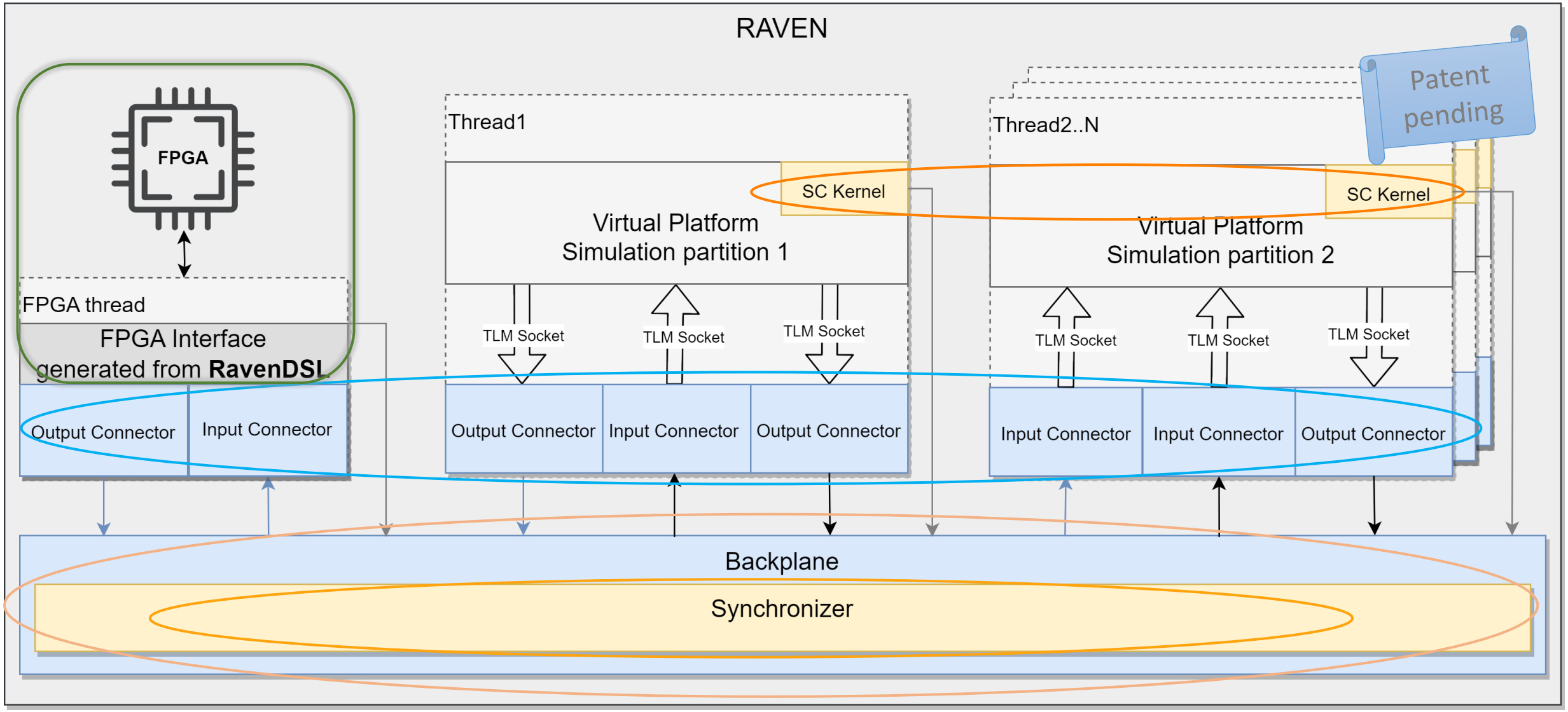

SYSTEMC
SYSTEMC
SYSTEMC
SYSTEMC
SYSTEMC
SYSTEMC
FPGA
Conventional
Single-Thread SystemC
Simulation
Coarse-Grain
Multi-Thread
LT-SystemC Simulation
Hybrid Simulation
Virtual Platform + FPGA
RAVEN Infrastructure
On-premise and in the Cloud


RAVEN
Patent pending
FPGA
FPGA thread
FPGA Interface generated from RavenDSL
Output Connector
Input Connector
Thread1
Virtual Platform Simulation partition 1
SC Kernel
TLM Socket
TLM Socket
TLM Socket
Output Connector
Input Connector
Output Connector
Thread2..N
Virtual Platform Simulation partition 2
SC Kernel
TLM Socket
TLM Socket
TLM Socket
Input Connector
Input Connector
Output Connector
Backplane
Synchronizer

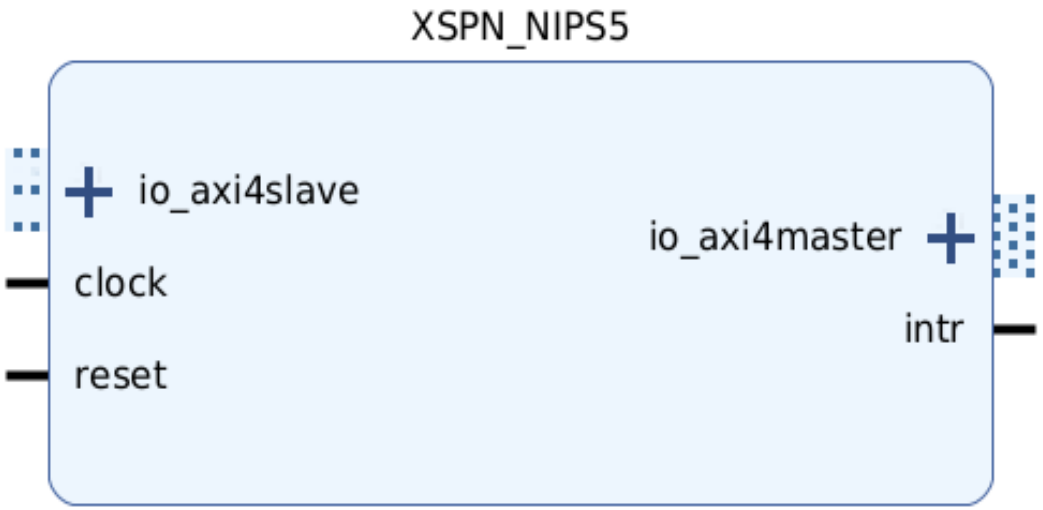
DUT integration process

- Step 1: Analyze Design to determine partition boundaries.
  - Minimal interactions between partitions to prevent bottlenecks.
  - Consider computational load within partitions for meaningful parallelization.
- Step 2: Partition the Design
  - Divide the design into partitions.
  - Connect open connections to RAVEN interthread connectors.
- Step 3: FPGA Integration
  - Generate wrapper for data exchange and synchronization.

Automation with RavenDSL

- Automating the Integration
  - RavenDSL to automate the integration process.
  - Reducing manual effort and minimizing errors.
- RavenDSL
  - Describes RTL interfaces and signal transitions.
- RavenDSL Compiler
  - Tool-flow automatically creates hardware and software components.
  - TaPaSCo Framework for FPGA bitstream generation.
  - Optionally adjust FPGA synthesis.

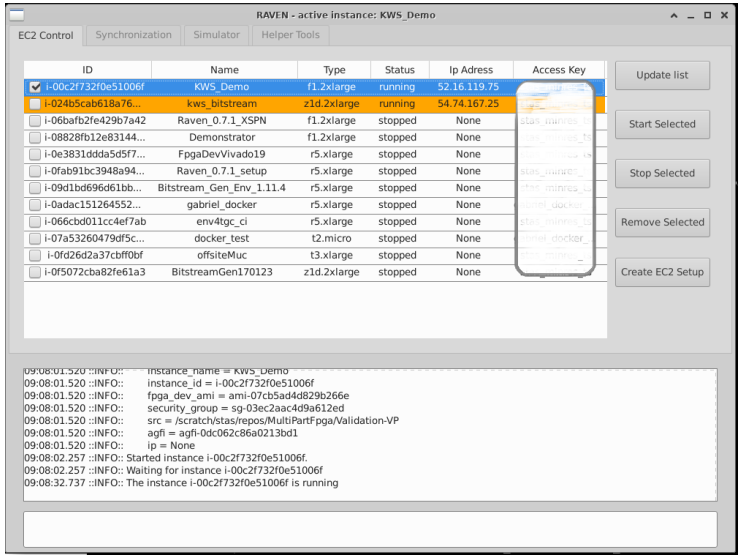
RavenDSL example




```
1  dut XSPN_NIPS5;
2      clocks {
3          Clock#(100 MHz) clock;
4      }
5      resets {
6          ResetAgent#()(ACTIVE_HIGH) reset;
7      }
8      AXI4LiteSlaveAgent#(32,32) io_axi4slave;
9      AXI4MasterAgent#(32,512,1,0) io_axi4master;
10     InterruptAgent#() intr;
11 }
```

Scalability

- Challenge:
  - High upfront costs for FPGA resource availability.
  - Waiting times for FPGA slots.
- RAVEN's Solution:
  - Cloud-Ready Infrastructure.
  - No upfront investments in FPGAs.
  - No Waiting Times.
  - GUI for user-friendly cloud usage.
  - Flexibility: scale resources as needed.



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RAVEN Simulation Performance

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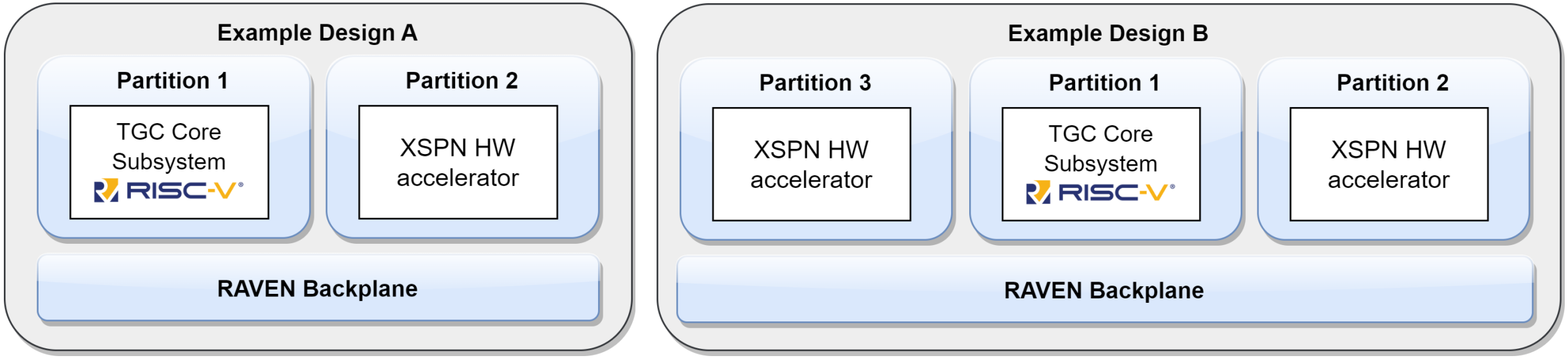
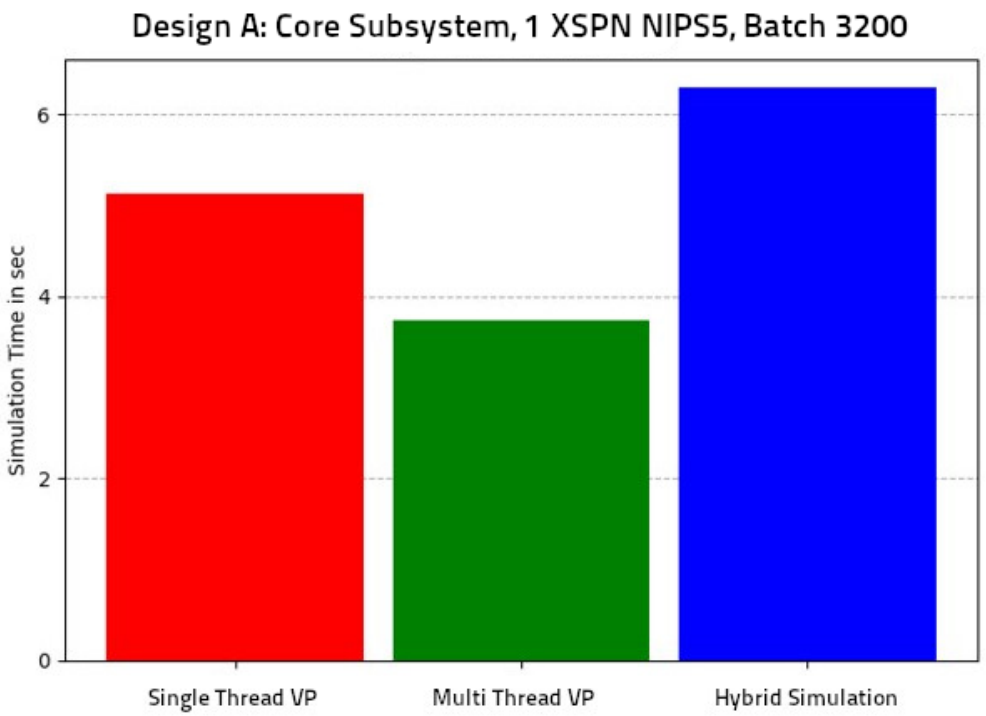
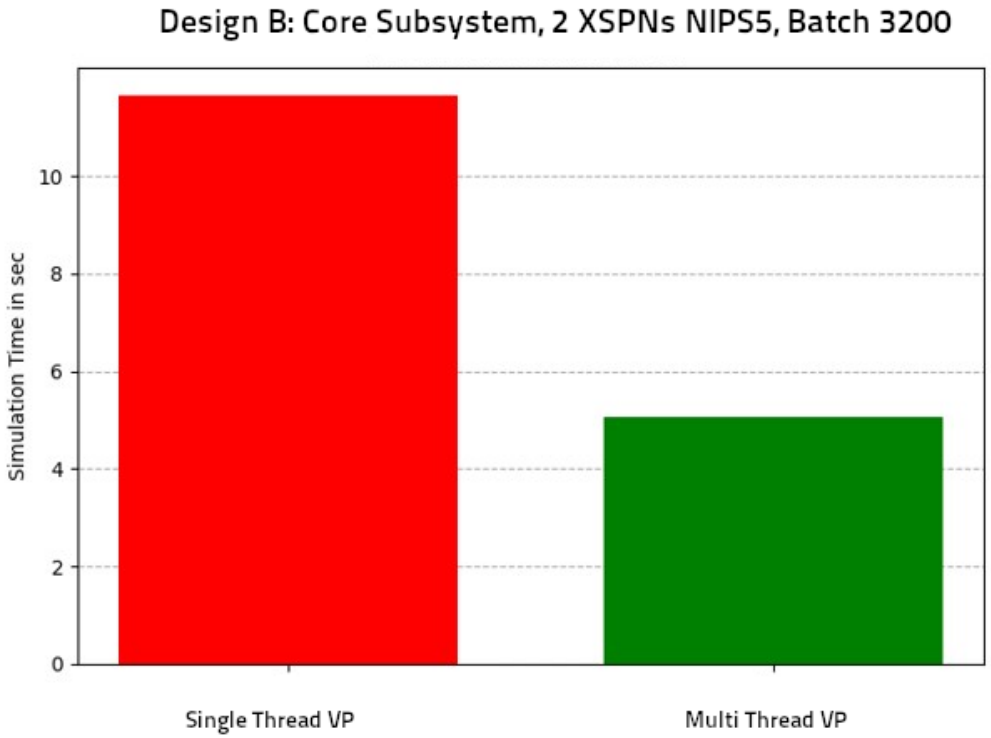


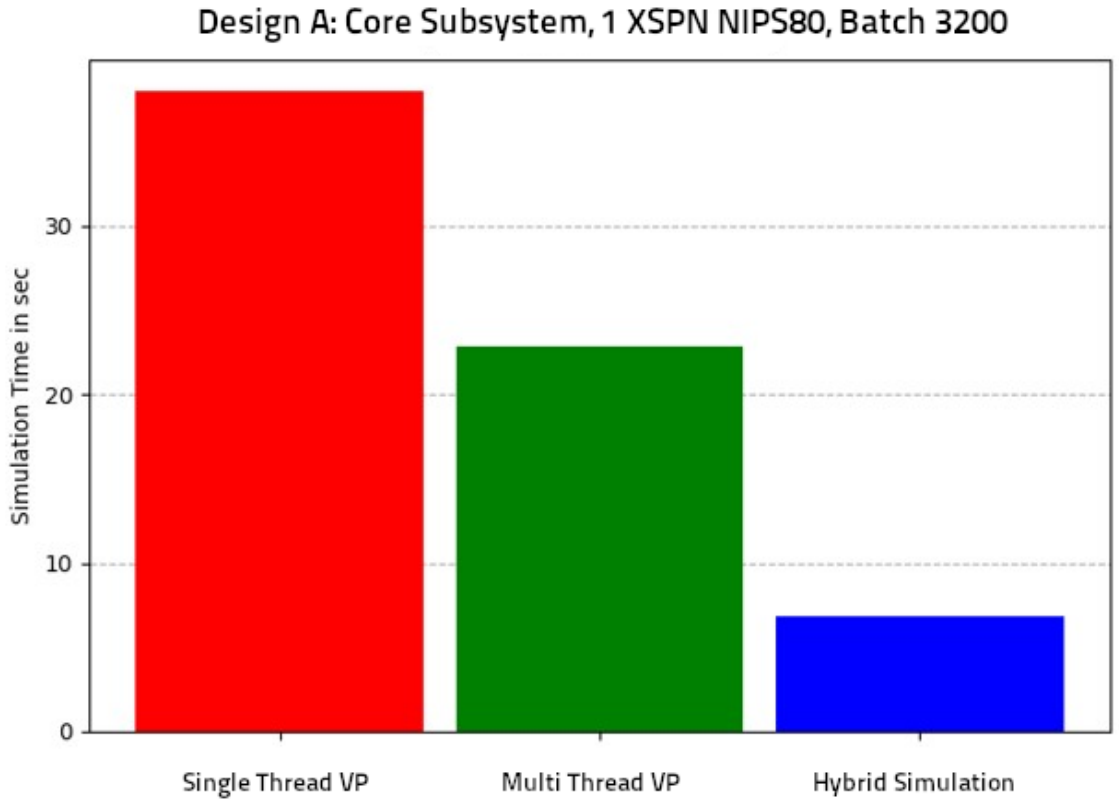
	NIPS5			NIPS80			Available
	DUT	RAVEN	Total	DUT	RAVEN	Total	
LUT	17k	25k	167k (12.8%)	99k	25k	250k (19.2%)	1304k
Register	7.7k	24k	214k (8.19%)	159k	24k	361k (13.9%)	2607k
CLB	3.3k	6.0k	36k (21.8%)	20k	4.3k	52k (31.8%)	163k
BRAM	11	103	222 (11.0%)	71	103	282 (14.0%)	2016
DSP	23	0	26 (0.25%)	736	0	739 (8.16%)	9024

RAVEN performance analysis



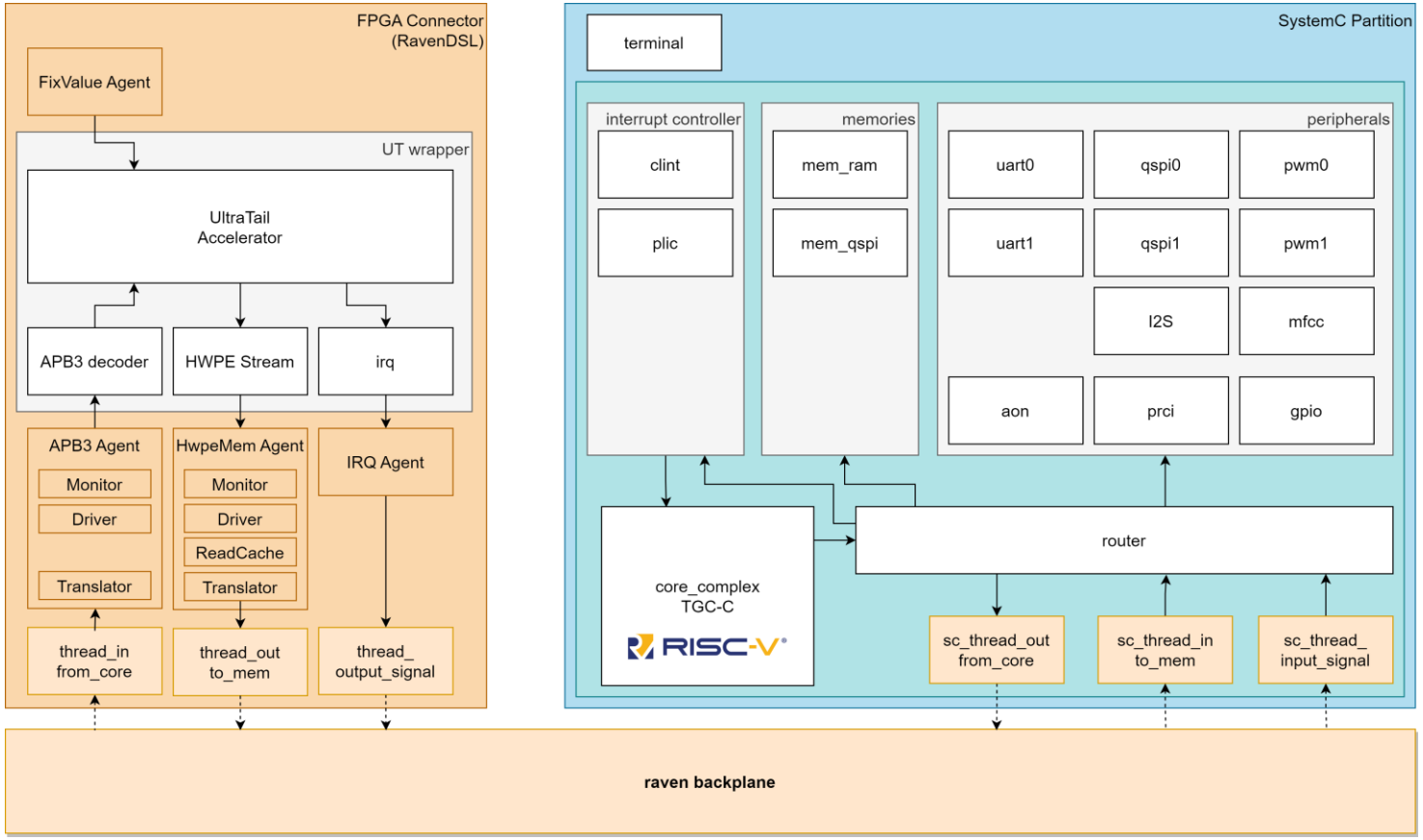


RAVEN performance analysis



Showcase Setup: Keyword Spotting System

- Audio Data Pre-processing: Performed in Virtual Prototype
- HW ML Accelerator on FPGA
- Live Demonstration at Our Booth



Conclusion

- Easy parallel and hybrid simulation
  - Simple partitioning
  - Automated RTL wrapper generation
- Low entry barrier for hybrid simulation
- Highly flexible and scalable through unified use of on-premise and Cloud resources
- Significant Speed Gains for large Virtual Prototypes as well as Complex HW Blocks

RAVEN

Questions