2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

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Absolute GLS Verification

An Early Simulation of Design Timing Constraints

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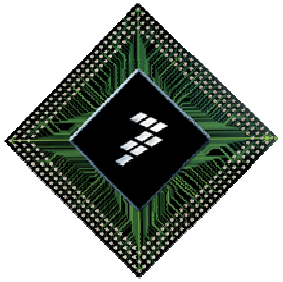
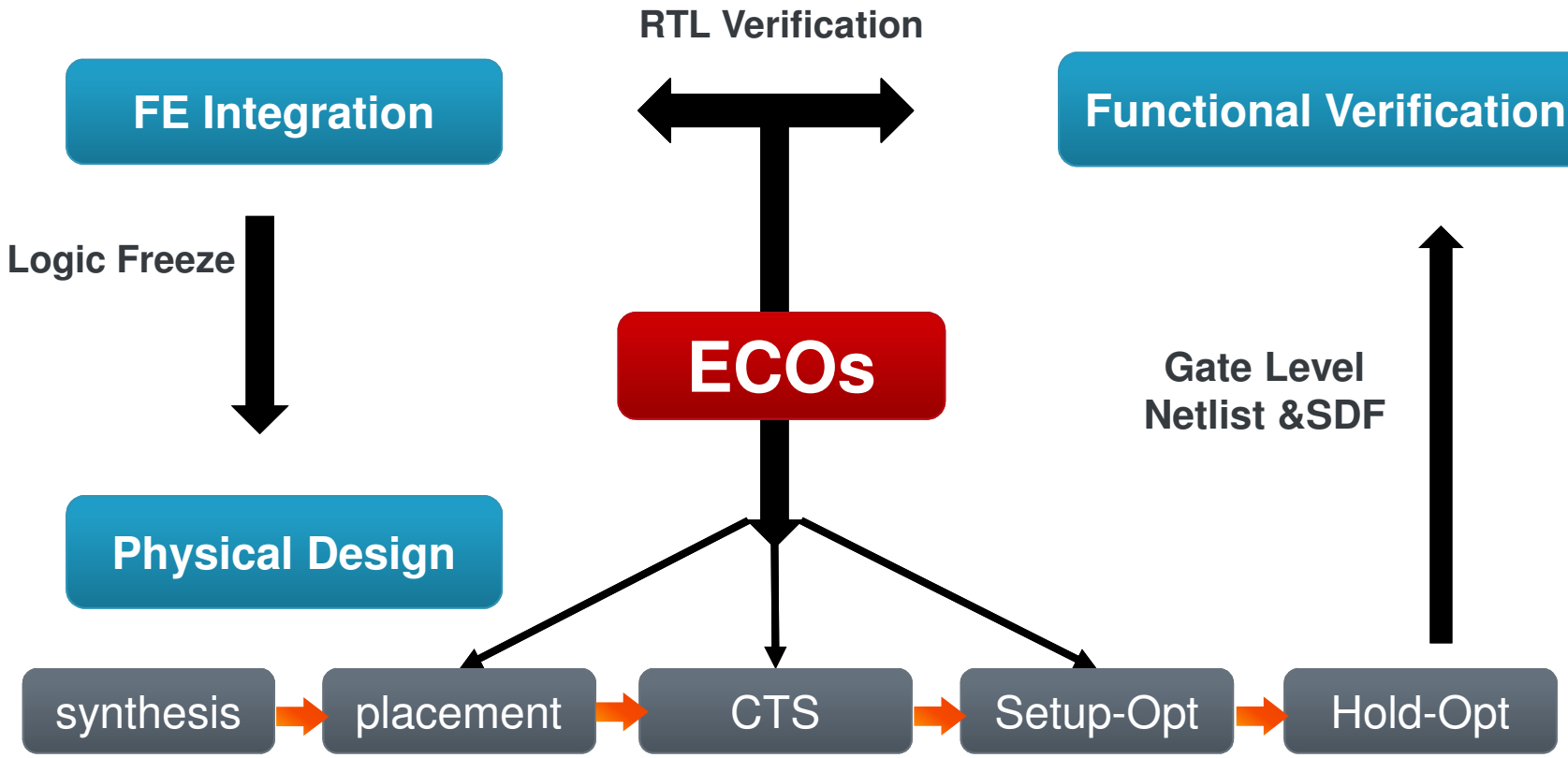


Agenda

- Basics Design Flow [FE-Verif-PD-Verif-FE-PD-Signoff]
- Motivation
- Defining the right scope
- Basics of Design Timing
- How current GLS verification is not absolute.
- Absolute GLS Verification
- Default Delays Modeling
- Different Aspects of Constraint Modeling
- SDF Generation Algorithm
- The new Design Flow
- Future Scope
- Results and Conclusion

Basic Design Flow and Challenge



Dependencies on skew matched clock delays..

Close to ~ 6 weeks turnaround time to provide SDF !!

REALLY ??

Are we doing robust gate level verification ?

Our Motivation

Close to ~ 6 weeks turnaround time !!

Are we doing robust gate level verification ?

Challenges Or …Opportunities ..!!

Early enablement

Adding Robustness

Defining the right scope…

Static Timing Analysis

Static Analysis

- Timing Signoff Across all Process Voltage and Temperature range
- Correct design constraints for all possible Functional/DFT modes

Gate Level Verification

Dynamic Analysis

- To model the delay dependencies on Verification Code
- Missing Synchronizers
- Glitches
- Verifying the above applied timing constraints
- Correct design constraints for all possible Functional/DFT modes

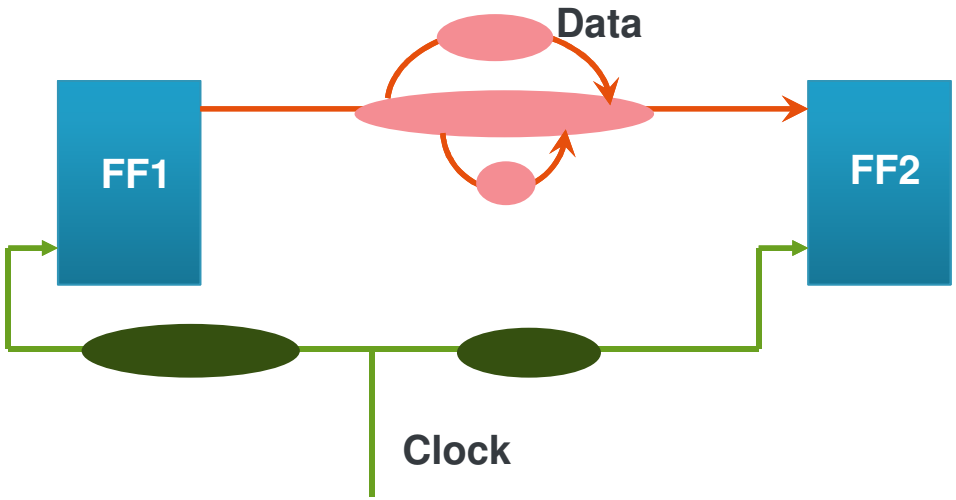
The Design will run at required performance of 200 MHz or 190 MHz, is to be answered by STA Analysis; Needs no Verification.

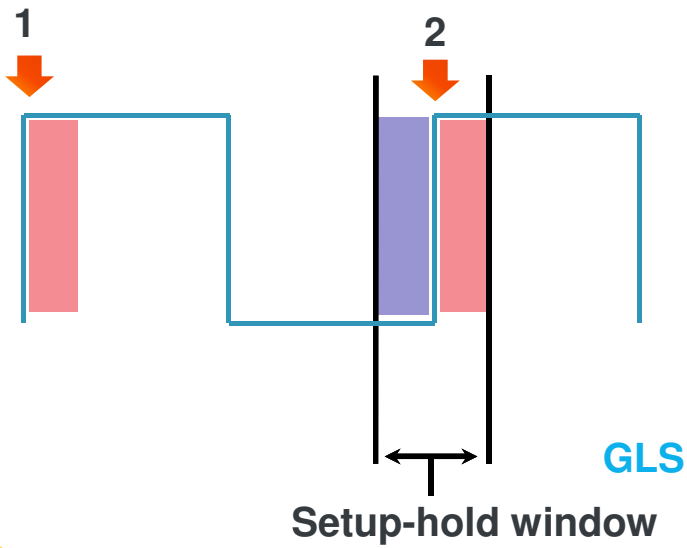
Design Timing Basics

Timing Checks

- ✓ Setup Timing
- ✓ Hold Timing
- ✓ Other Race Condition (data to data check)

- ➢ Early/Late Modeling
- ➢ Technology Derates





Timing Constraints

To be Verified

- ❖ Multi-Cycle Paths
- ❖ False Paths
- ❖ Asynchronous Clocks

GLS Tool generates "X" if data comes in setup/hold window

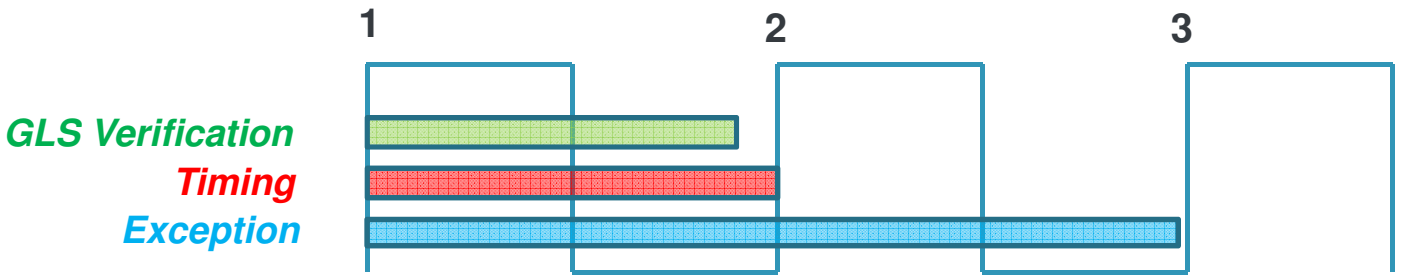
Why current GLS verification is not absolute ?

Scenario 1

Single Analysis Mode Timing SDF

There could be no timing violation in single mode, but there is in actual and being missed in Signoff condition.

Timing is still not met, and will cause Yield Drop.



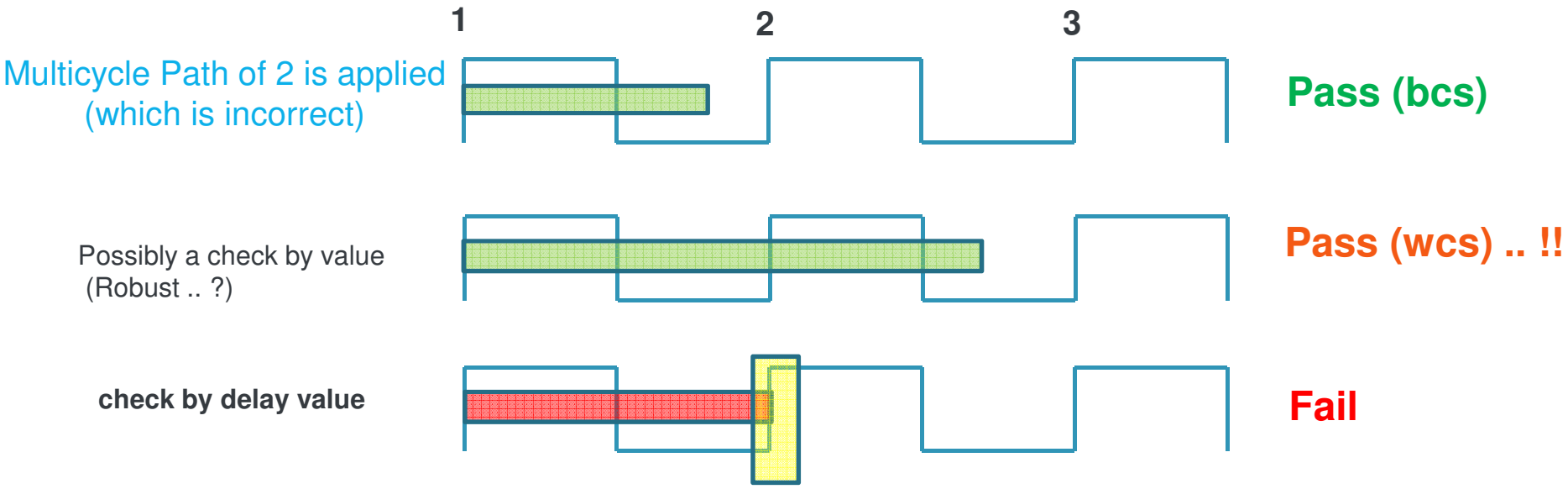
Multicycle Path of 2 is applied
(which is incorrect)

Why current GLS verification is not absolute ?

Scenario 2

Dependency on Functional Pattern

It doesn't fail unless total delay is lying in setup/hold window of capturing flop.



ABSOLUTE GLS VERIFICATION

Early Simulation of Design Timing Constraints

Self Simulating Environment

Delays are modeled to make GLS fail if timing constraints are wrong !!

A. False Path (through static pins), let cell delays delayed **by huge number**.

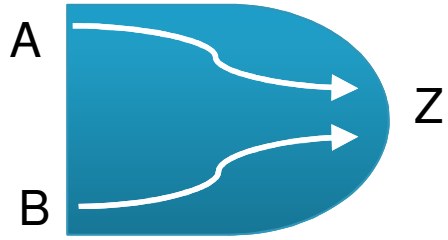
B. Clocks are assumed asynchronous, **let them have varied latencies**.

C. Multicycle Path, let total data delay just meet **the first edge** of capture flop.

Simulated SDF

Modelling the default delays

Data Cell delay



Two Attribute of a cell delay

- Delay
- Functional Arc definition

Default data delays are modeled to **Technology Unit Cell Delay.**

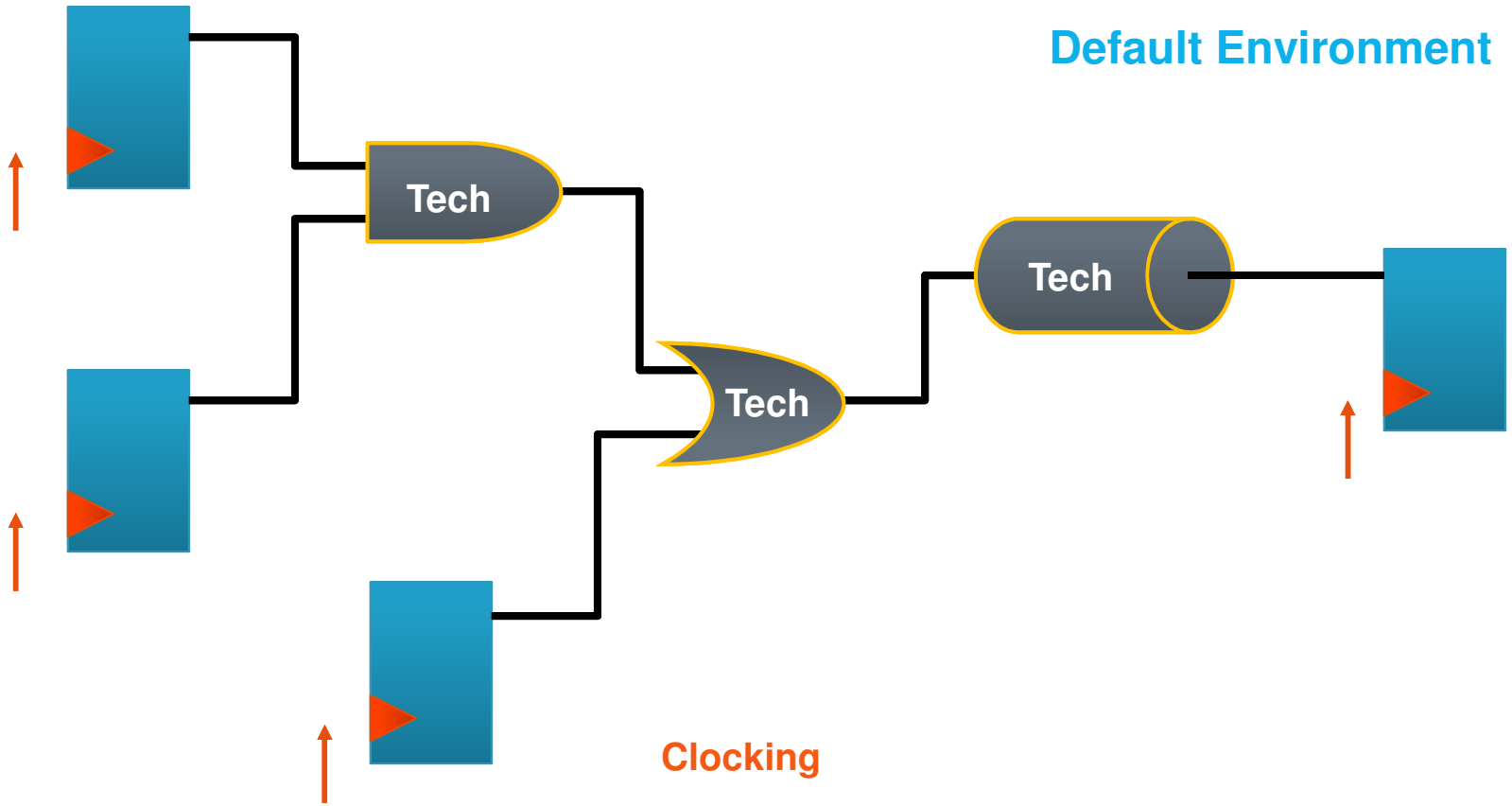
(For e.g. for C55, it is 110psec)

Clock Cell delay

ZERO !!

Making all the clock edges to arrive at the same time at all the sinks.

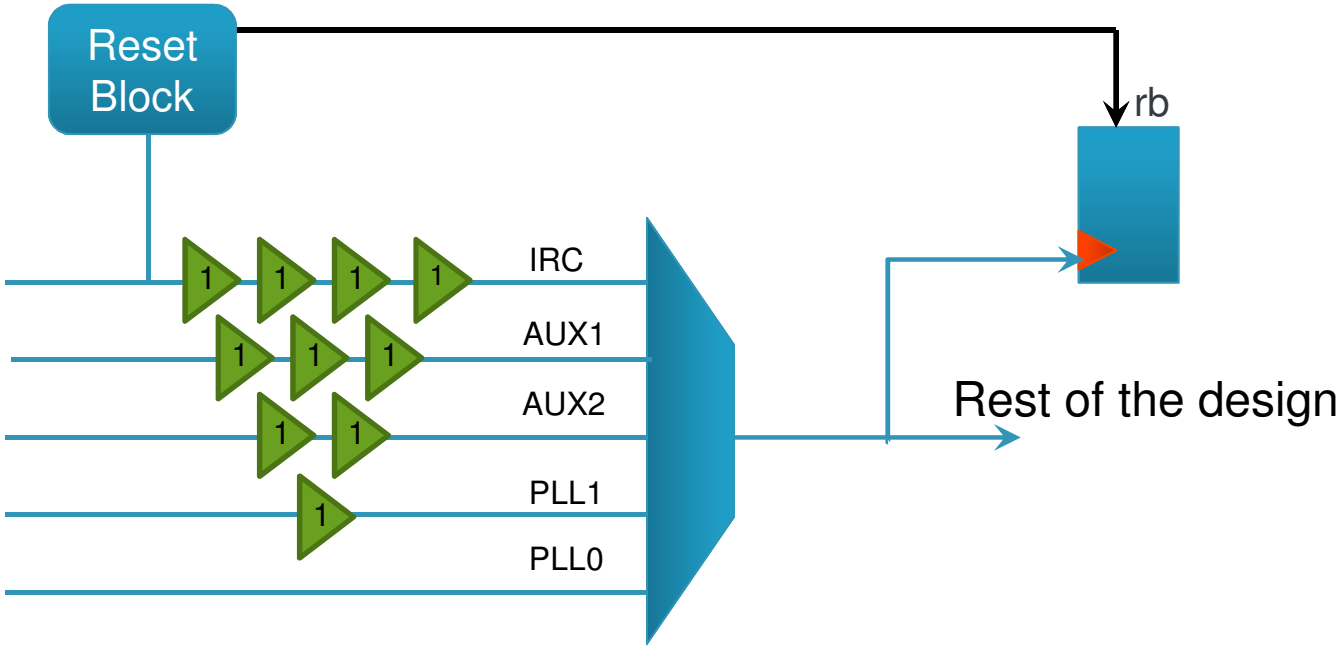
Default Design Timing and Logic Function



Asynchronous Clock Constraints Modelling

Missing Synchronizers in Reset Domain Crossing.

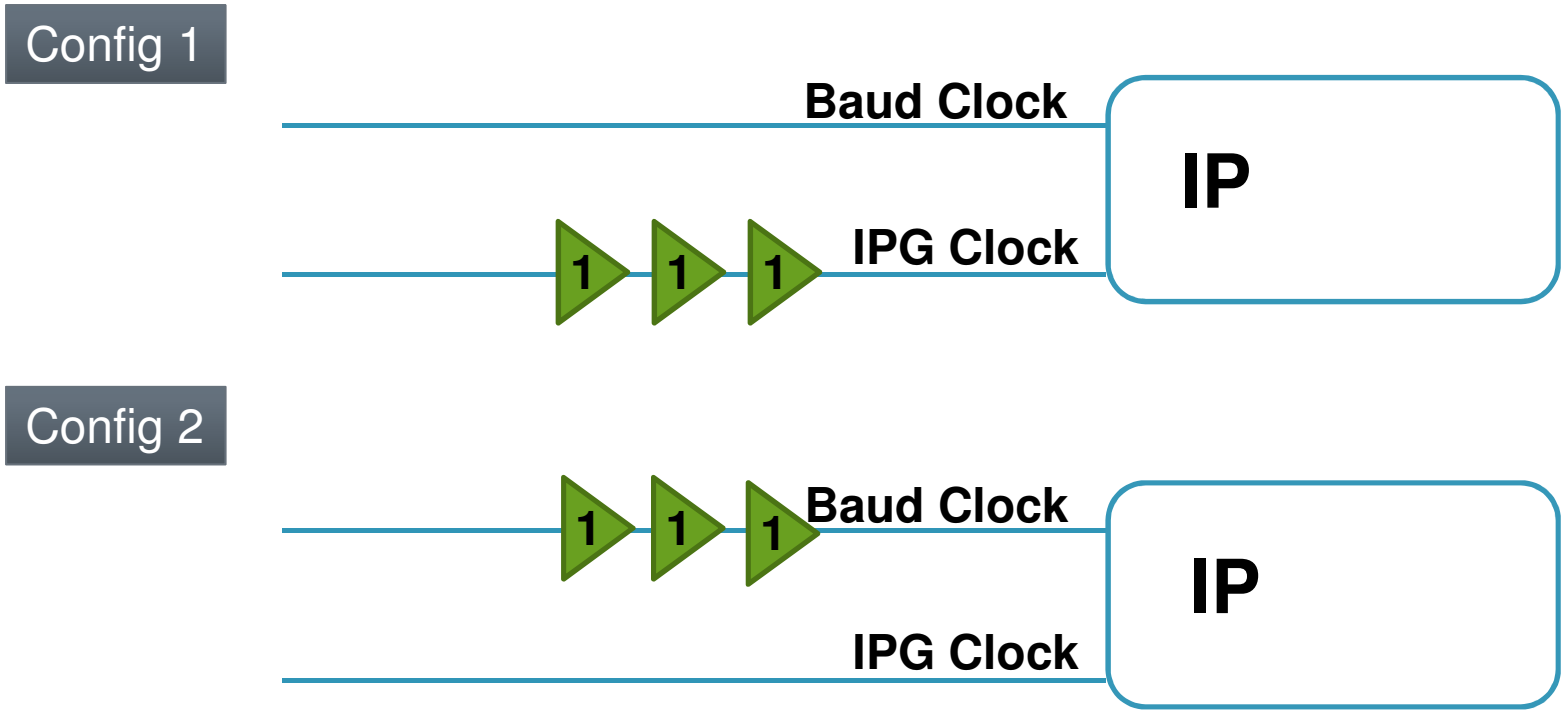
GLS will certainly fail if this asynchronous system FAILS, Due to HOLD Violation.



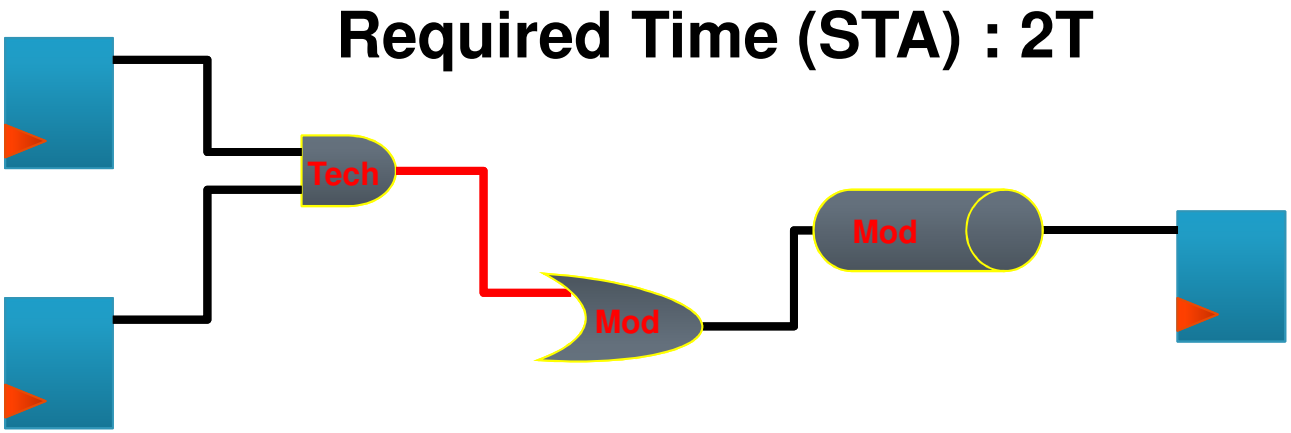
Technology annotated buffer delay 1

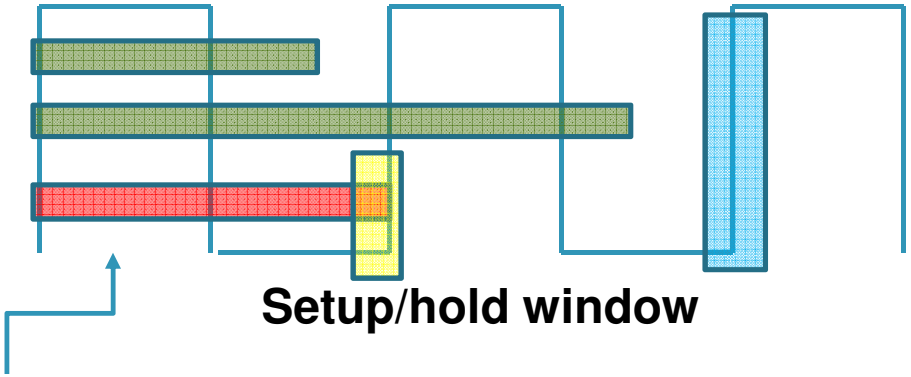
IP Async clock bug

GLS will certainly fail if this asynchronous system FAILS, Due to HOLD Violation.



Multi Cycle Path Modelling





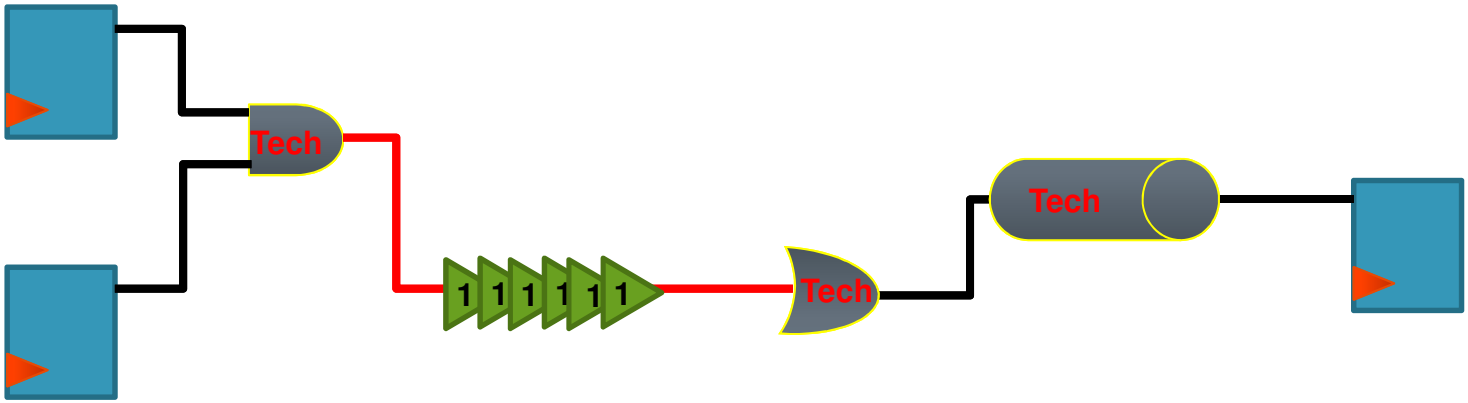
Absolute Fail or PASS

Pass if it's a 2 cycle path

Fail if it's a single cycle path

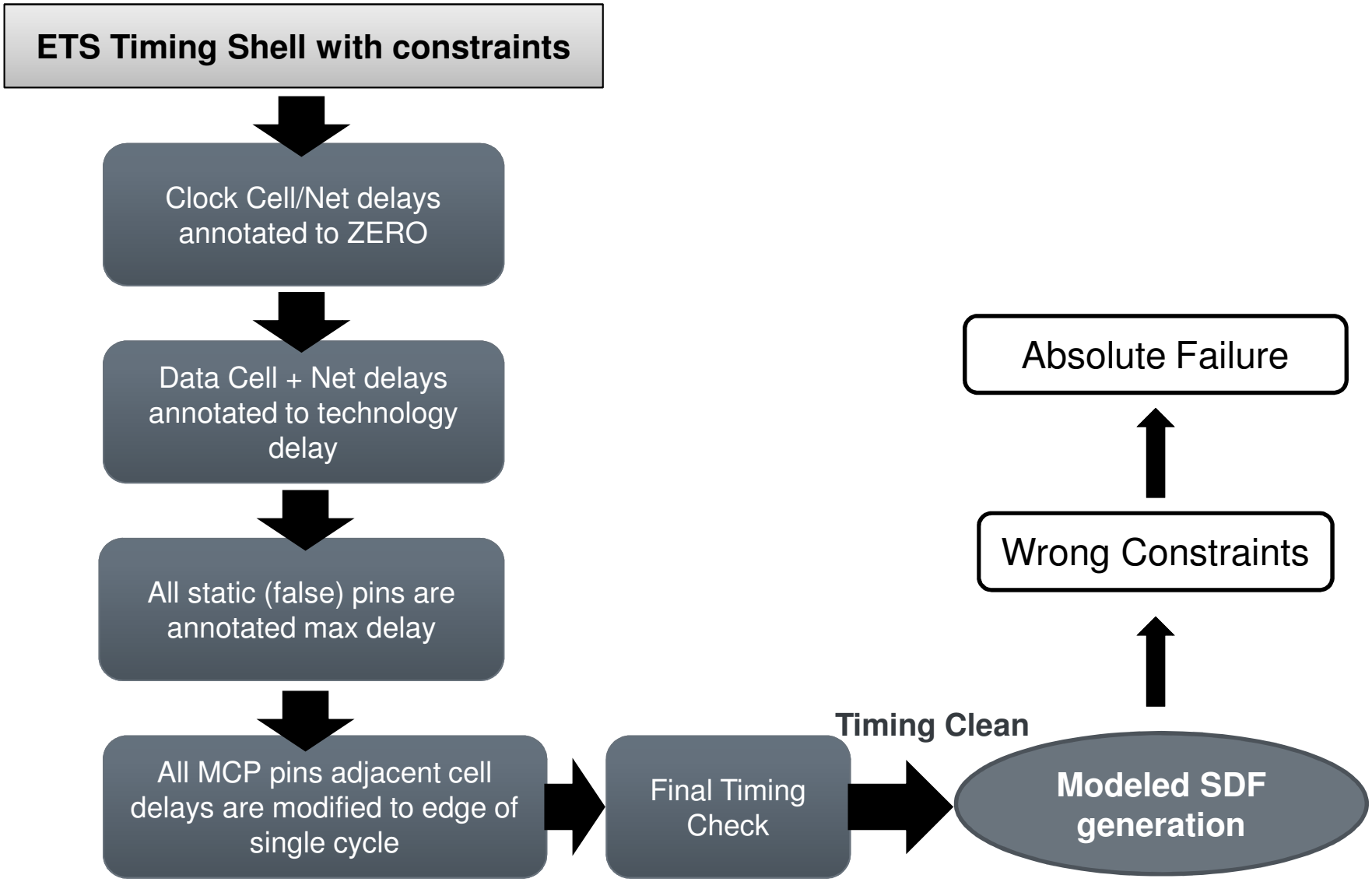
Individual Buffer Delay in the fanin/fanout cone are adjusted to make path lie exactly in 1 Time period

False through below RED Signal

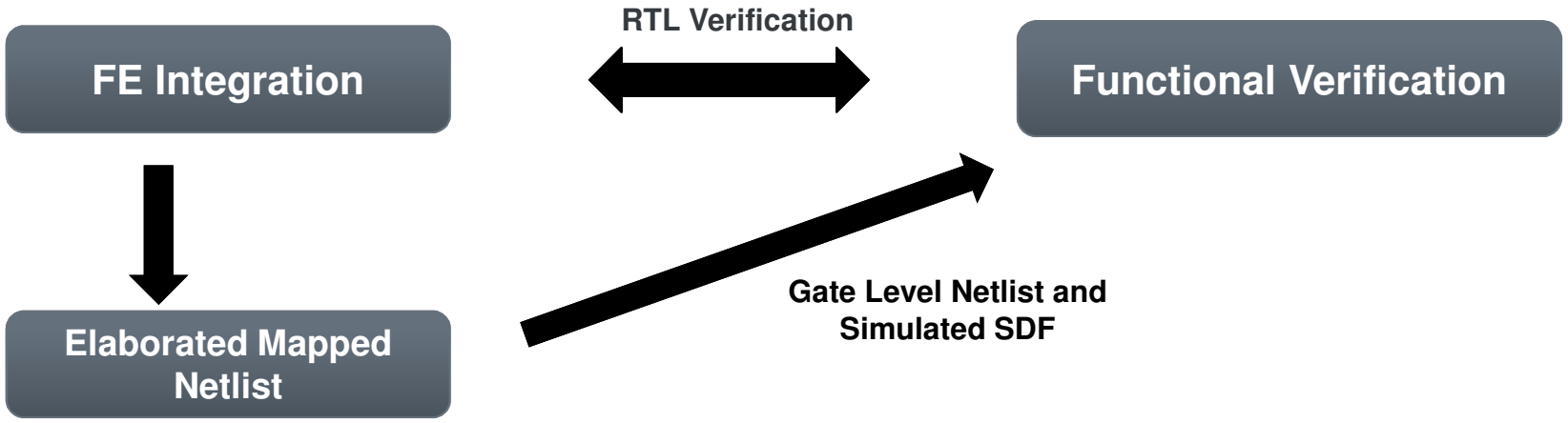


False to the frequency limit – Signal is buffered upto the lowest working frequency

Absolute GLS SDF Generation



The New Design Flow



Even further early look ahead .. ??

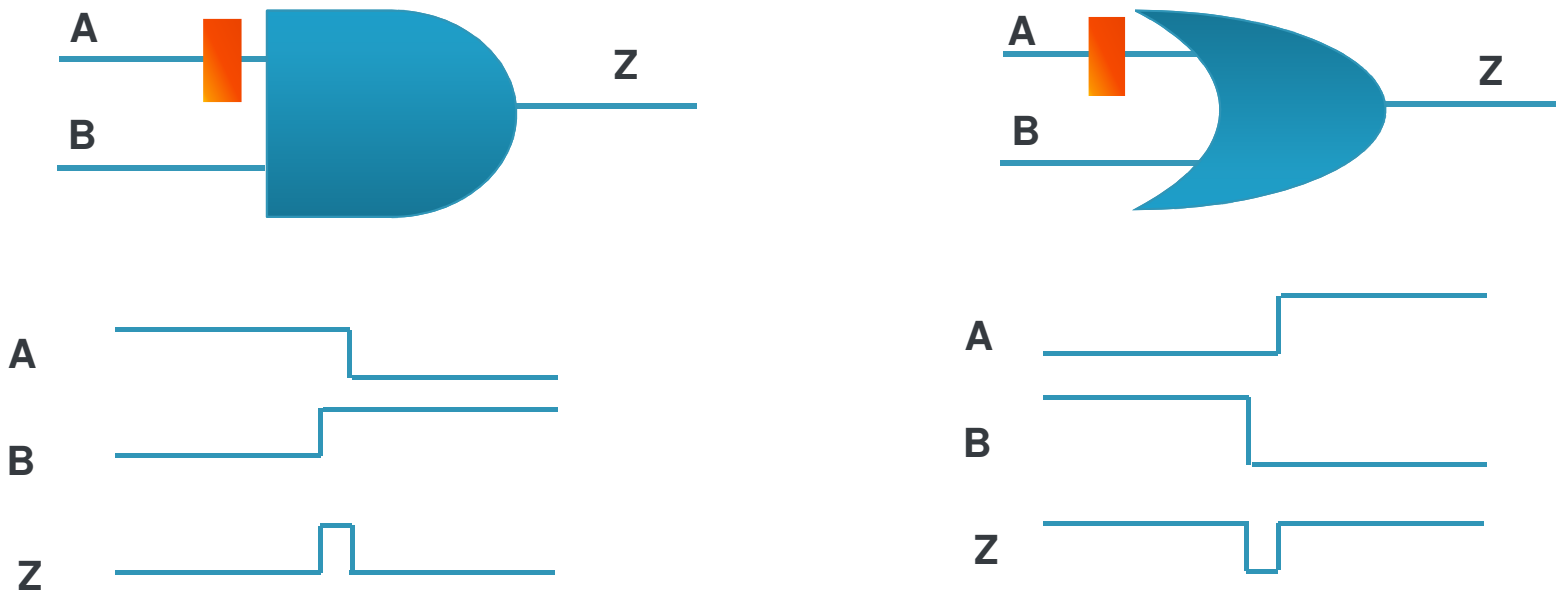
How about Gate level verification at IP level itself ??

IP level verification dominates the SOC verification for internal functionality (due to its diverse scope)

POSSIBLE .. !!

Clock Glitch Modelling

Future Road Map (Under exploration…)



AND and OR Type gating usually get gating setup/hold check.

What about other clocking cells ?

Glitch modelling will be done only for clock logic and the un-timed signals (SE, Reset)

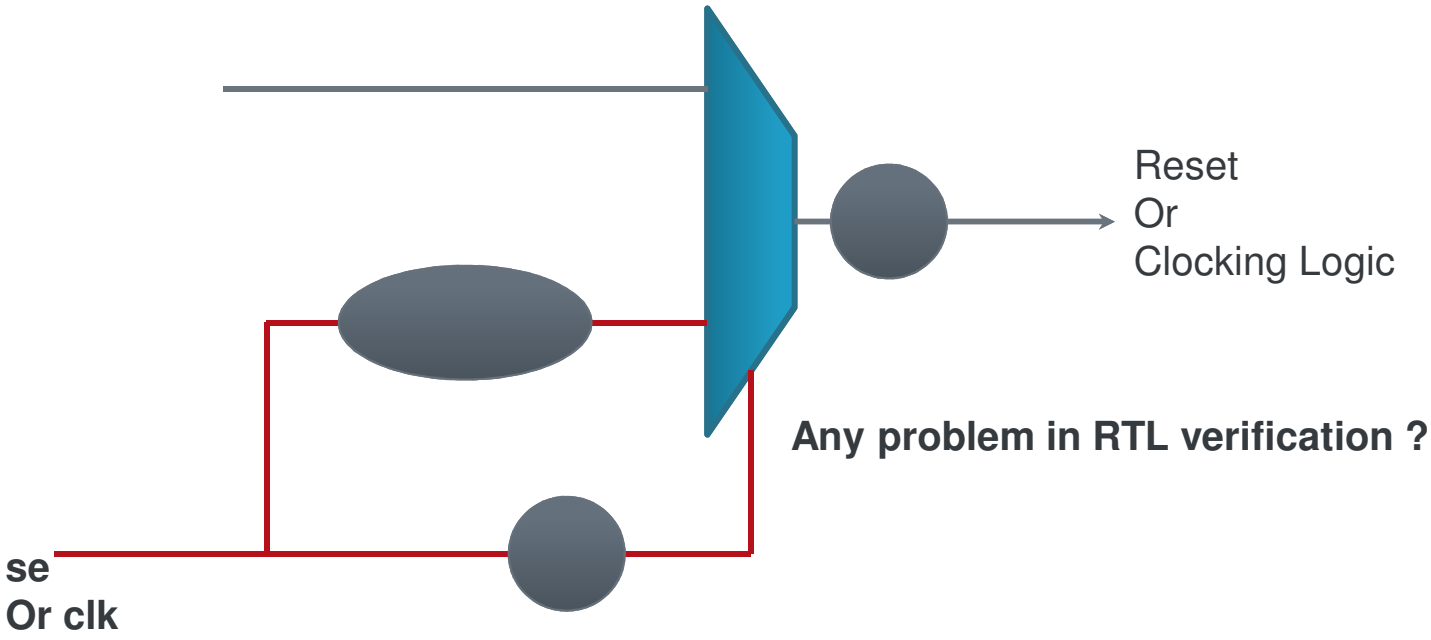
Data Glitch is anyways ensured by delay glitch signoff done later in STA the design cycle

(To be checked for glitch problems and efficiency)

Clock Glitch Modelling

Future Road Map (Under exploration…)

Re-convergent Path Glitch Modeling



Different re-convergent paths are modeled to different delays

DFT Pattern generation and GLS verification

Future Road Map (Under exploration…)

DFT GLS Pattern verification

Final SDF are modeled to the difference in single timing mode and the signoff timing mode.

Will lead to early debug**, saving tester time.**

Conclusion

- In Past few NPI's GLS was enabled immediately after 1st synthesis run
- We caught 2 bugs in the clock path from the early enabled Absolute GLS verification
- Promising to get more bugs.

Fast and Robust,

The Absolute GLS Verification Flow

It's worthy..!!

Backup Slides

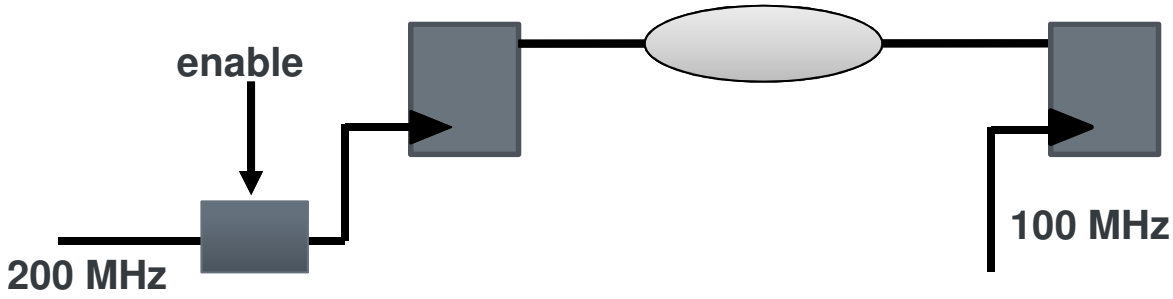


Figure 1(A) Valid Multicycle Path (100MHz) as achieved by enable

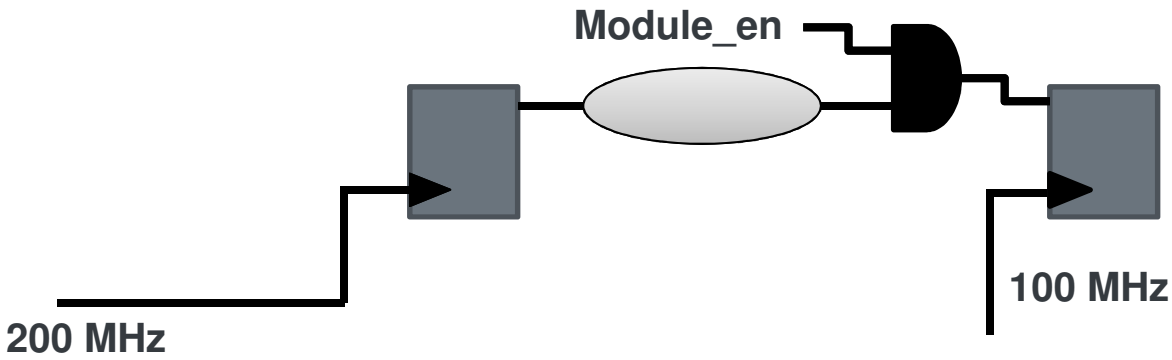


Figure 1(B) Valid Multicycle Path (100MHz) as achieved by data path gating

Backup Slides

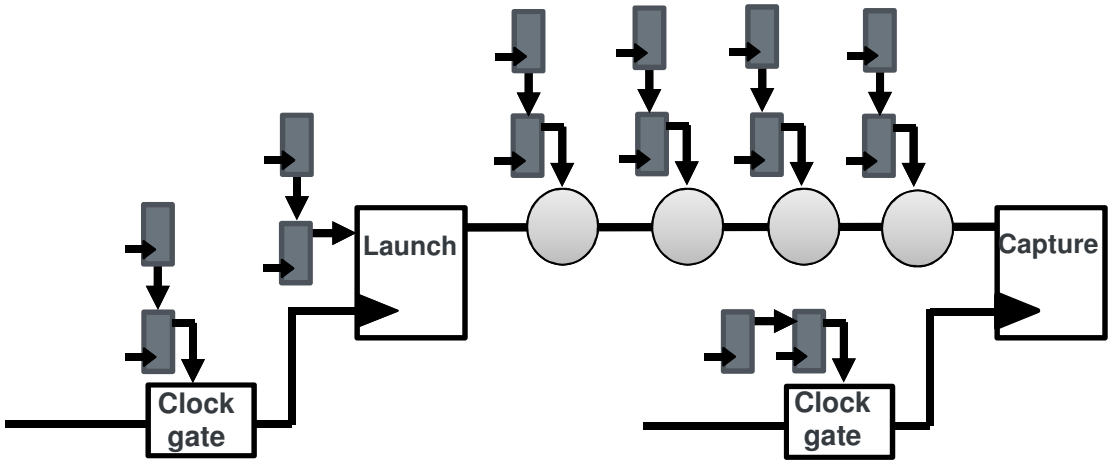
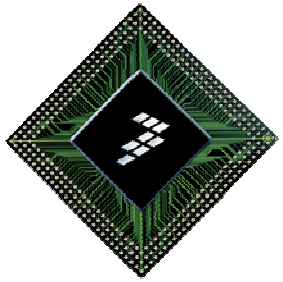


Figure 2 : Possible 2 level of back to back logical check on shaded flops

Q & A



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Thank You

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