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ACT with Confidence: Formal Verification of Packet Based Designs using Array Centric Tracking

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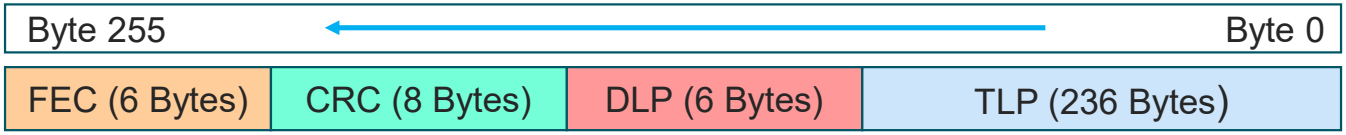
Agenda

- Design Overview
- Traditional FV Data Integrity Techniques
- Problem Statement
- Array Centric Tracking Methodology
- Results
- Applications
- Summary

Design Overview

- FLIT Mode introduced in PCIe 6.0 as a new data stream.

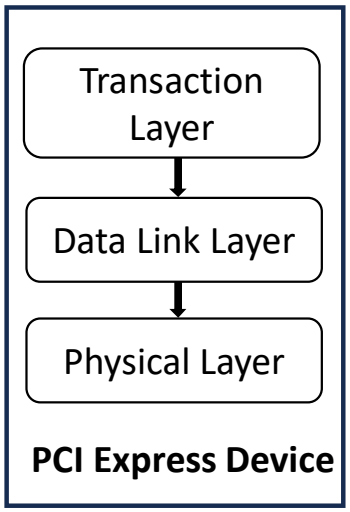


Flit Structure – 256 Bytes (64 DWs)

- TLP length varies from 3 DW's to 1024 DW's
- Flit Encoder packs the 236 TLP Bytes (59 DW's) in Flit.
- Allocates space for DLP, CRC and FEC Bytes (5 DW's)

Control Bus provides the information

- Number of TLPs starting
- Number of TLPs ending
- TLP starting and ending positions
- Nullified, Poisoned TLPs

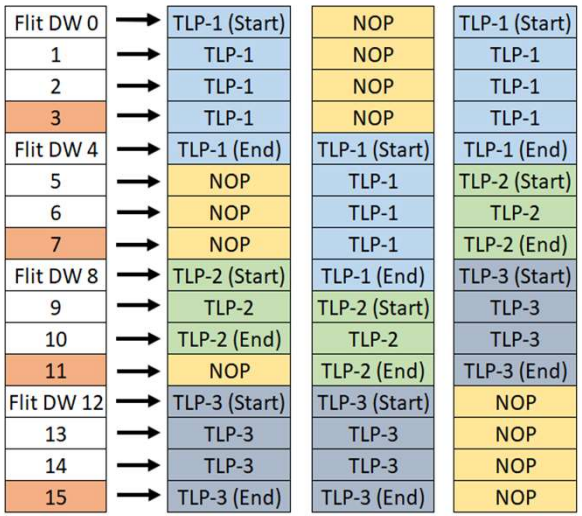


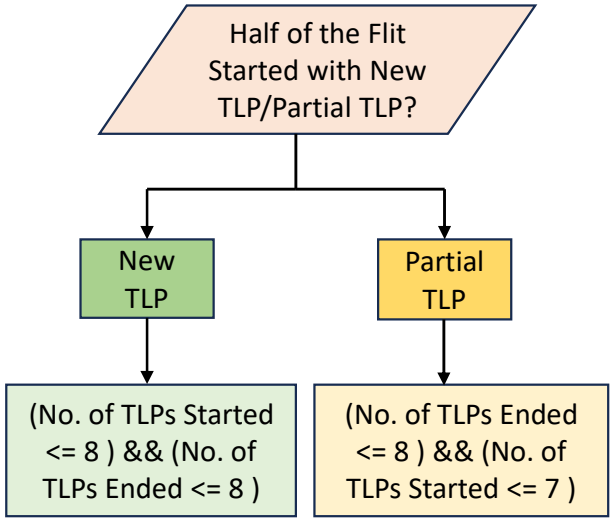
Flit Packing Rules

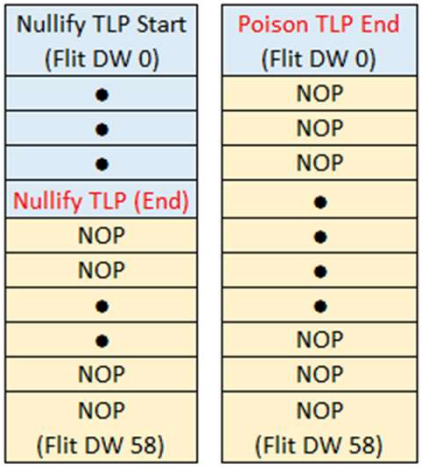
- Once a NOP (No operation) TLP is scheduled, it must continue until the next 4DW aligned boundary

- No more than 8 non - NOP TLPs, including partial TLPs in each Flit half
  1. First Half - 0 to 31 DWs
  2. Second Half – 32 to 58 DWs

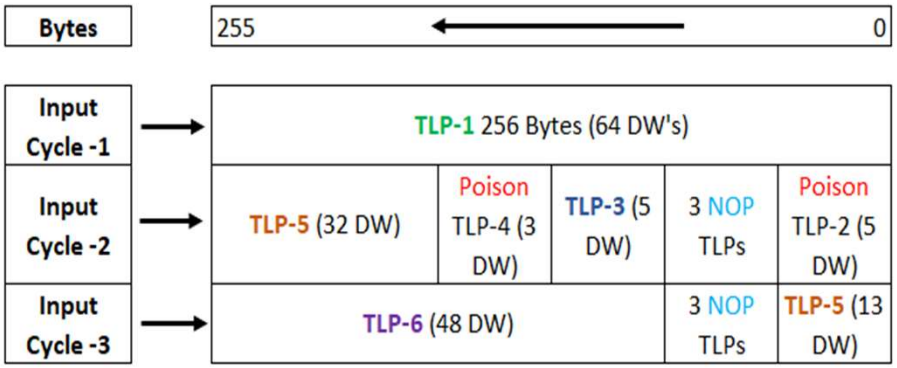
- Error TLP (Nullified or Poisoned) must be succeeded by only NOP TLPs through the end of the Flit.



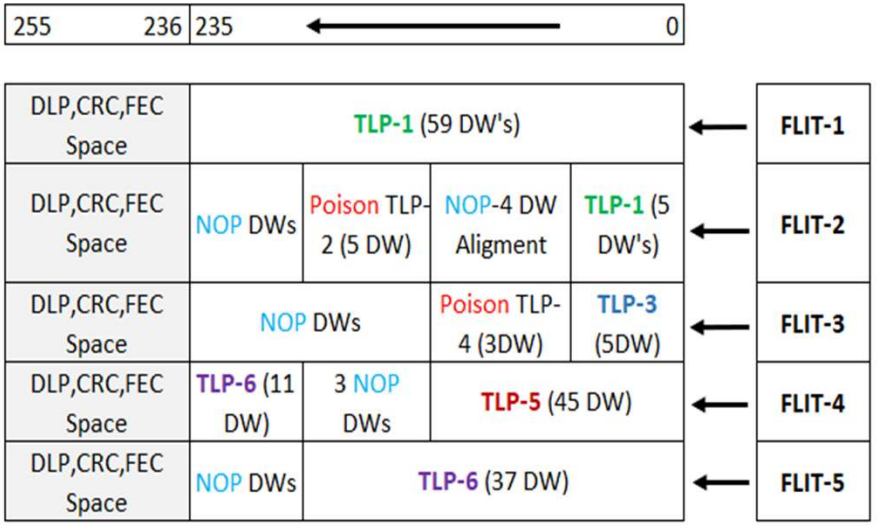




TLP’s Packing in Flit - Example



Input – TLP Data

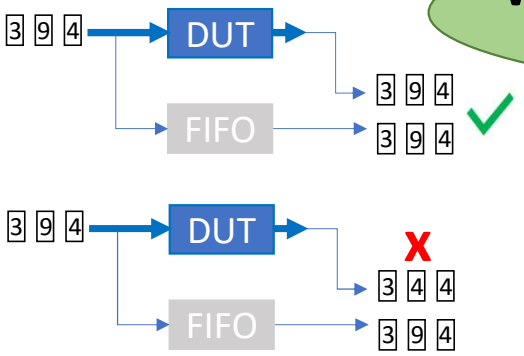


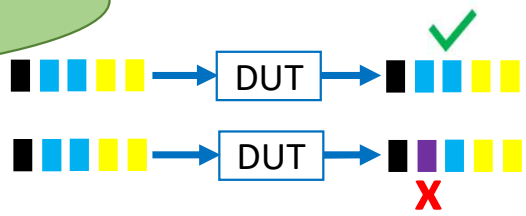
Output – FLIT Data

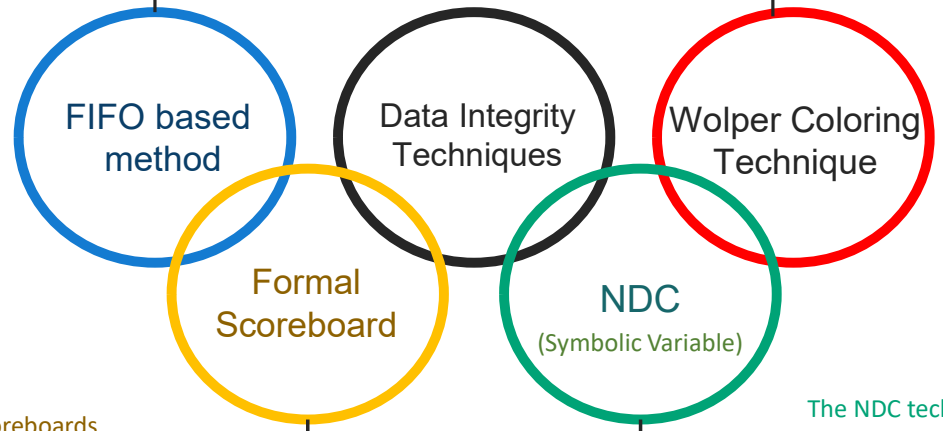
<< **Input TLP data gets shifted within a FLIT** due to packing rules, and the output data doesn’t directly match the input data

Traditional FV Data-Integrity techniques

work well when output data exactly matches the input in same order and content







FPV apps provide Formal Scoreboards. Scoreboard acts as a monitor of the DUT and embedded with all the required assertions for verification of end-to-end data integrity.

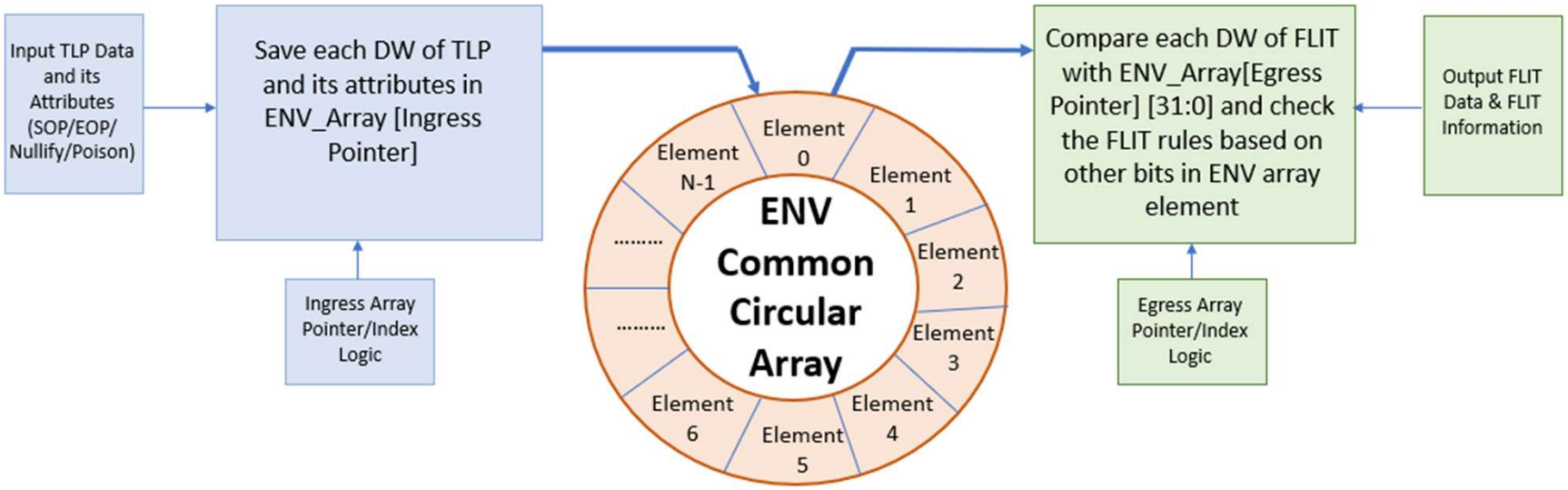
The NDC technique assertions use a variable whose value remains constant during a formal run. The assertions are triggered when the NDC variable value is seen at the input and verifies its appearance at the output after a defined delay.

Problem Statement

- The Flit packing rules introduce significant complexity which require extensive shifting and alignment of TLP data.
- Increases the risk of data integrity issues such as TLP DW corruption, duplication, dropping, and reordering.
- The Flit interface does not provide required TLP level details such as SOP DW, EOP DW, Nullify or Poison TLP end DW information.
- Traditional FV Data-Integrity techniques are ineffective.
- To address these challenges, a new FV approach is required to verify data integrity and Flit packing rules.

Array Centric Tracking (ACT) Methodology

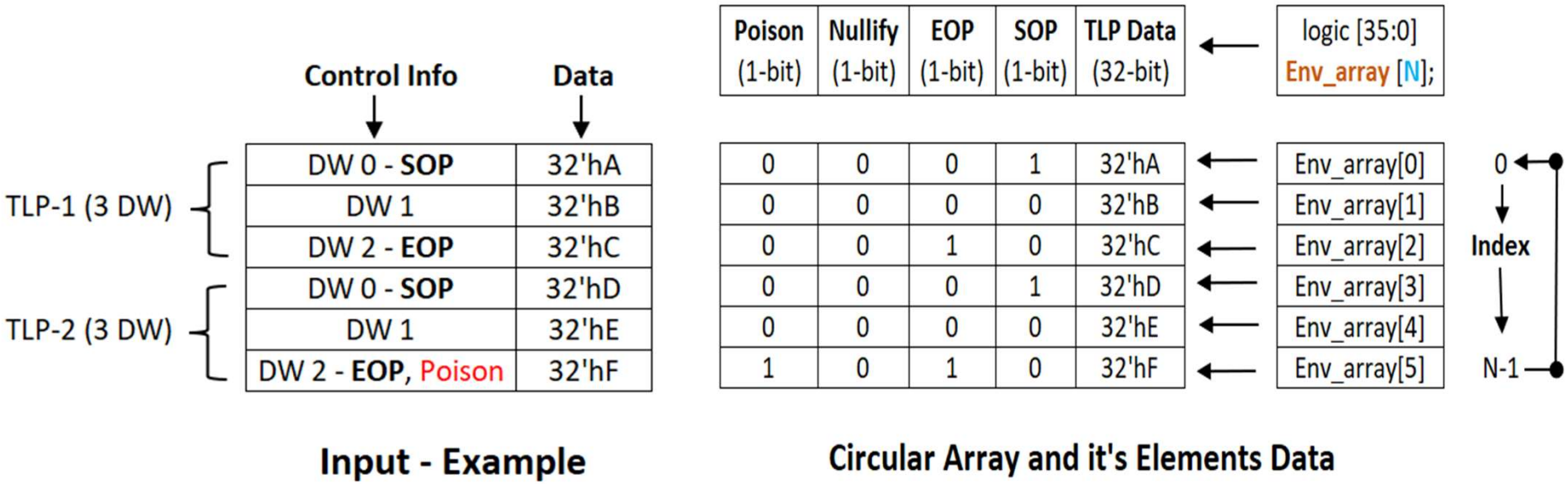
- ACT is a circular array-based approach
- Verifies data integrity at a DW (Double Word) level
- Tracks the start and end of each TLP to validate complex Flit rules



Note: Array Length (N) value depends upon design configuration. For eg data path, number of pipeline stages, etc.

ACT Ingress Flow

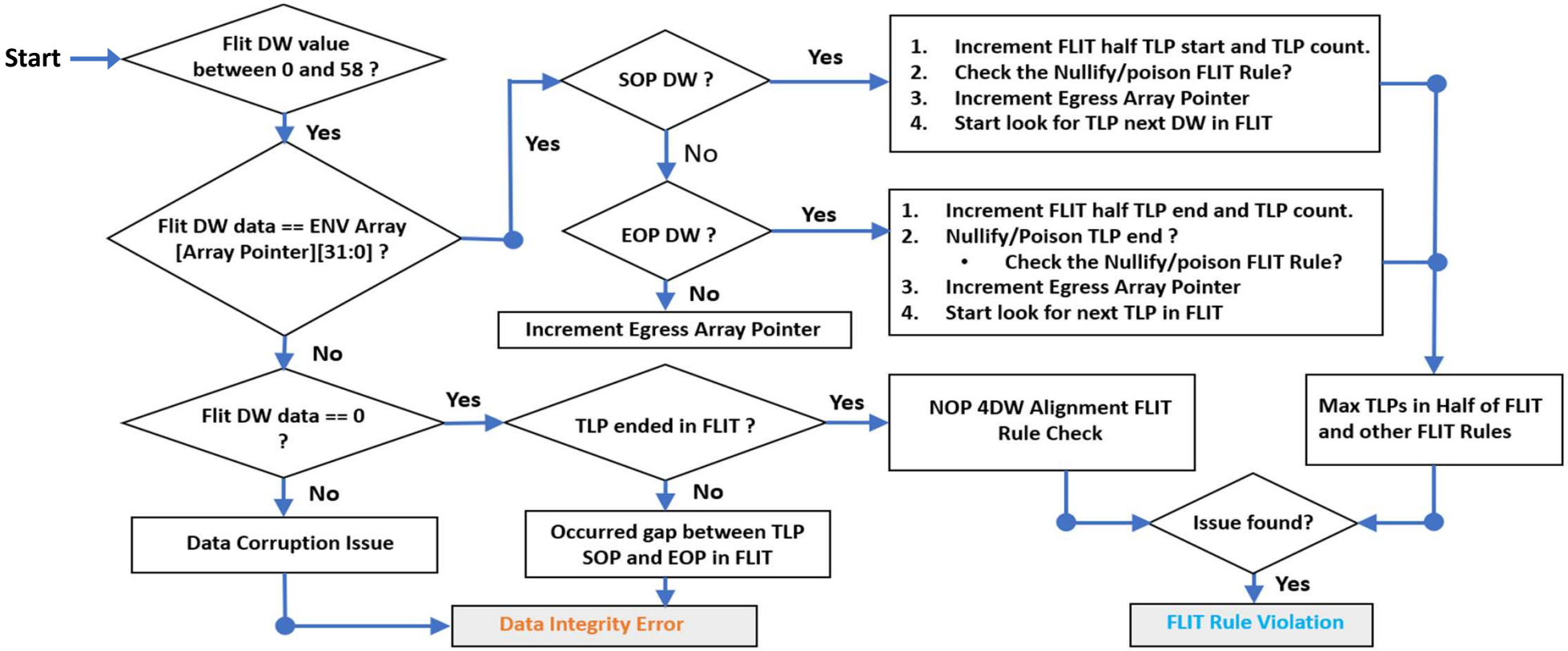
- Each DW of a non-NOP TLP is stored in the array, along with its attributes: SOP, EOP, Nullify, and Poison.



Input - Example

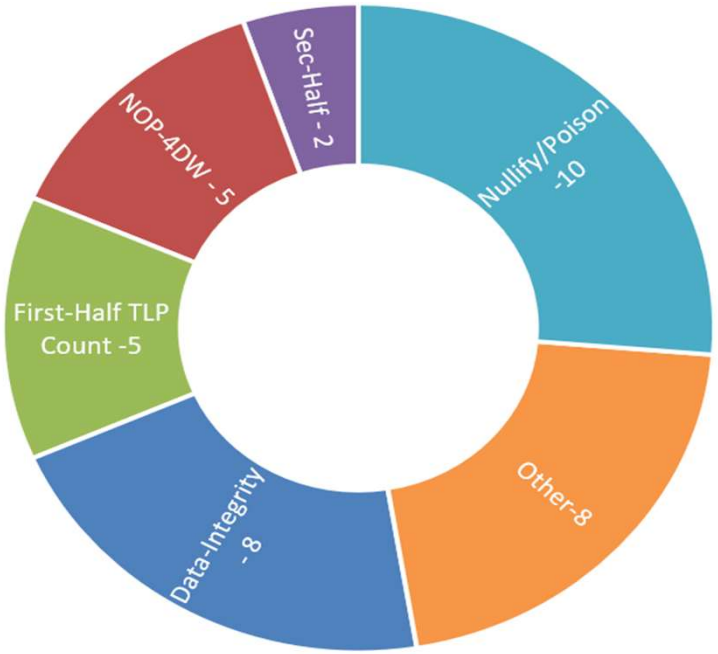
Circular Array and it's Elements Data

ACT Egress Flow



Results

- Identified a total number of 38 RTL bugs
- Array Centric Tracking (ACT) approach helped in uncovering a variety of elusive design issues



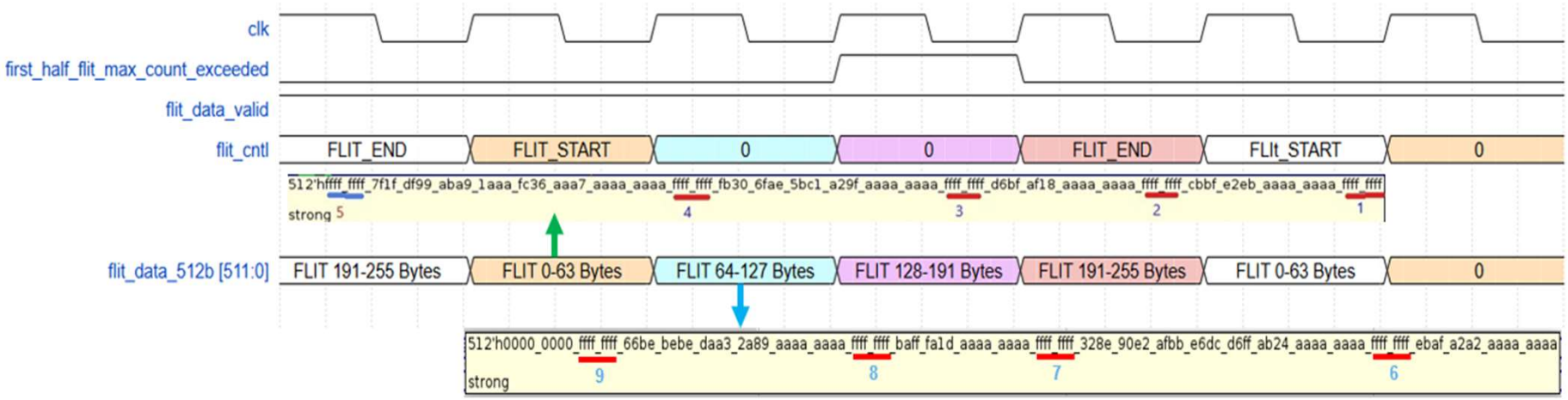
Bug - 1: Flit Packing Rule Violation

Expected Behavior :

- Packing more than 8 non-NOP TLP's including partial TLP's in each half of Flit is not allowed.

Behavior Violation :

- Data present in 0 to 127 Bytes represents the first half of flit in 512-bit data path.
- 1 partial TLP ended, 8 non-NOP TLP's started and ended in the first half of flit.



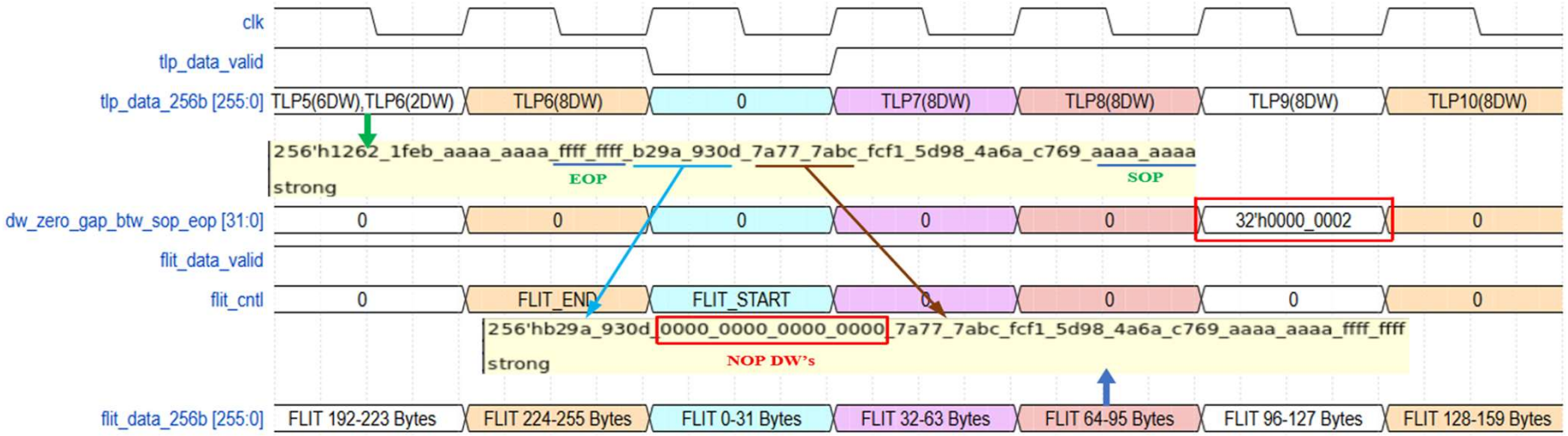
Bug - 2: Data Integrity Violation

Expected Behavior :

- Once a TLP starts, inserting NOP DWs (DW with value zero) before the TLP end is not allowed.

Behavior Violation :

- DUT incorrectly inserted two NOP DWs before the TLP ended within the Flit in a 256-bit data path



Application & Summary

- “Array Centric Tracking” is a versatile data integrity approach designed to handle complex Flit packing rules.
- Accurately verifies output features that depend on partial input data presence.
- Reusable across multiple designs and protocols, wherever traditional data integrity checks are applied.
- Easily adaptable to spec updates – e.g., PCIe Gen7’s TLP-per-half-Flit reduction
- Successfully identified 38 RTL bugs
- Scalable for emerging protocols like CXL, UCIe, and UALink

References

- PCI Express 6.0 Specification
  - https://pcisig.com/pci-express-6.0-specification
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- Dr. Shahid Ikram, Mark Eslinger, "Demystifying Formal Testbenches: Tips, Tricks, and Recommendations" DVCon US 2023.

Acknowledgements

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Q & A